

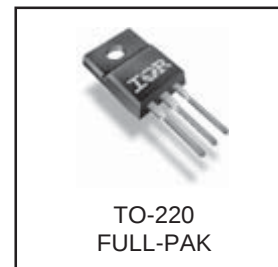
Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching

V_{DSS}	$R_{DS(on)}$ typ.	I_D
500V	290m Ω	6.7A

Benefits

- Low Gate Charge Q_g results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	6.7	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	4.2	
I_{DM}	Pulsed Drain Current ①	27	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	45	W
	Linear Derating Factor	0.36	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	17	V/ns
T_J	Operating Junction and	-55 to + 150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	1.1(10)	N•m (lbf•in)

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	290	mJ
I_{AR}	Avalanche Current ①	—	6.7	A
E_{AR}	Repetitive Avalanche Energy ①	—	4.5	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.76	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient	—	65	

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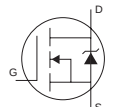
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.59	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	290	350	m Ω	$V_{GS} = 10V, I_D = 4.0A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	50	μA	$V_{DS} = 500V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 400V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	4.7	—	—	V	$V_{DS} = 50V, I_D = 4.0A$
Q_g	Total Gate Charge	—	—	89	nC	$I_D = 6.7A$
Q_{gs}	Gate-to-Source Charge	—	—	24		$V_{DS} = 400V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	44		$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	$V_{DD} = 250V$
t_r	Rise Time	—	16	—		$I_D = 6.7A$
$t_{d(off)}$	Turn-Off Delay Time	—	28	—		$R_G = 38\Omega$
t_f	Fall Time	—	8.4	—		$V_{GS} = 10V$ ④
C_{iss}	Input Capacitance	—	2160	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	240	—		$V_{DS} = 25V$
C_{riss}	Reverse Transfer Capacitance	—	27	—		$f = 1.0MHz$
C_{oss}	Output Capacitance	—	2600	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	62	—		$V_{GS} = 0V, V_{DS} = 400V, f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	120	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V$ ⑤

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	6.7	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ① ⑥	—	—	27		
V_{SD}	Diode Forward Voltage	—	—	2.0	V	$T_J = 25^\circ\text{C}, I_S = 6.7A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	430	640	ns	$T_J = 25^\circ\text{C}, I_F = 6.7A$
Q_{rr}	Reverse Recovery Charge	—	2840	4270	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11).
- ② Starting $T_J = 25^\circ\text{C}$, $L = 13mH$, $R_G = 25\Omega$, $I_{AS} = 6.7A$, $dv/dt = 17V/ns$ (See Figure 12a).
- ③ $I_{SD} \leq 6.7A$, $di/dt \leq 330A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$.

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

⑤ $C_{oss \text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

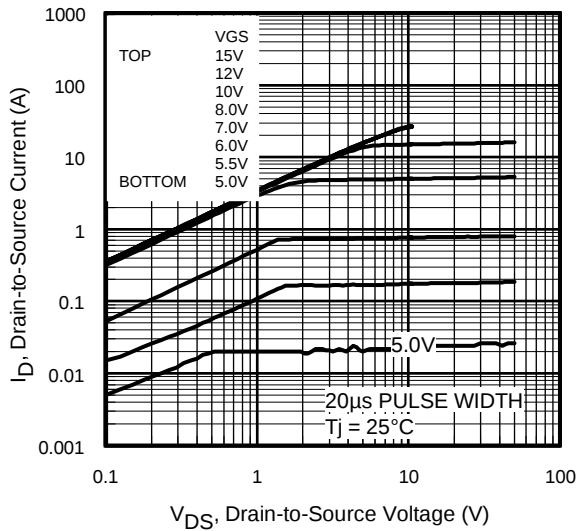


Fig 1. Typical Output Characteristics

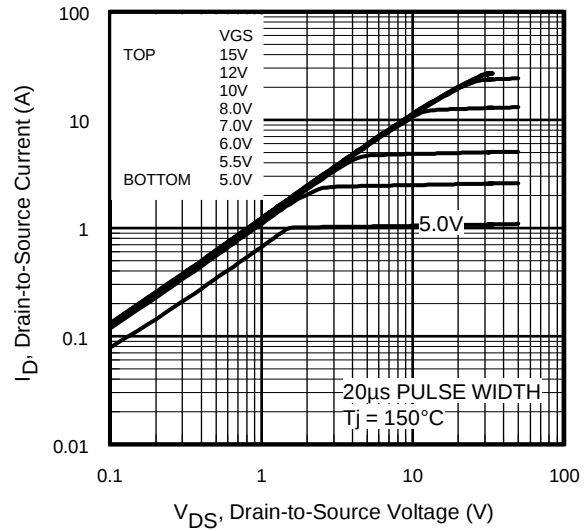


Fig 2. Typical Output Characteristics

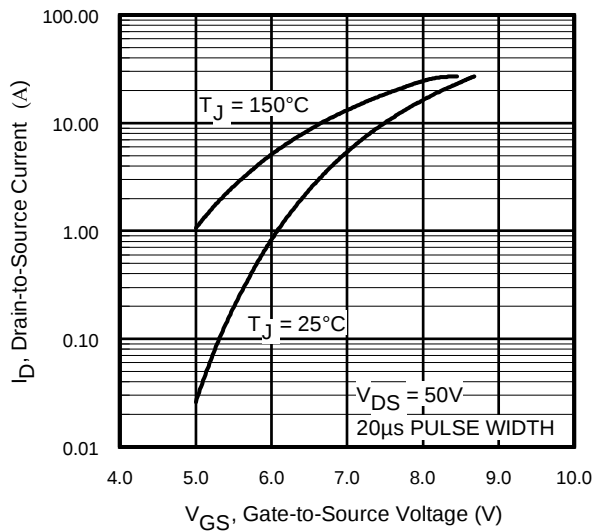


Fig 3. Typical Transfer Characteristics

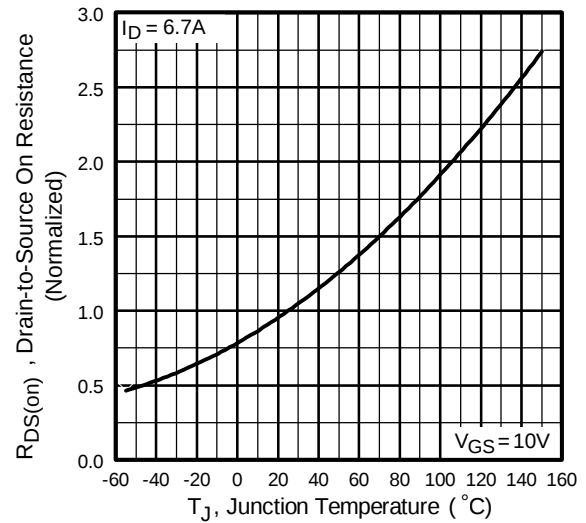


Fig 4. Normalized On-Resistance
Vs. Temperature

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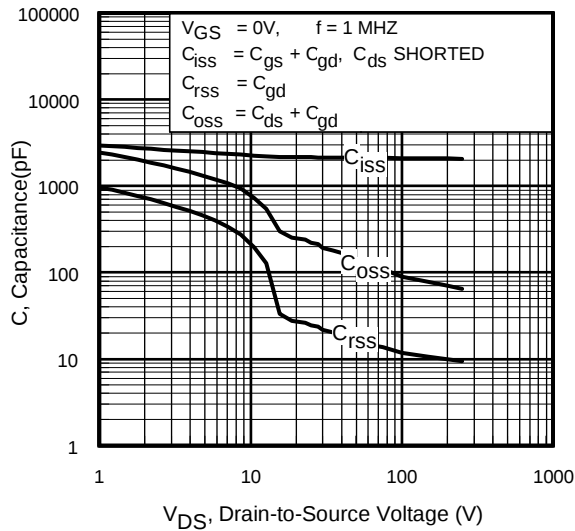


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

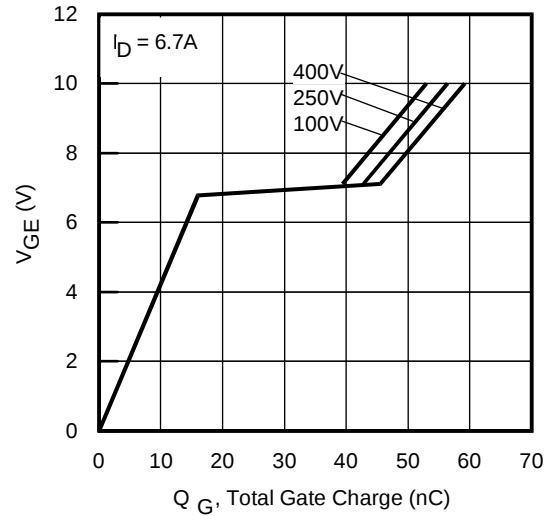


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

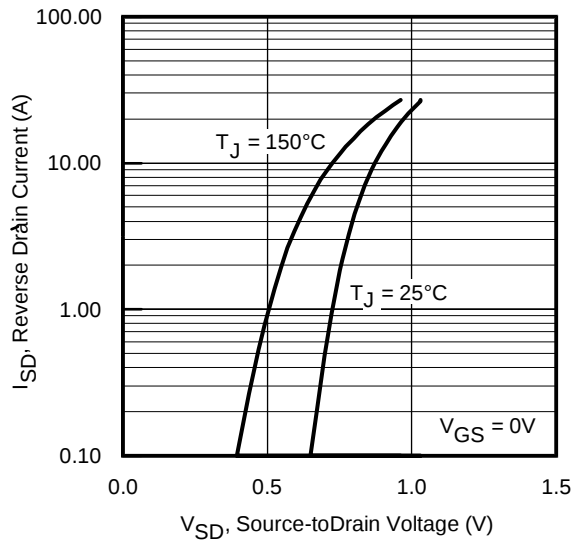


Fig 7. Typical Source-Drain Diode Forward Voltage

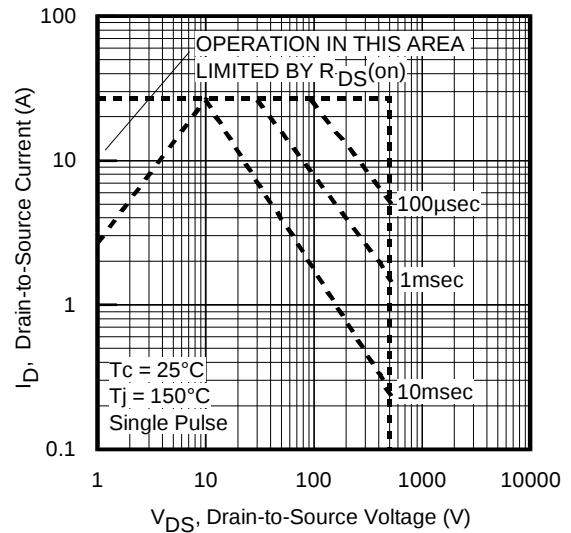


Fig 8. Maximum Safe Operating Area

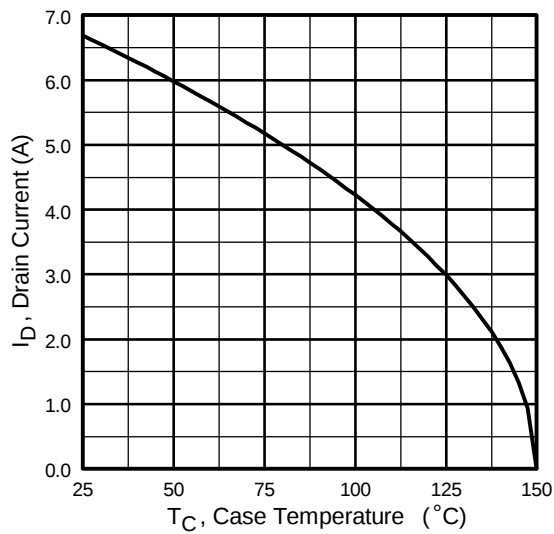


Fig 9. Maximum Drain Current Vs. Case Temperature

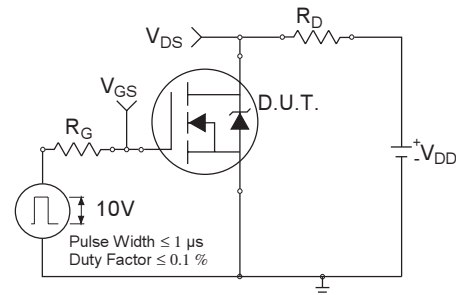


Fig 10a. Switching Time Test Circuit

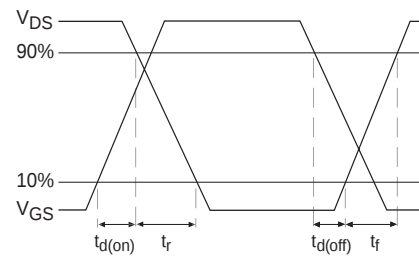


Fig 10b. Switching Time Waveforms

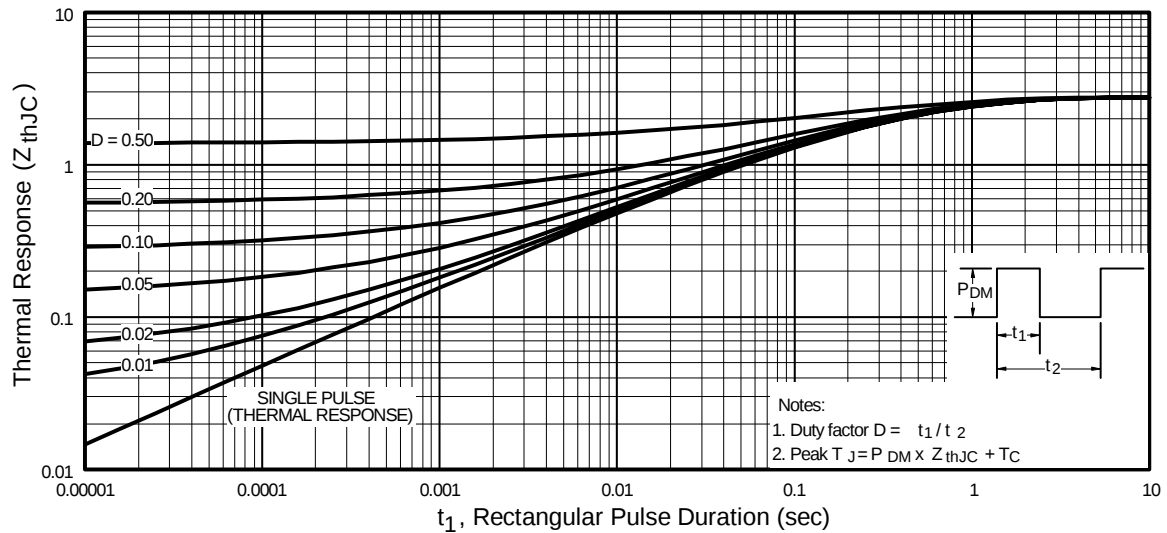


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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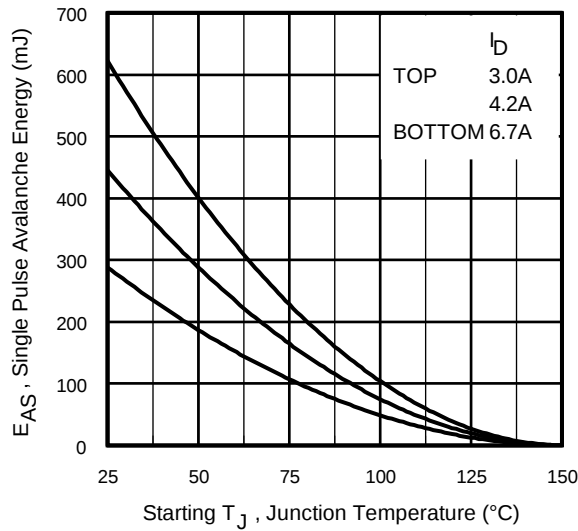


Fig 12a. Maximum Avalanche Energy Vs. Drain Current

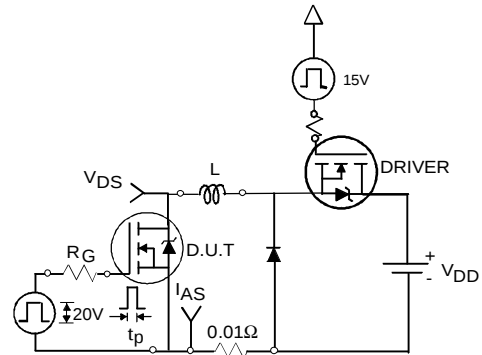


Fig 12c. Unclamped Inductive Test Circuit

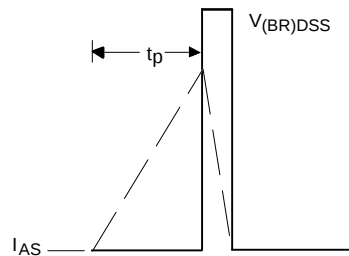


Fig 12d. Unclamped Inductive Waveforms

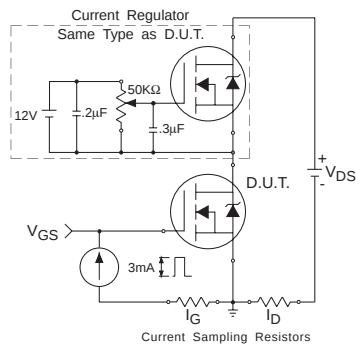


Fig 13a. Gate Charge Test Circuit

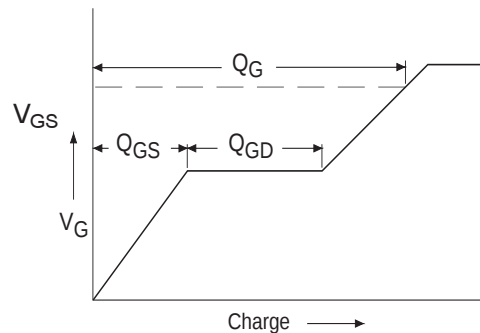
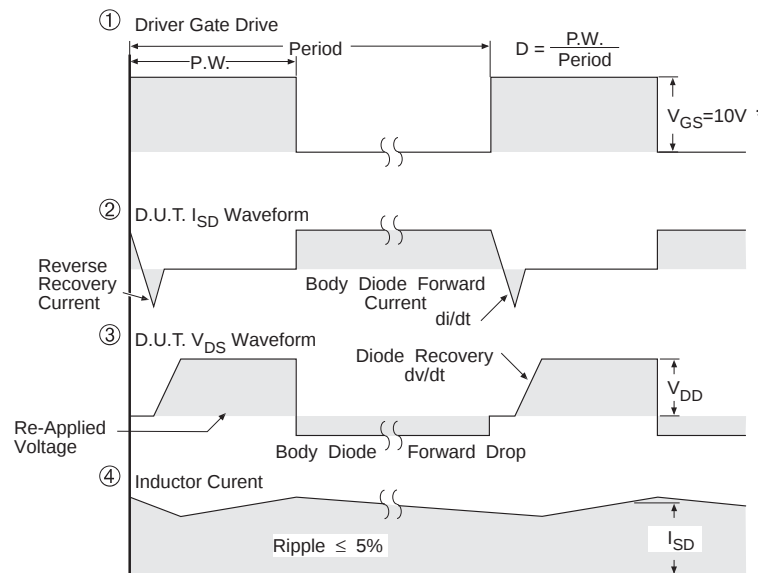
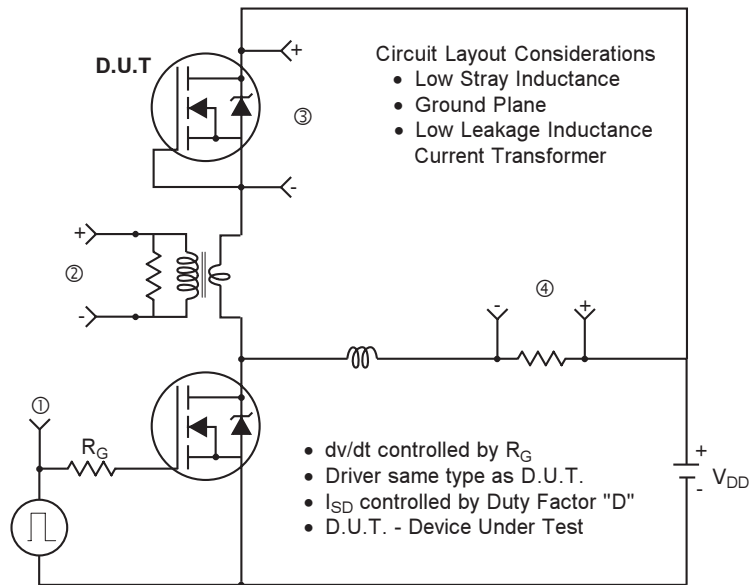


Fig 13b. Basic Gate Charge Waveform

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

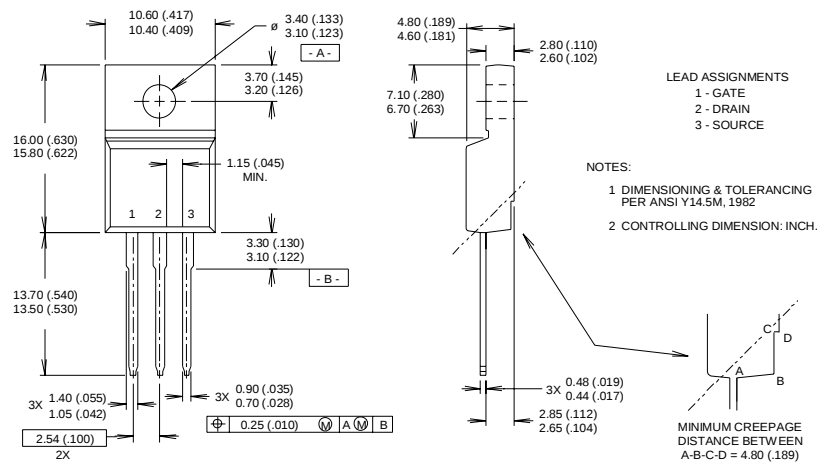
Fig 14. For N-Channel HEXFET® Power MOSFETs

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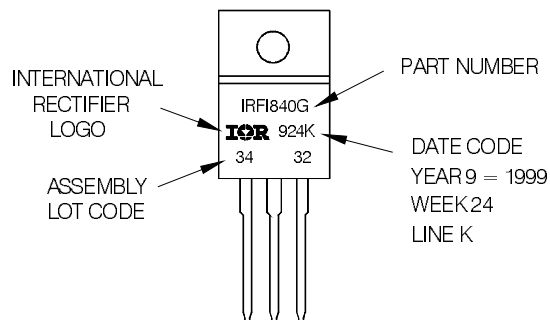
TO-220 Full-Pak Package Outline

Dimensions are shown in millimeters (inches)



TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRF1840G
WITH ASSEMBLY
LOT CODE 3432
ASSEMBLED ON WW 24 1999
IN THE ASSEMBLY LINE "K"



TO-220 Full-Pak package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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