

# SCAN18540T

## Inverting Line Driver with 3-STATE Outputs

### General Description

The SCAN18540T is a high speed, low-power line driver featuring separate data inputs organized into dual 9-bit bytes with byte-oriented paired output enable control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

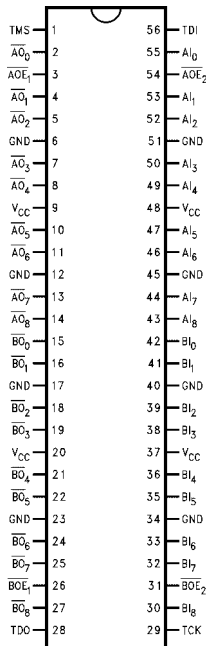
### Features

- IEEE 1149.1 (JTAG) compliant
- Dual output enable signals per byte
- 3-STATE outputs for bus-oriented applications
- 9-bit data busses for parity applications
- Reduced-swing outputs source 32 mA/sink 64 mA
- Guaranteed to drive 50Ω transmission line to TTL input levels of 0.8V and 2.0V
- TTL compatible inputs
- 25 mil pitch SSOP (Shrink Small Outline Package)
- Includes CLAMP and HIGHZ instructions
- Member of Fairchild's SCAN products

### Ordering Code:

Order Number	Package Number	Package Description
SCAN18540TSSC	MS54A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide

### Connection Diagram



### Pin Descriptions

Pin Names	Description
$AI_{(0-8)}$	Input pins, A side
$BI_{(0-8)}$	Input pins, B side
$\overline{AOE}_1, \overline{AOE}_2$	3-STATE Output Enable Input pins, A side
$\overline{BOE}_1, \overline{BOE}_2$	3-STATE Output Enable Input pins, B side
$\overline{AO}_{(0-8)}$	Output pins, A side
$\overline{BO}_{(0-8)}$	Output pins, B side

### Truth Tables

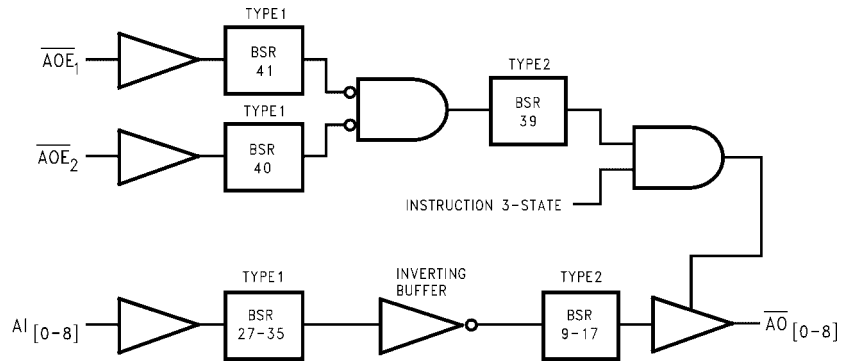
Inputs			$\overline{AO}_{(0-8)}$
$\overline{AOE}_1$	$\overline{AOE}_2$	$AI_{(0-8)}$	
L	L	H	L
H	X	X	Z
X	H	X	Z
L	L	L	H

Inputs			$\overline{BO}_{(0-8)}$
$\overline{BOE}_1$	$\overline{BOE}_2$	$BI_{(0-8)}$	
L	L	H	L
H	X	X	Z
X	H	X	Z
L	L	L	H

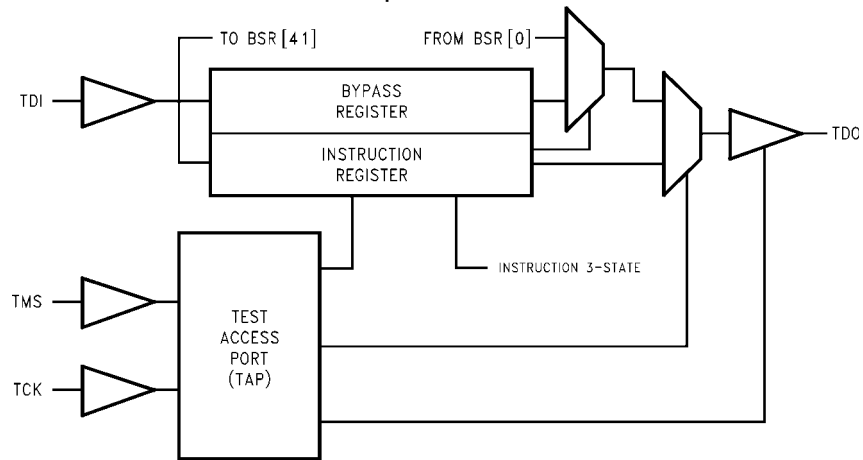
H = HIGH Voltage Level X = Immaterial  
L = LOW Voltage Level Z = High Impedance

## Block Diagrams

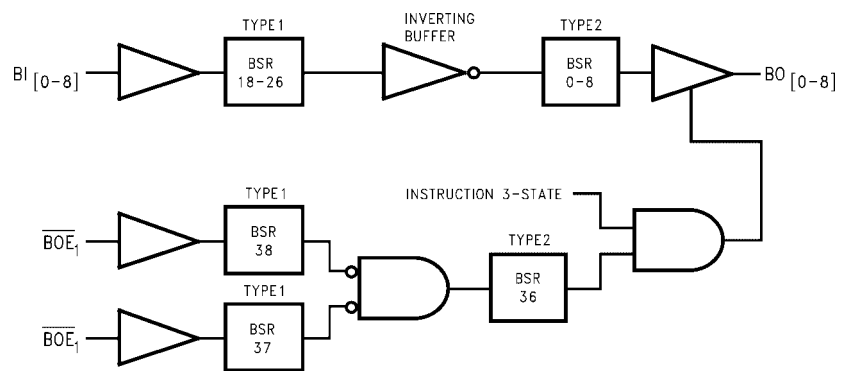
### Byte-A



### Tap Controller



### Byte-B



**Note:** BSR stands for Boundary Scan Register

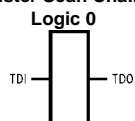
## Description of BOUNDARY-SCAN Circuitry

The scan cells used in the BOUNDARY-SCAN register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data.

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

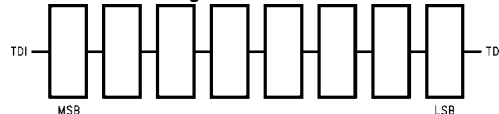
### Bypass Register Scan Chain Definition



The INSTRUCTION register is an 8-bit register which captures the default value of 01001101. The two least significant bits of this captured value (01) are required by IEEE

Std 1149.1. The upper six bits are unique to the SCAN18540T device. SCAN CMOS Test Access Logic devices do not include the IEEE 1149.1 optional identification register. Therefore, this unique captured value can be used as a "pseudo ID" code to confirm that the correct device is placed in the appropriate location in the boundary scan chain.

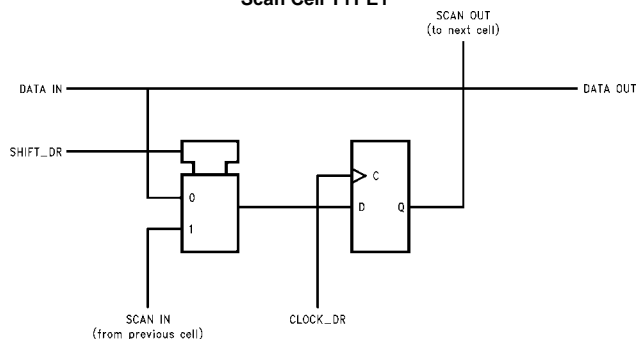
### Instruction Register Scan Chain Definition



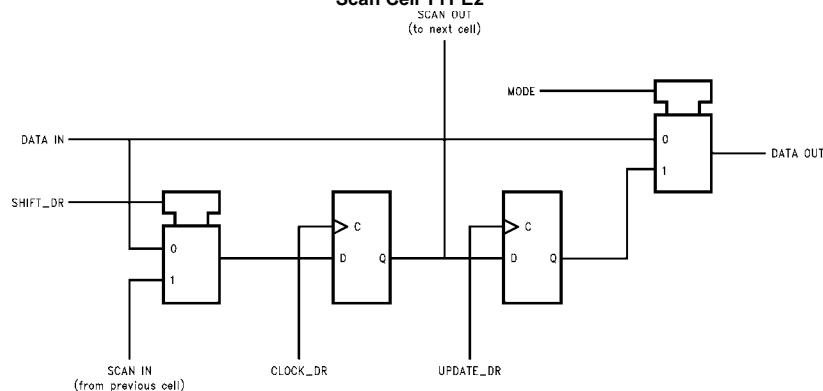
MSB→LSB

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGH-Z
All Others	BYPASS

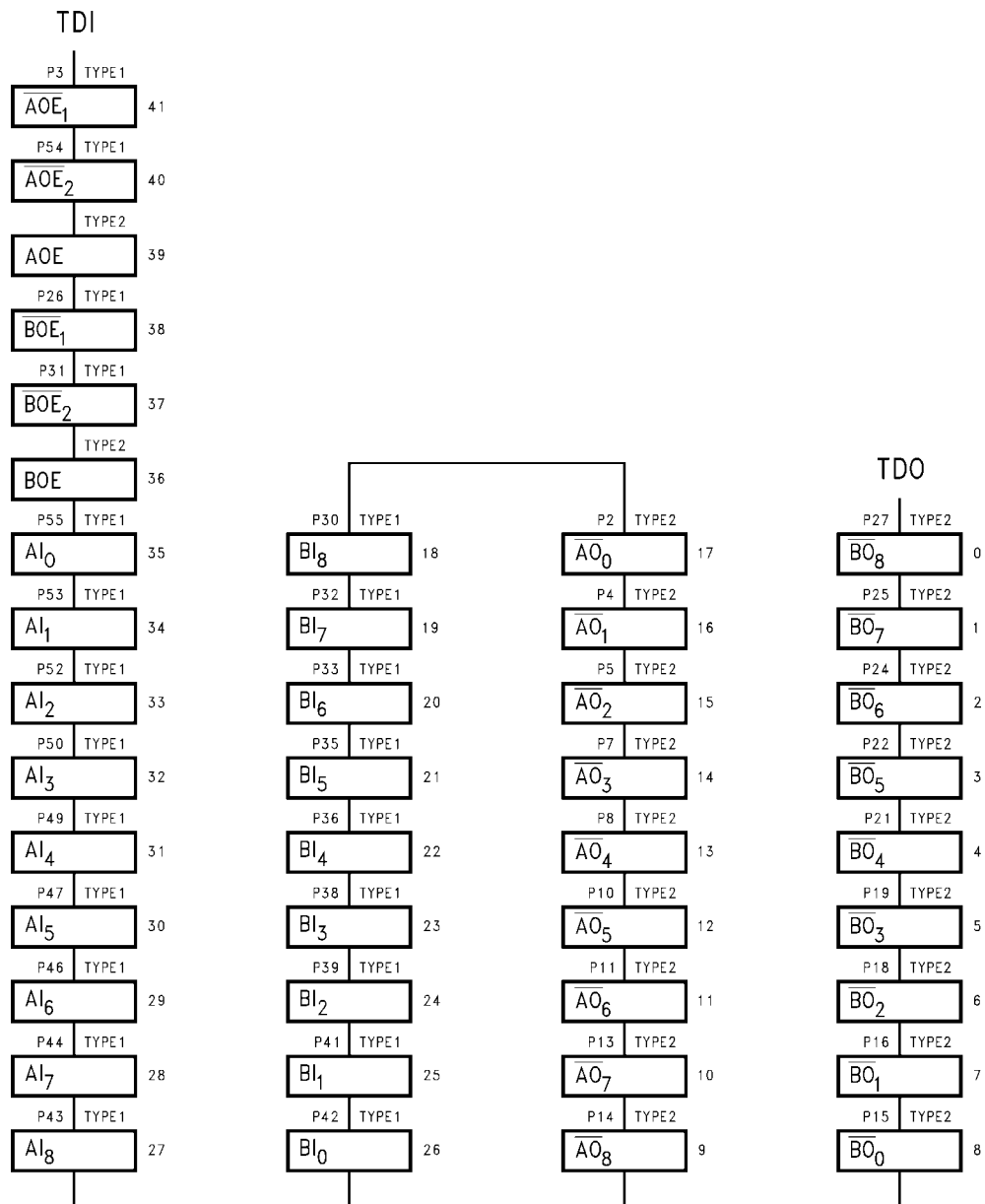
### Scan Cell TYPE1



### Scan Cell TYPE2



**BOUNDARY-SCAN Register**  
**Scan Chain Definition (42 Bits in Length)**



BOUNDARY-SCAN Register Definition Index

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
41	$\overline{AOE}_1$	3	Input	TYPE1	Control Signals
40	$\overline{AOE}_2$	54	Input	TYPE1	
39	AOE		Internal	TYPE2	
38	$\overline{BOE}_1$	26	Input	TYPE1	
37	$\overline{BOE}_2$	31	Input	TYPE1	
36	BOE		Internal	TYPE2	
35	AI <sub>0</sub>	55	Input	TYPE1	A-in
34	AI <sub>1</sub>	53	Input	TYPE1	
33	AI <sub>2</sub>	52	Input	TYPE1	
32	AI <sub>3</sub>	50	Input	TYPE1	
31	AI <sub>4</sub>	49	Input	TYPE1	
30	AI <sub>5</sub>	47	Input	TYPE1	
29	AI <sub>6</sub>	46	Input	TYPE1	
28	AI <sub>7</sub>	44	Input	TYPE1	
27	AI <sub>8</sub>	43	Input	TYPE1	
26	BI <sub>0</sub>	42	Input	TYPE1	B-in
25	BI <sub>1</sub>	41	Input	TYPE1	
24	BI <sub>2</sub>	39	Input	TYPE1	
23	BI <sub>3</sub>	38	Input	TYPE1	
22	BI <sub>4</sub>	36	Input	TYPE1	
21	BI <sub>5</sub>	35	Input	TYPE1	
20	BI <sub>6</sub>	33	Input	TYPE1	
19	BI <sub>7</sub>	32	Input	TYPE1	
18	BI <sub>8</sub>	30	Input	TYPE1	
17	AO <sub>0</sub>	2	Output	TYPE2	A-out
16	AO <sub>1</sub>	4	Output	TYPE2	
15	AO <sub>2</sub>	5	Output	TYPE2	
14	AO <sub>3</sub>	7	Output	TYPE2	
13	AO <sub>4</sub>	8	Output	TYPE2	
12	AO <sub>5</sub>	10	Output	TYPE2	
11	AO <sub>6</sub>	11	Output	TYPE2	
10	AO <sub>7</sub>	13	Output	TYPE2	
9	AO <sub>8</sub>	14	Output	TYPE2	
8	BO <sub>0</sub>	15	Output	TYPE2	B-in
7	BO <sub>1</sub>	16	Output	TYPE2	
6	BO <sub>2</sub>	18	Output	TYPE2	
5	BO <sub>3</sub>	19	Output	TYPE2	
4	BO <sub>4</sub>	21	Output	TYPE2	
3	BO <sub>5</sub>	22	Output	TYPE2	
2	BO <sub>6</sub>	24	Output	TYPE2	
1	BO <sub>7</sub>	25	Output	TYPE2	
0	BO <sub>8</sub>	27	Output	TYPE2	

**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ )	–0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	–20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	–20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	–0.5V to $V_{CC} + 0.5V$
DC Output Source/Sink Current ( $I_O$ )	±70 mA
DC $V_{CC}$ or Ground Current	
Per Output Pin	±70 mA
Junction Temperature	
SSOP	+140°C
Storage Temperature	–65°C to +150°C
ESD (Min)	2000V

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	4.5V to 5.5V
SCAN Products	
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	–40°C to +85°C
Minimum Input Edge Rate $\Delta V/\Delta t$	125 mV/ns
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of SCAN circuits outside databook specifications.

**DC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V <sub>IH</sub>	Minimum HIGH Input Voltage	4.5	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V
		5.5	1.5	2.0	2.0		
V <sub>IL</sub>	Maximum LOW Input Voltage	4.5	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V
		5.5	1.5	0.8	0.8		
V <sub>OH</sub>	Minimum HIGH Output Voltage (Note 2)	4.5		3.15	3.15	V	I <sub>OUT</sub> = −50 μA
		5.5		4.15	4.15		
		4.5		2.4	2.4	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −32 mA
		5.5		2.4	2.4		
		4.5		2.4		V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = −24 mA
V <sub>OL</sub>	Maximum LOW Output Voltage (Note 2)	4.5		0.1	0.1	V	I <sub>OUT</sub> = 50 μA
		5.5		0.1	0.1		
		4.5		0.55	0.55	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 64 mA
		5.5		0.55	0.55		
		4.5		0.55		V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 48 mA
I <sub>IN</sub>	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND
I <sub>IN</sub> TDI, TMS	Maximum Input Leakage	5.5		2.8	3.6	μA	V <sub>I</sub> = V <sub>CC</sub>
				−385	−385	μA	V <sub>I</sub> = GND
	Minimum Input Leakage	5.5		−160	−160	μA	V <sub>I</sub> = GND
I <sub>OLD</sub>	Minimum Dynamic	5.5		94	94	mA	V <sub>OLD</sub> = 0.8V Max
I <sub>OHD</sub>	Output Current (Note 3)			−40	−40	mA	V <sub>OHD</sub> = 2.0V Min
I <sub>OZ</sub>	Maximum Output Leakage Current	5.5		±0.5	±5.0	μA	V <sub>I</sub> (OE) = V <sub>IL</sub> , V <sub>IH</sub>
I <sub>OS</sub>	Output Short Circuit Current	5.5		−100	−100	mA Min	V <sub>O</sub> = 0V
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5		16.0	88	μA	V <sub>O</sub> = Open TDI, TMS = V <sub>CC</sub>
		5.5		750	820	μA	V <sub>O</sub> = Open TDI, TMS = GND

**DC Electrical Characteristics** (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
I <sub>CC1</sub>	Maximum I <sub>CC</sub> Per Input	5.5		2.0	2.0	mA	V <sub>I</sub> = V <sub>CC</sub> -2.1V
		5.5		2.15	2.15	mA	V <sub>I</sub> = V <sub>CC</sub> -2.1V TDI/TMS Pin, Test One with the other Floating

**Note 2:** All outputs loaded; thresholds associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

**Noise Specifications**

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C	Units
			Typ	Guaranteed Limits		
V <sub>OLP</sub>	Maximum HIGH Output Noise (Note 4)(Note 5)	5.0	1.0	1.5		V
V <sub>OLV</sub>	Minimum LOW Output Noise (Note 4)(Note 5)	5.0	−0.6	−1.2		V
V <sub>OHP</sub>	Maximum Overshoot (Note 5)(Note 6)	5.0	V <sub>OH</sub> +1.0	V <sub>OH</sub> +1.5		V
V <sub>OHV</sub>	Minimum V <sub>CC</sub> Droop (Note 6)(Note 5)	5.0	V <sub>OH</sub> −1.0	V <sub>OH</sub> −1.8		V
V <sub>IHD</sub>	Minimum HIGH Dynamic Input Voltage Level (Note 6)(Note 7)	5.5	1.6	2.0	2.0	V
V <sub>ILD</sub>	Maximum LOW Dynamic Input Voltage Level (Note 6)(Note 7)	5.5	1.4	0.8	0.8	V

**Note 4:** Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched LOW and one output held LOW.

**Note 5:** Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched HIGH and one output held HIGH.

**Note 6:** Worst case package.

**Note 7:** Maximum number of data inputs (n) switching. (n-1) input switching 0V to 3V. Input under test switching 3V to threshold (V<sub>ILD</sub>).

**AC Electrical Characteristics**

Normal Operation:

Symbol	Parameter	V <sub>CC</sub> (V) (Note 8)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	5.0	2.5		9.0	2.5	9.8	ns
t <sub>PHL</sub>	Data to Q		2.5		9.0	2.5	9.8	
t <sub>PLZ</sub>	Disable Time	5.0	1.5		10.2	1.5	10.7	ns
t <sub>PHZ</sub>			1.5		10.2	1.5	10.7	
t <sub>PZL</sub>	Enable Time	5.0	2.0		11.8	2.0	12.8	ns
t <sub>PZH</sub>			2.0		9.5	2.0	10.5	

**Note 8:** Voltage Range 5.0 is 5.0V ± 0.5V.

**Note:** All Input Timing Delays involving TCK are measured from the rising edge of TCK.

## AC Electrical Characteristics

Scan Test Operation:

Symbol	Parameter	V <sub>CC</sub> (V) (Note 9)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay TCK to TDO	5.0	3.5		13.2	3.5	14.5	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Disable Time TCK to TDO	5.0	2.5		11.5	2.5	11.9	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Enable Time TCK to TDO	5.0	3.0		14.5	3.0	15.8	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay TCK to Data Out During Update- -DR State	5.0	5.0		18.0	5.0	19.8	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay TCK to Data Out During Update- IR State	5.0	5.0		18.6	5.0	20.2	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	5.5		19.9	5.5	21.5	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Propagation Delay TCK to Data Out During Update- DR State	5.0	4.0		16.4	4.0	18.2	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Propagation Delay TCK to Data Out During Update- IR State	5.0	5.0		19.5	5.0	20.8	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	5.0		19.9	5.0	21.5	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Propagation Delay TCK to Data Out During Update- DR State	5.0	5.0		18.9	5.0	20.9	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Propagation Delay TCK to Data Out During Update- IR State	5.0	6.5		22.4	6.5	24.2	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	7.0		23.8	7.0	25.7	ns

**Note 9:** Voltage Range 5.0 is 5.0V ± 0.5V.

**Note:** All Input Timing Delays involving TCK are measured from the rising edge of TCK.



## AC Operating Requirements

Scan Test Operation:

Symbol	Parameter	V <sub>CC</sub> (V) (Note 10)	T <sub>A</sub> = +25°C	T <sub>A</sub> = -40°C to +85°C	Units
			C <sub>L</sub> = 50 pF	C <sub>L</sub> = 50 pF	
			Guaranteed Minimum		
t <sub>S</sub>	Setup Time, H or L Data to TCK (Note 11)	5.0	3.0	3.0	ns
t <sub>H</sub>	Hold Time, H or L TCK to Data (Note 11)	5.0	4.5	4.5	ns
t <sub>S</sub>	Setup Time, H or L AOE <sub>n</sub> , BOE <sub>n</sub> to TCK (Note 12)	5.0	3.0	3.0	ns
t <sub>H</sub>	Hold Time, H or L TCK to AOE <sub>n</sub> , BOE <sub>n</sub> (Note 12)	5.0	4.5	4.5	ns
t <sub>S</sub>	Setup Time, H or L Internal AOE, BOE, to TCK (Note 13)	5.0	3.0	3.0	ns
t <sub>H</sub>	Hold Time, H or L TCK to Internal AOE, BOE (Note 13)	5.0	3.0	3.0	ns
t <sub>S</sub>	Setup Time, H or L TMS to TCK	5.0	8.0	8.0	ns
t <sub>H</sub>	Hold Time, H or L TCK to TMS	5.0	2.0	2.0	ns
t <sub>S</sub>	Setup Time, H or L TDI to TCK	5.0	4.0	4.0	ns
t <sub>H</sub>	Hold Time, H or L TCK to TDI	5.0	4.5	4.5	ns
t <sub>W</sub>	Pulse Width TCK	5.0	15.0 5.0	15.0 5.0	ns
f <sub>MAX</sub>	Maximum TCK Clock Frequency	5.0	25	25	MHz
T <sub>PU</sub>	Wait Time, Power Up to TCK	5.0	100	100	ns
T <sub>DN</sub>	Power Down Delay	0.0	100	100	ms

**Note 10:** Voltage Range 5.0 is 5.0V ± 0.5V.

**Note 11:** This delay represents the timing relationship between the data input and TCK at the associated scan cells numbered 0-8, 9-17, 18-26, and 27-35.

**Note 12:** Timing pertains to BSR 37, 38, 40 and 41.

**Note 13:** This delay represents the timing relationship between AOE/BOE and TCK for scan cells 36 and 39 only.

**Note:** All Input Timing Delays involving TCK are measured from the rising edge of TCK.

## Extended AC Electrical Characteristics

Symbol	Parameter	$T_A = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$ $C_L = 50\text{ pF}$ 18 Outputs Switching (Note 14)			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 0.5\text{V}$ $C_L = 250\text{ pF}$ (Note 15)		Units
		Min	Typ	Max	Min	Max	
$t_{PLH}$	Propagation Delay	3.0		11.0	4.0	13.0	ns
$t_{PHL}$	Data to Output	3.0		11.0	4.0	15.0	
$t_{PZH}$	Output Enable Time	2.5		11.5	(Note 16)		ns
$t_{PZL}$		2.5		14.0			
$t_{PHZ}$	Output Disable Time	2.0		11.5	(Note 17)		ns
$t_{PLZ}$		2.0		11.5			
$t_{OSHL}$ (Note 18)	Pin to Pin Skew HL Data to Output		0.5	1.0		1.0	ns
$t_{OSLH}$ (Note 18)	Pin to Pin Skew LH Data to Output		0.5	1.0		1.0	ns

**Note 14:** This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW etc.).

**Note 15:** This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

**Note 16:** 3-STATE delays are load dominated and have been excluded from the datasheet.

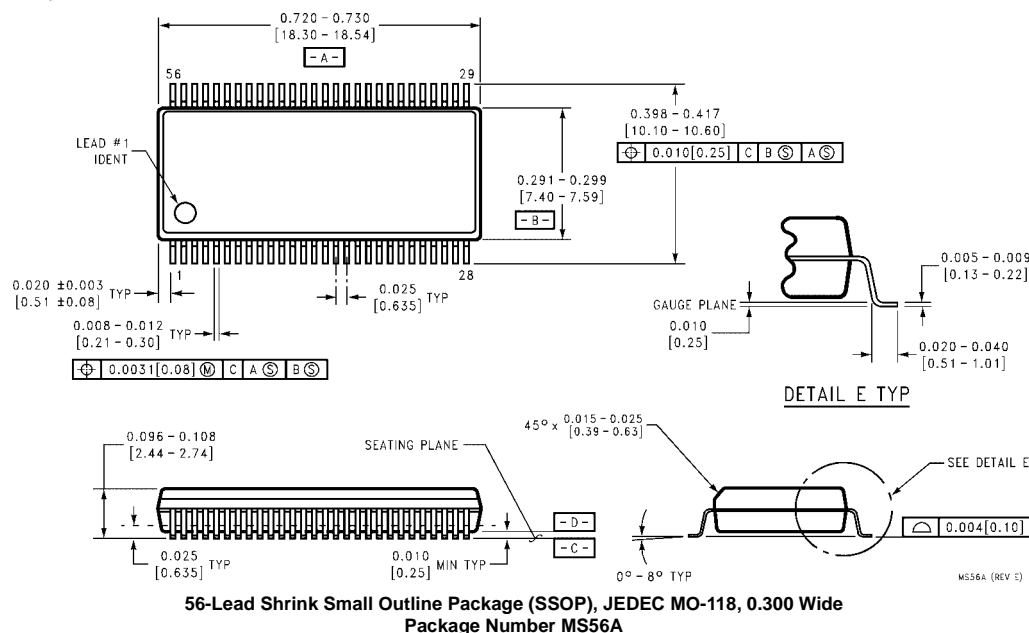
**Note 17:** The Output Disable Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

**Note 18:** Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW ( $t_{OSHL}$ ), LOW-to-HIGH ( $t_{OSLH}$ ), or any combination LOW-to-HIGH and/or HIGH-to-LOW.

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
$C_{IN}$	Input Pin Capacitance	4.0	pF	$V_{CC} = 5.0\text{V}$
$C_{OUT}$	Output Pin Capacitance	13.0	pF	$V_{CC} = 5.0\text{V}$
$C_{PD}$	Power Dissipation Capacitance	34.0	pF	$V_{CC} = 5.0\text{V}$

# Physical Dimensions inches (millimeters) unless otherwise noted



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