

## 2A, 80V and 100V, 1.050 Ohm, Logic Level, N-Channel Power MOSFETs

The RFP2N08L and RFP2N10L are N-Channel enhancement mode silicon gate power field effect transistors specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V to 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

Formerly developmental type TA0924.

### Ordering Information

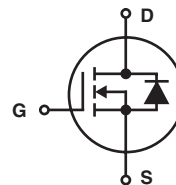
PART NUMBER	PACKAGE	BRAND
RFP2N08L	TO-220AB	RFP2N08L
RFP2N10L	TO-220AB	RFP2N10L

NOTE: When ordering, include the entire part number.

### Features

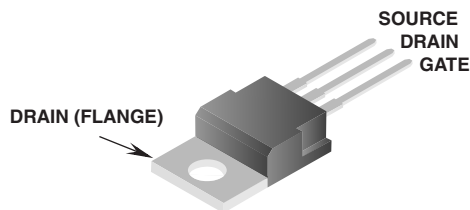
- 2A, 80V and 100V
- $r_{DS(ON)} = 1.050\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

### Symbol



### Packaging

JEDEC TO-220AB



# RFP2N08L, RFP2N10L

## Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

	RFP2N08L	RFP2N10L	UNITS	
Drain to Source Voltage (Note 1) . . . . .	$V_{DS}$	80	100	V
Drain to Gate Voltage ( $R_{GS} = 1M\Omega$ ) (Note 1) . . . . .	$V_{DGR}$	80	100	V
Continuous Drain Current . . . . .	$I_D$	2	2	A
Pulsed Drain Current (Note 3) . . . . .	$I_{DM}$	5	5	A
Gate to Source Voltage . . . . .	$V_{GS}$	$\pm 10$	$\pm 10$	V
Maximum Power Dissipation . . . . .	$P_D$	25	25	W
Derate above 25°C. . . . .		0.2	0.2	W/°C
Operating and Storage Temperature . . . . .	$T_J, T_{STG}$	-55 to 150	-55 to 150	°C
Maximum Temperature for Soldering				
Leads at 0.063in (1.6mm) from Case for 10s. . . . .	$T_L$	300	300	°C
Package Body for 10s, See Techbrief 334 . . . . .	$T_{pkg}$	260	260	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

1.  $T_J = 25^\circ\text{C}$  to  $125^\circ\text{C}$ .

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	80	-	-	V
RFP2N08L						
RFP2N10L			100	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1.0	-	2.0	V
Gate to Source Leakage	$I_{GSS}$	$V_{GS} = \pm 10\text{V}, V_{DS} = 0\text{V}$	-	-	$\pm 100$	nA
Zero to Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}$	-	-	1.0	$\mu\text{A}$
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}, T_C = 125^\circ\text{C}$	-	-	25	$\mu\text{A}$
Drain to Source On Voltage (Note 2)	$V_{DS(ON)}$	$I_D = 2\text{A}, V_{GS} = 5\text{V}$	-	-	2.1	V
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 2\text{A}, V_{GS} = 5\text{V}, (\text{Figures 6, 7})$	-	-	1.050	$\Omega$
Turn-On Delay Time	$t_{d(ON)}$	$I_D = 2\text{A}, V_{DD} = 50\text{V}, R_G = 6.25\Omega, R_L = 25\Omega, V_{GS} = 5\text{V}$ (Figures 10, 11, 12)	-	10	25	ns
Rise Time	$t_r$		-	15	45	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	25	45	ns
Fall Time	$t_f$		-	20	25	ns
Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1.0\text{MHz}$ (Figure 9)	-	-	200	pF
Output Capacitance	$C_{OSS}$		-	-	80	pF
Reverse Transfer Capacitance	$C_{RSS}$		-	-	35	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	5	$^\circ\text{C/W}$

## Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	$V_{SD}$	$I_{SD} = 2\text{A}$	-	-	1.4	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = 2\text{A}, dI_{SD}/dt = 50\text{A}/\mu\text{s}$	-	100	-	ns

### NOTES:

2. Pulse test: pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .
3. Repetitive rating: pulse width limited by maximum junction temperature.

# Typical Performance Curves Unless Otherwise Specified

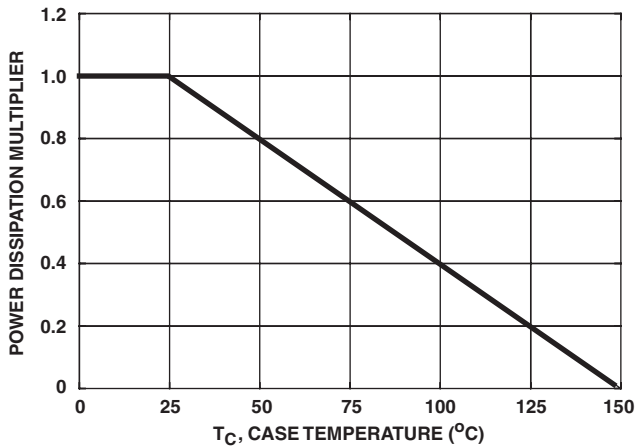


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

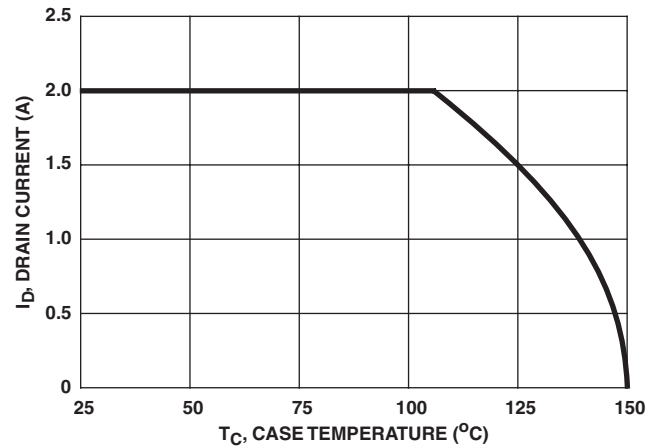


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

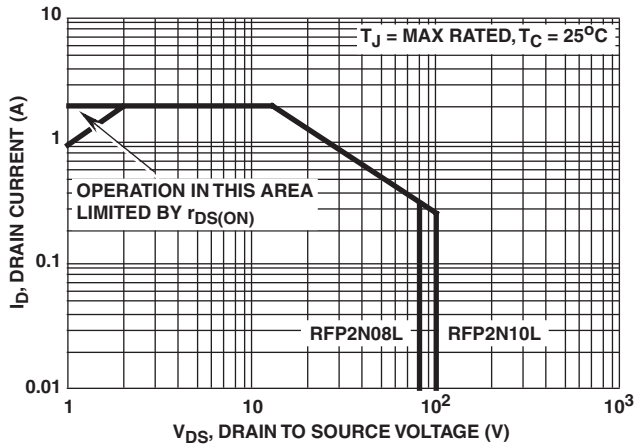


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

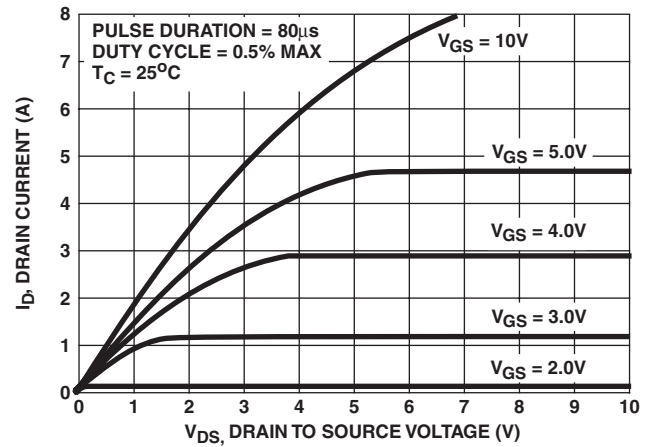


FIGURE 4. SATURATION CHARACTERISTICS

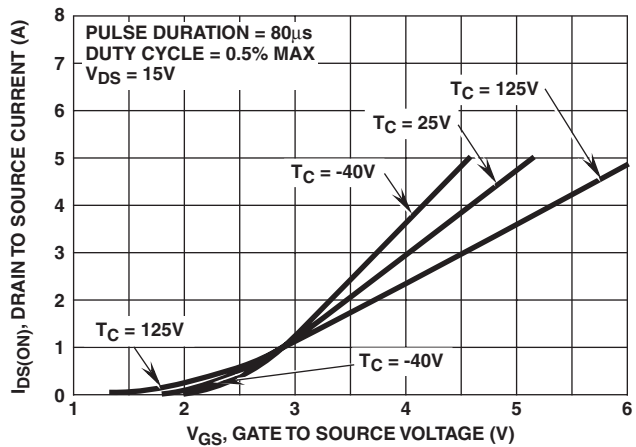


FIGURE 5. TRANSFER CHARACTERISTICS

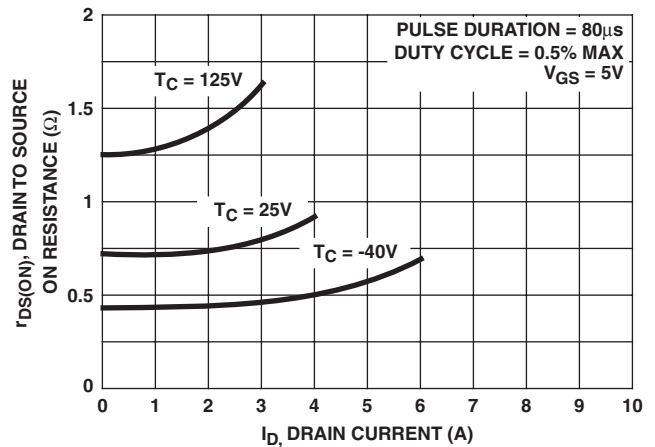


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

## Typical Performance Curves Unless Otherwise Specified (Continued)

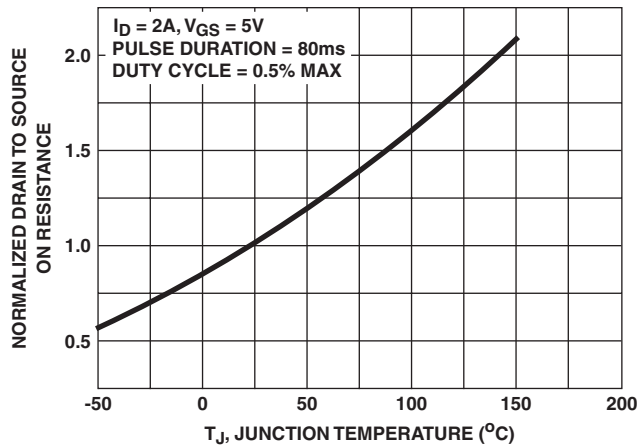


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

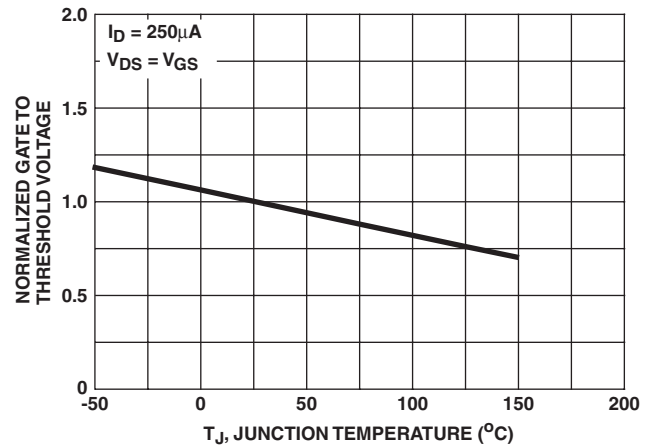


FIGURE 8. NORMALIZED GATE TO THRESHOLD vs JUNCTION TEMPERATURE

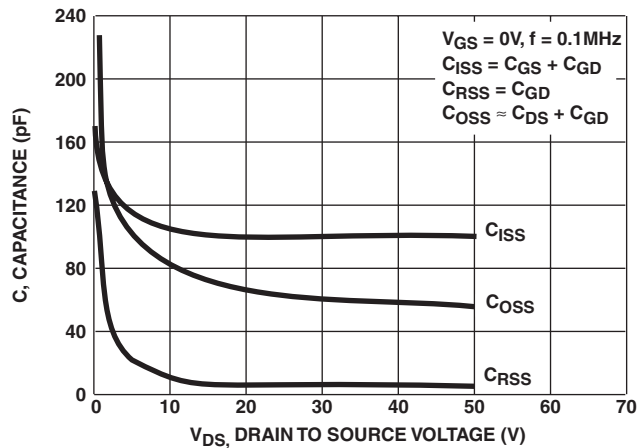
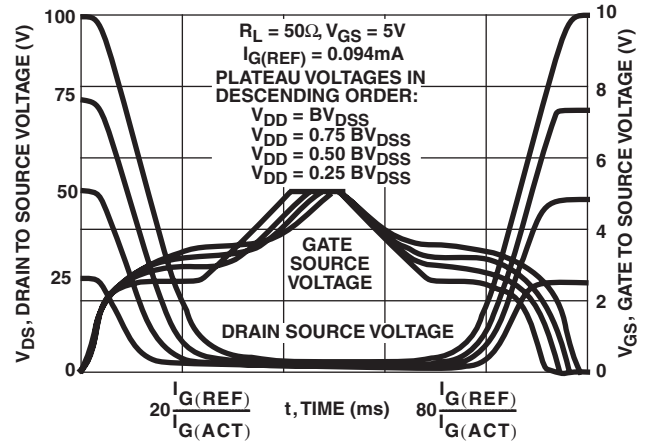


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

## Test Circuit and Waveforms

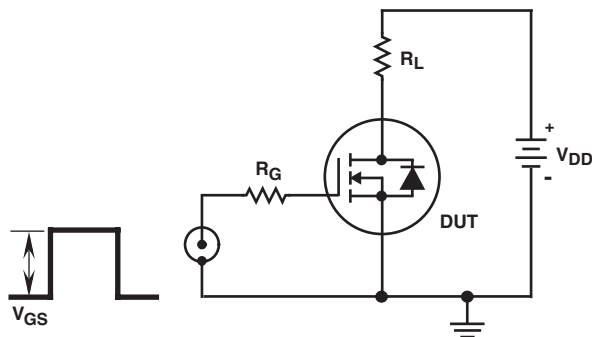


FIGURE 11. SWITCHING TIME TEST CIRCUIT

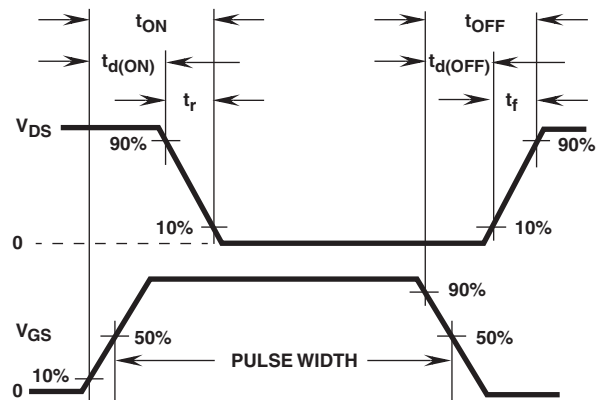


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS

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DenseTrench™	GTO™	Power247™	SuperSOT™-6	
DOMETM	HiSeC™	PowerTrench®	SuperSOT™-8	
EcoSPARK™	ISOPPLANAR™	QFET™	SyncFET™	
E <sup>2</sup> CMOS™	LittleFET™	QST™	TinyLogic™	
EnSigna™	MicroFET™	QT Optoelectronics™	TruTranslation™	
FACT™	MicroPak™	Quiet Series™	UHC™	
FACT Quiet Series™	MICROWIRE™	SILENT SWITCHER®	UltraFET®	

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