FAIRCHILD SEMICONDUCTOR™

February 2000

NM24C04/05 – 4K-Bit Standard 2-Wire Bus Interface Serial EEPROM

General Description

The NM24C04/05 devices are 4096 bits of CMOS non-volatile electrically erasable memory. These devices conform to all specifications in the Standard IIC 2-wire protocol and are designed to minimize device pin count, and simplify PC board layout requirements.

The upper half (upper 2Kbit) of the memory of the NM24C05 can be write protected by connecting the WP pin to V_{CC}. This section of memory then becomes unalterable unless WP is switched to V_{SS}.

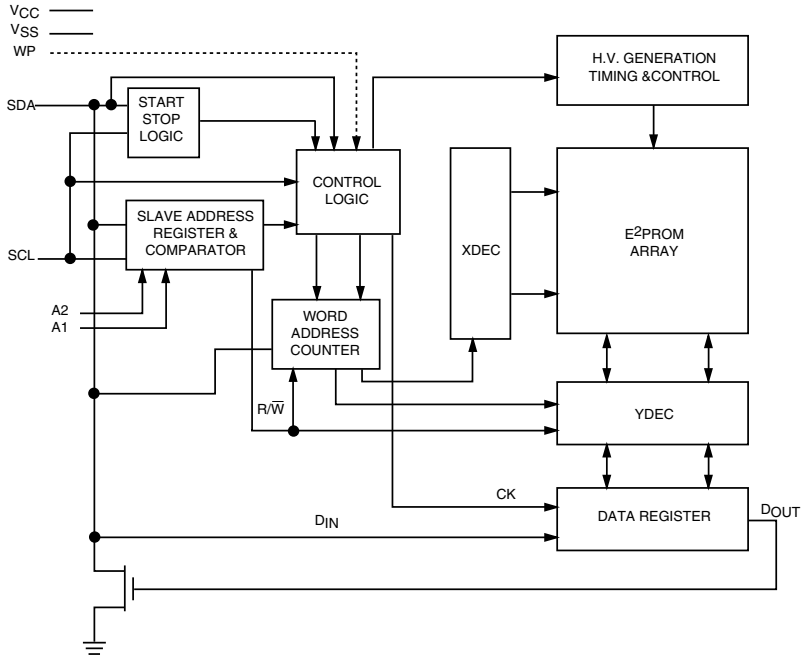
This communications protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s). The Standard IIC protocol allows for a maximum of 16K of EEPROM memory which is supported by the Fairchild family in 2K, 4K, 8K, and 16K devices, allowing the user to configure the memory as the application requires with any combination of EEPROMs. In order to implement higher EEPROM memory densities on the IIC bus, the Extended IIC protocol must be used. (Refer to the NM24C32 or NM24C65 datasheets for more information.)

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption.

Features

- Extended operating voltage 2.7V – 5.5V
- 400 KHz clock frequency (F) at 2.7V - 5.5V
- 200µA active current typical
  - 10µA standby current typical
  - 1µA standby current typical (L)
  - 0.1µA standby current typical (LZ)
- IIC compatible interface
  - – Provides bi-directional data transfer protocol
- Schmitt trigger inputs
- Sixteen byte page write mode
  - – Minimizes total write time per byte
- Self timed write cycle
  - Typical write cycle time of 6ms
- Hardware Write Protect for upper half (NM24C05 only)
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
- Packages available: 8-pin DIP, 8-pin SO, and 8-pin TSSOP
- Available in three temperature ranges
  - - Commercial: 0° to +70°C
  - - Extended (E): -40° to +85C
  - - Automotive (V): -40° to +125°C

Block Diagram



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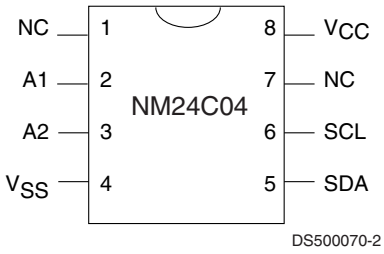
Connection Diagrams

Dual-in-Line Package (N), SO Package (M8) and TSSOP Package (MT8)

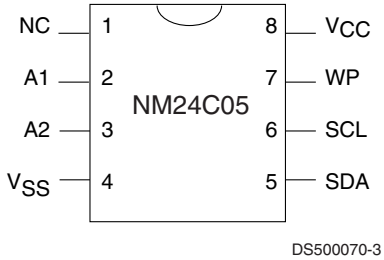


See Package Number N08E, M08A and MTC08

Pin Names

A1,A2	Device Address Inputs
V_{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock Input
NC	No Connection
V_{CC}	Power Supply

Dual-in-Line Package (N), SO Package (M8) and TSSOP Package (MT8)

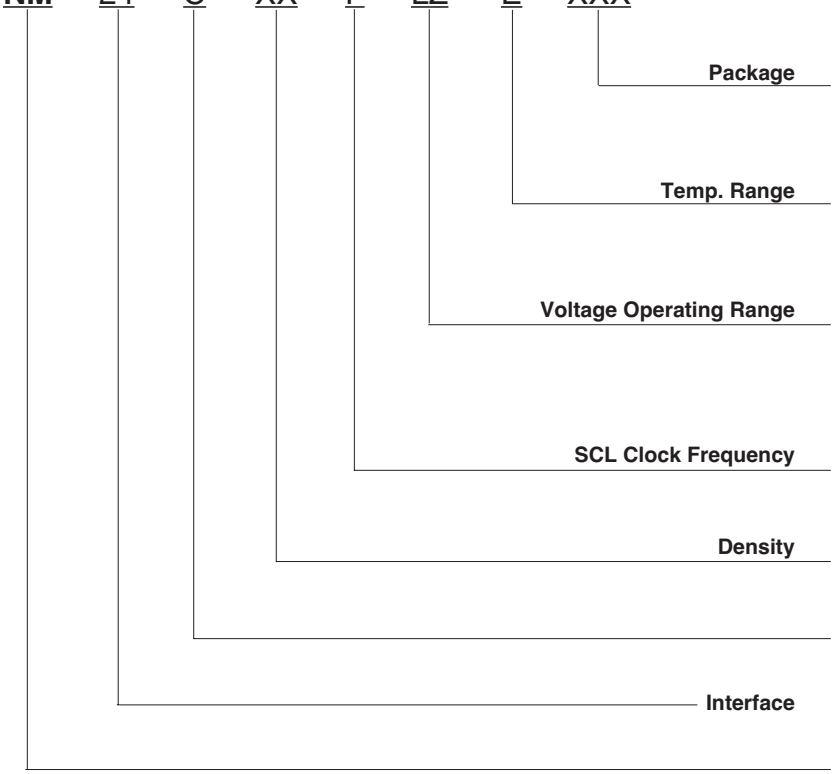


See Package Number N08E, M08A and MTC08

Pin Names

A1,A2	Device Address Inputs
V_{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock input
WP	Write Protect
V_{CC}	Power Supply
NC	No Connection

Ordering Information



	Letter	Description
Package	N	8-pin DIP
	M8	8-pin SOIC
	MT8	8-pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 5.5V
	LZ	2.7V to 5.5V and <1μA Standby Current
SCL Clock Frequency	Blank	100KHz
	F	400KHz
Density	04	4K
	05	4K with Write Protect
	C	CMOS Technology
Interface	24	IIC
	NM	**Fairchild Non-Volatile Memory**

Product Specifications

Absolute Maximum Ratings

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to Ground	6.5V to –0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min.

Operating Conditions

Ambient Operating Temperature	
NM24C04/05	0°C to +70°C
NM24C04E/05E	-40°C to +85°C
NM24C04V/05V	-40°C to +125°C
Positive Power Supply	
NM24C04/05	4.5V to 5.5V
NM24C04L/05L	2.7V to 5.5V
NM24C04LZ/05LZ	2.7V to 5.5V

DC Electrical Characteristics (2.7V to 5.5V)

Symbol	Parameter	Test Conditions		Limits			Units
				Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 400 KHz f_{SCL} = 100 KHz			0.2	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}	V_{CC} = 2.7V - 5.5V V_{CC} = 2.7V - 5.5V (L) V_{CC} = 2.7V - 4.5V (LZ)		10 1 0.1	50 10 1	µA µA µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}			0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			0.1	1	µA
V_{IL}	Input Low Voltage			–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA				0.4	V

Capacitance T_A = +25°C, f = 100/400 KHz, V_{CC} = 5V (Note 2)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

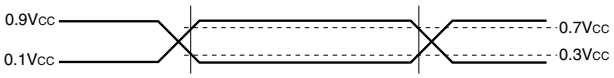
Note 1: Typical values are T_A = 25°C and nominal supply voltage of 5V for 4.5V-5.5V operation and at 3V for 2.7V-4.5V operation.

Note 2: This parameter is periodically sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input & Output Timing Levels	V_{CC} x 0.3 to V_{CC} x 0.7
Output Load	1 TTL Gate and C_L = 100 pF

AC Testing Input/Output Waveforms



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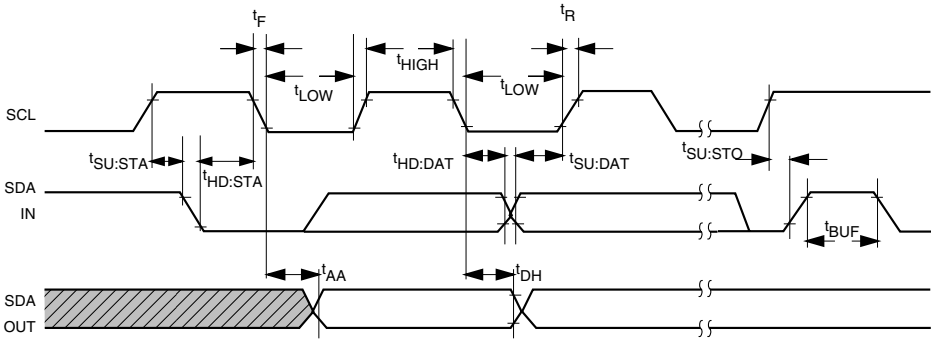
Read and Write Cycle Limits (Standard and Low V_{CC} Range 2.7V - 5.5V)

Symbol	Parameter	100 KHz		400 KHz		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse width)		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	0.9	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.5		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data in Hold Time	20		20		ns
$t_{SU:DAT}$	Data in Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1		0.3	µs
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	300		50		ns
t_{WR} (Note 3)	Write Cycle Time - NM24C04/05 - NM24C04/05L, NM24C04/05LZ		10 15		10 15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM24C04/05 bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address. Refer "Write Cycle Timing" diagram.

Bus Timing



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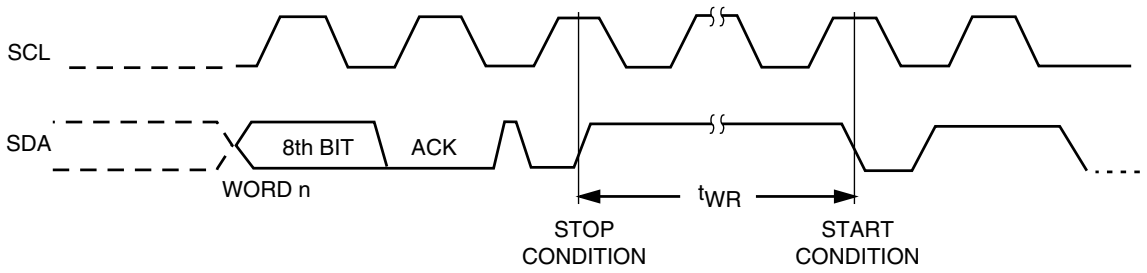
Write Cycle Timing



Note: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle.

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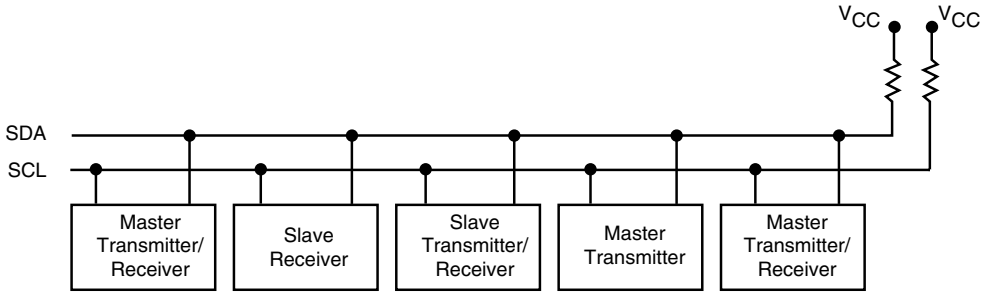
Typical System Configuration



Note: Due to open drain configuration of SDA and SCL, a bus-level pull-up resistor is called for, (typical value = 4.7kΩ)

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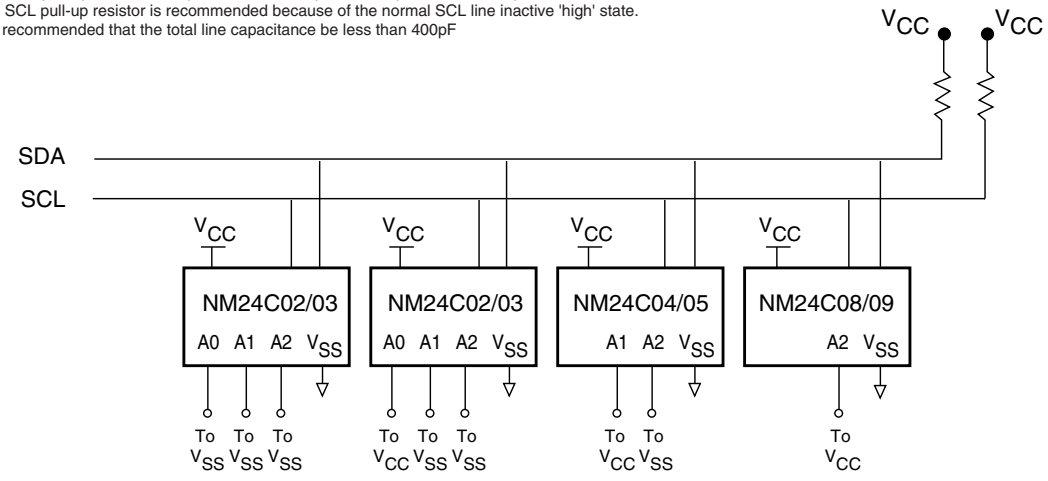
Example of 16K of Memory on 2-Wire Bus

Note: The SDA pull-up resistor is required due to the open-drain/open collector output of IIC bus devices.
The SCL pull-up resistor is recommended because of the normal SCL line inactive 'high' state.
It is recommended that the total line capacitance be less than 400pF



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Device	Address Pins Present			Memory Size	# of Page Blocks
	A0	A1	A2		
NM24C02/03	Yes	Yes	Yes	2048 Bits	1
NM24C04/05	No	Yes	Yes	4096 Bits	2
NM24C08/09	No	No	Yes	8192 Bits	4
NM24C16/17	No	No	No	16,384 Bits	8

Background Information (IIC Bus)

IIC bus allows synchronous bi-directional communication between a TRANSMITTER and a RECEIVER using a Clock signal (SCL) and a Data signal (SDA). Additionally there are up to three Address signals (A2, A1 and A0) which collectively serve as "chip select signal" to a device (example EEPROM) on the IIC bus.

All communication on the IIC bus must be started with a valid START condition (by a MASTER), followed by transmittal (by the MASTER) of byte(s) of information (Address/Data). For every byte of information received, the addressed RECEIVER provides a valid ACKNOWLEDGE pulse to further continue the communication unless the RECEIVER intends to discontinue the communication. Depending on the direction of transfer (Write or Read), the RECEIVER can be a SLAVE or the MASTER. A typical IIC communication concludes with a STOP condition (by the MASTER).

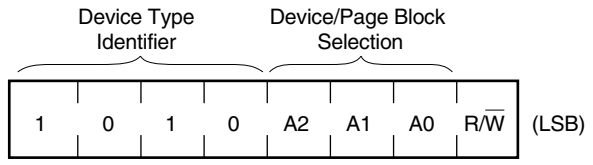
Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]—[DEVICE/PAGE BLOCK SELECTION]—[R/W BIT]—{acknowledge pulse}—[ARRAY ADDRESS]

Slave Address

Slave Address is an 8-bit information consisting of a Device type field (4bits), Device/Page block selection field (3bits) and Read/Write bit (1bit).

Slave Address Format



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Device Type

IIC bus is designed to support a variety of devices such as RAMs, EPROMs etc., along with EEPROMS. Hence to properly identify various devices on the IIC bus, a 4-bit “Device Type” identifier string is used. For EEPROMS, this 4-bit string is 1-0-1-0. Every IIC device on the bus internally compares this 4-bit string to its own “Device Type” string to ensure proper device selection.

Device/Page Block Selection

When multiple devices of the same type (e.g. multiple EEPROMS) are present on the IIC bus, then the A2, A1 and A0 address information bits are also used as part of the Slave Address. Every IIC device on the bus internally compares this 3-bit string to its own physical configuration (A2, A1 and A0 pins) to ensure proper device selection. This comparison is in addition to the “Device Type” comparison. In addition to selecting an EEPROM, these 3 bits are also used to select a “page block” within the selected EEPROM. Each page block is 2Kbit (256Bytes) in size. Depending on the density, an EEPROM can contain from a minimum of 1 to a maximum of 8 page blocks (in multiples of 2) and selection of a page block within a device is by using A2, A1 and A0 bits.

Read/Write Bit

Last bit of the Slave Address indicates if the intended access is Read or Write. If the bit is "1," then the access is Read, whereas if the bit is "0," then the access is Write.

Acknowledge

Acknowledge is an active LOW pulse on the SDA line driven by an addressed receiver to the addressing transmitter to indicate receipt of 8-bits of data. The receiver provides an ACK pulse for every 8-bits of data received. This handshake mechanism is done as follows: After transmitting 8-bits of data, the transmitter releases the SDA line and waits for the ACK pulse. The addressed receiver, if present, drives the ACK pulse on the SDA line during the 9th clock and releases the SDA line back (to the transmitter). Refer *Figure 3*.

Array Address

Array address is an 8-bit information containing the address of a memory location to be selected within a page block of the device.

16K bit Addressing Limitation:

Standard IIC specification limits the maximum size of EEPROM memory on the bus to 16K bits. This limitation is due to the addressing protocol implemented which consists of the 8-bit Slave Address and an additional 8-bit field called Array Address. This Array Address selects 1 out of 256 locations (2^8=256). Since the data format of IIC specification is 8-bit wide, a total of 256 x 8 = 2048 = 2K bit now becomes addressable by this 8-bit Array Address. This 2K bit is typically referred as a “Page Block”. Combining this 8-bit Array Address with the 3-bit Device/Page address (part of Slave Address) allows a maximum of 8 pages (2^3=8) of memory that can be addressed. Since each page is 2K bit in size, 8 x 2K bit = 16K bit is the maximum size of memory that is addressable on the Standard IIC bus. This 16Kb of memory can be in the form of a single 16Kb EEPROM device or multiple EEPROMs of varying density (in 2Kb multiples) to a maximum total of 16Kb. To address the needs of systems that require more than 16Kb on the IIC bus, a different specification called “Extended IIC Specification” is used. Please refer to NM24C32xx Datasheet for more information on Extended IIC Specification.

DEFINITIONS	
WORD	8 bits (byte) of data
PAGE	16 sequential byte locations starting at a 16-byte address boundary, that may be programmed during a "page write" programming cycle
PAGE BLOCK	2048 (2K) bits organized into 16 pages of addressable memory. (8 bits) x (16 bytes) x (16 pages) = 2048 bits
MASTER	Any IIC device CONTROLLING the transfer of data (such as a microprocessor)
SLAVE	Device being controlled (EEPROMs are always considered Slaves)
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master or Slave).
RECEIVER	Device currently RECEIVING data on the bus (Master or Slave)

Pin Descriptions

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bi-directional pin used to transfer data into and out of the device. It is an open drain output and may be wire–ORed with any number of open drain or open collector outputs.

Write Protect (WP) (NM24C05 Only)

If tied to V_{CC}, PROGRAM operations onto the upper half (upper 2Kbit) of the memory will not be executed. READ operations are possible. If tied to V_{SS}, normal operation is enabled, READ/WRITE over the entire memory is possible.

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

This pin has an internal pull-down circuit. However, on systems where write protection is not required it is recommended that this pin is tied to V_{SS}.

Device Selection Inputs A2, A1 and A0 (as appropriate)

These inputs collectively serve as "chip select" signal to an EEPROM when multiple EEPROMs are present on the same IIC bus. Hence these inputs, if present, should be connected to V_{CC} or V_{SS} in a unique manner to allow proper selection of an EEPROM amongst multiple EEPROMs. During a typical addressing sequence, every EEPROM on the IIC bus compares the configuration of these inputs to the respective 3 bit "Device/Page block selection" information (part of slave address) to determine a valid selection. For e.g. if the 3 bit "Device/Page block selection" is 1-0-1, then the EEPROM whose "Device Selection inputs" (A2, A1 and A0) are connected to V_{CC}-V_{SS}-V_{CC} respectively, is selected.

Depending on the density, only appropriate number of "Device Selection inputs" are provided on an EEPROM. For every "Device selection input" that is not present on the device, the corresponding bit in the "Device/Page block selection" field is used to select a "Page Block" within the device instead of the device itself. Following table illustrates the above:

EEPROM Density	Number of Page Blocks	Device Selection Inputs Provided			Address Bits Selecting Page Block
2k bit	1	A0	A1	A2	None
4k bit	2	—	A1	A2	A0
8k bit	4	—	—	A2	A0 and A1
16k bit	8	—	—	—	A0, A1 and A2

Note that even when just one EEPROM present on the IIC bus, these pins should be tied to V_{CC} or V_{SS} to ensure proper termination.

Device Operation

The NM24C04/05 supports a bi-directional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24C04/05 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figure 1* and *Figure 2* on next page.

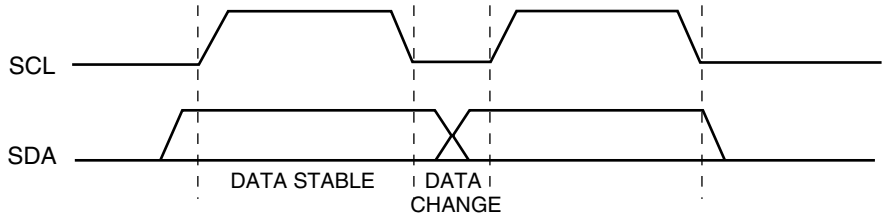
Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24C04/05 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Stop Condition

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24C04/05 to place the device in the standby power mode, except when a Write operation is being executed, in which case a second stop condition is required after t_{WR} period, to place the device in standby mode.

Data Validity (Figure 1)



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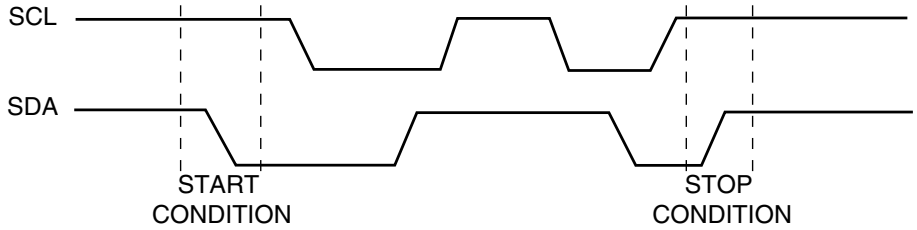
Start and Stop Definition (Figure 2)



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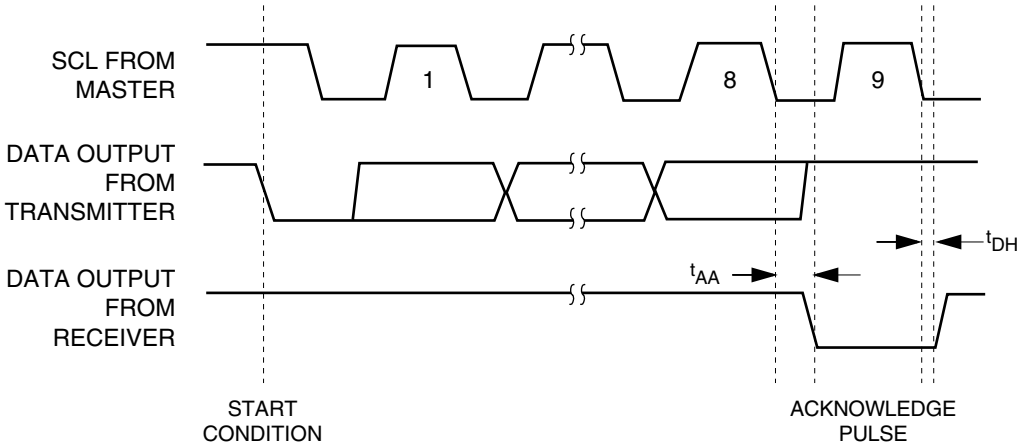
Acknowledge Response from Receiver (Figure 3)



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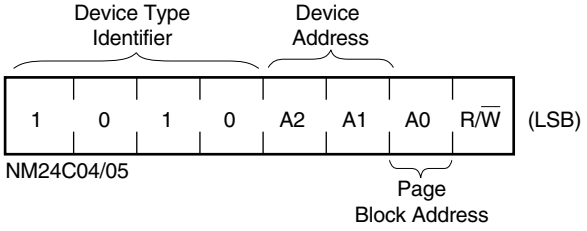
Acknowledge

The NM24C04/05 device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24C04/05 will respond with an acknowledge after the receipt of each subsequent eight bit byte.

In the read mode the NM24C04/05 slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected, NM24C04/05 will continue to transmit data. If an acknowledge is not detected,NM24C04/05 will terminate further data transmissions and await the stop condition to return to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier. This is fixed as 1010 for all EEPROM devices.



Refer the following table for Slave Addresses string details:

Device	A0	A1	A2	Page Blocks	Page Block Addresses
NM24C04/05	P	A	A	2	0, 1

A: Refers to a hardware configured Device Address pin.

P: Refers to an internal PAGE BLOCK.

All IIC EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Word addresses 0x00 through 0xFF). Therefore, address bits A0, A1, or A2 (if designated 'P') are used to access a PAGE BLOCK in conjunction with the Word address used to access any individual data byte.

The last bit of the slave address defines whether a write or read condition is requested by the master. A '1' indicates that a read operation is to be executed, and a '0' initiates the write mode.

A simple review: After the NM24C04/05 recognizes the start condition, the devices interfaced to the IIC bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a write operation a second address field is required which is a word address that is comprised of eight bits and provides access to any one of the 256 bytes in the selected page of memory. Upon receipt of the byte address the NM24C04/05 responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24C04/05 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24C04/05 inputs are disabled, and the device will not respond to any requests from the master for the duration of t_{WR}. Refer to *Figure 4* for the address, acknowledge and data transfer sequence.

PAGE WRITE

To minimize write cycle time, NM24C04/05 offer Page Write feature, by which, up to a maximum of 16 contiguous bytes locations can be programmed all at once (instead of 16 individual byte writes). To facilitate this feature, the memory array is organized in terms of "Pages." A Page consists of 16 contiguous byte locations starting at every 16-Byte address boundary (for example, starting at array address 0x00, 0x10, 0x20 etc.). Page Write operation limits access to byte locations within a page. In other words a single Page Write operation will not cross over to locations on another page but will "roll over" to the beginning of the page whenever end of Page is reached and additional locations are a continued to be accessed. A Page Write operation can be initiated to begin at any location within a page (starting address of the Page Write operation need not be the starting address of a Page).

Page Write is initiated in the same manner as the Byte Write operation; but instead of terminating the cycle after transmitting the first data byte, the master can further transmit up to 15 more bytes. After the receipt of each byte, NM24C04/05 will respond with an acknowledge pulse, increment the internal address counter to the next address and is ready to accept the next data. If the master should transmit more than sixteen bytes prior to generating the STOP condition, the address counter will "roll over" and previously written data will be overwritten. As with the Byte Write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.

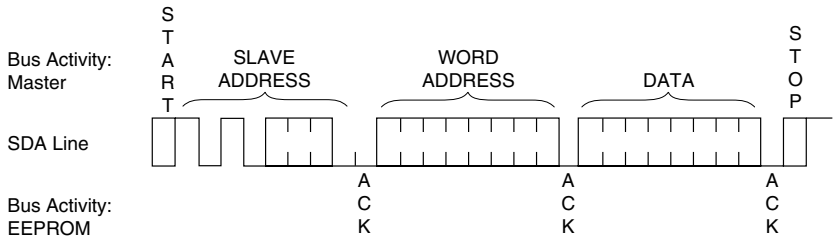
Acknowledge Polling

Once the stop condition is issued to indicate the end of the host's write operation the NM24C04/05 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24C04/05 is still busy with the write operation no ACK will be returned. If the NM24C04/05 has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

Write Protection (NM24C05 Only)

Programming of the upper half (upper 2Kbit) of the memory will not take place if the WP pin of the NM24C05 is connected to V_{CC}. The NM24C05 will respond to slave and byte addresses; but if the memory accessed is write protected by the WP pin, the NM24C05 will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

Byte Write (Figure 4)



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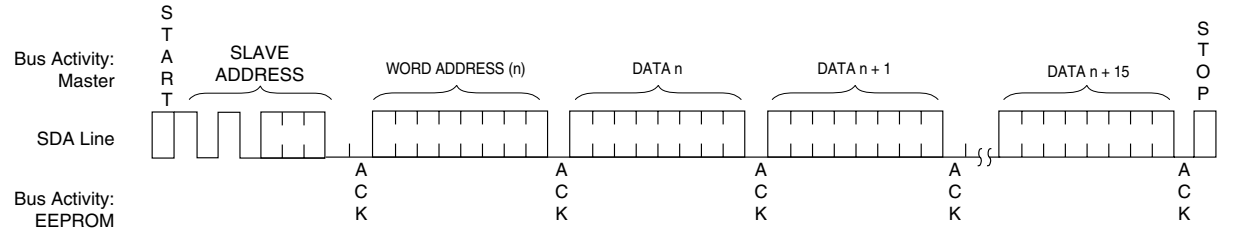
Page Write (Figure 5)



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Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

Internally the NM24C04/05 contains an address counter that maintains the address of the last byte accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24C04/05 issues an acknowledge and transmits the eight bit byte. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM24C04/05 discontinues transmission. Refer to *Figure* 6 for the sequence of address, acknowledge and data transfer.

Random Read

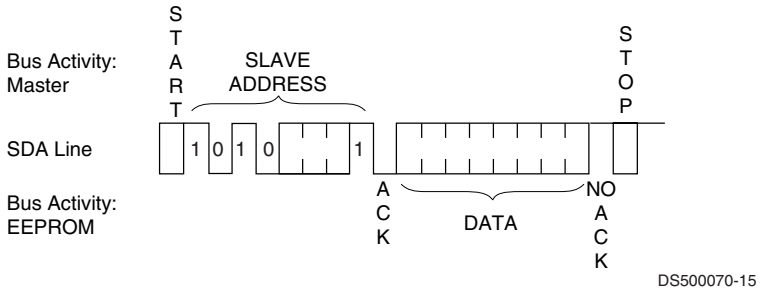
Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, slave address with the R/$\overline{W}$ bit set to zero and then the byte address it is to read. After the byte address acknowledge, the master immediately issues another start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM24C04/05 and then by the eight bit byte. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24C04/05 discontinues transmission. Refer to *Figure 7* for the address, acknowledge and data transfer sequence.

Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24C04/05 continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" to the beginning of the memory. NM24C04/05 continues to output data for each acknowledge received. Refer to *Figure 8* for the address, acknowledge, and data transfer sequence.

Current Address Read (Figure 6)



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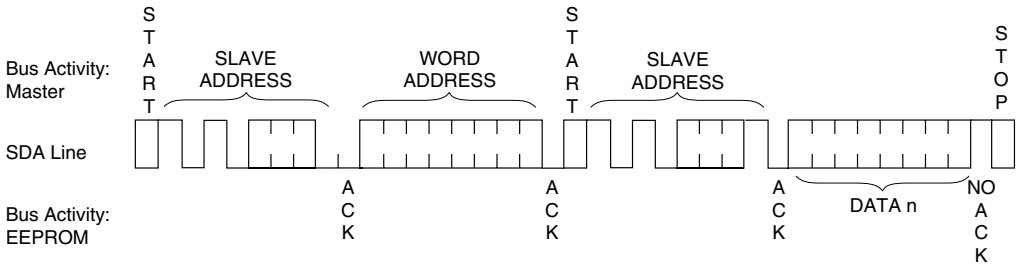
Random Read (Figure 7)



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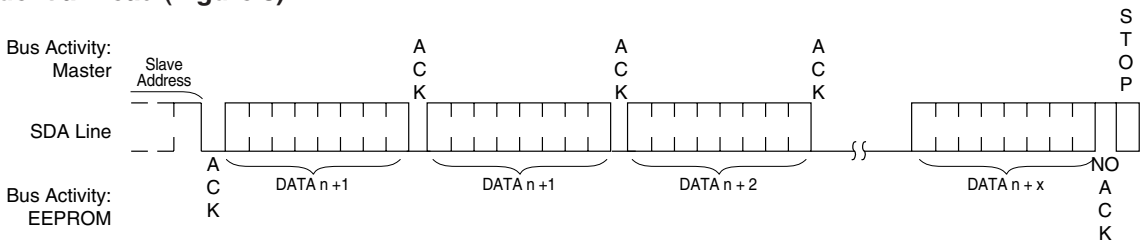
Sequential Read (Figure 8)



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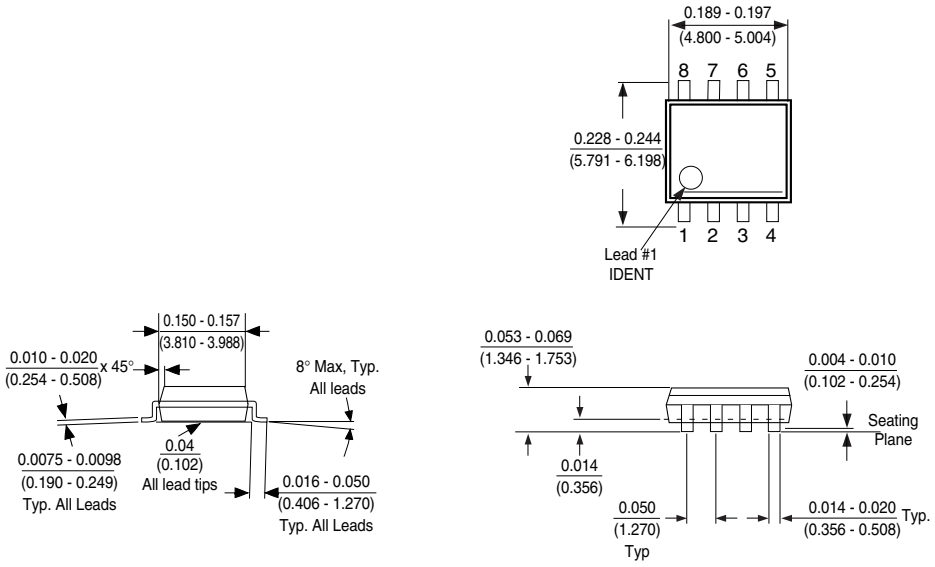
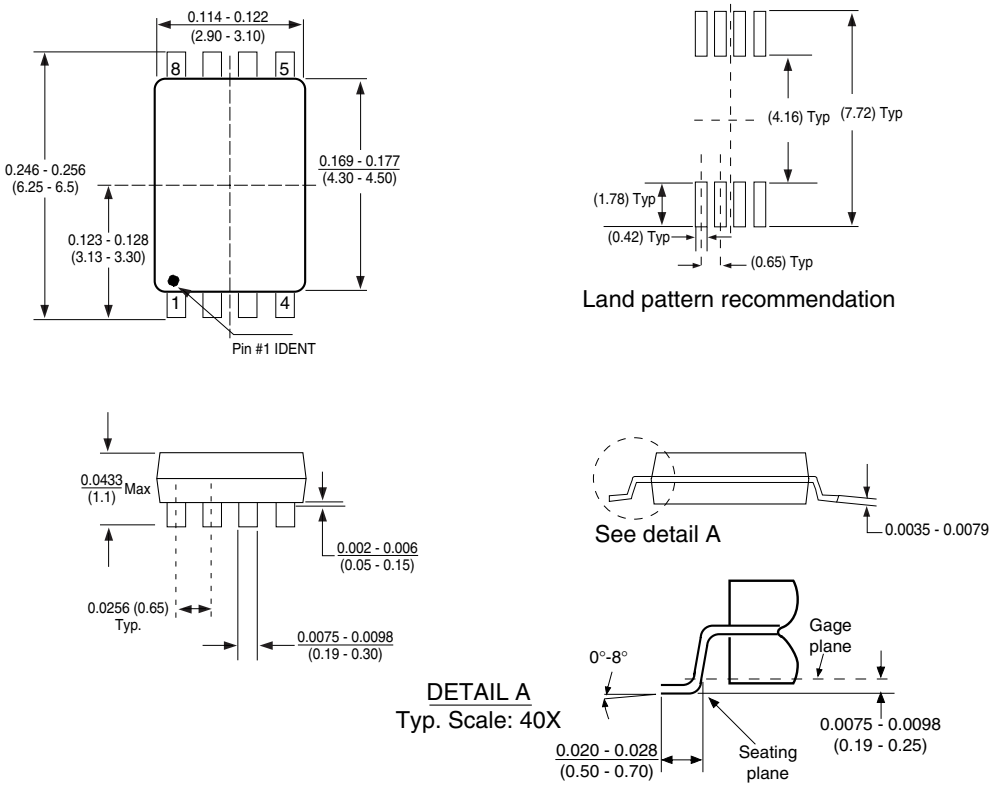
Physical Dimensions inches (millimeters) unless otherwise noted



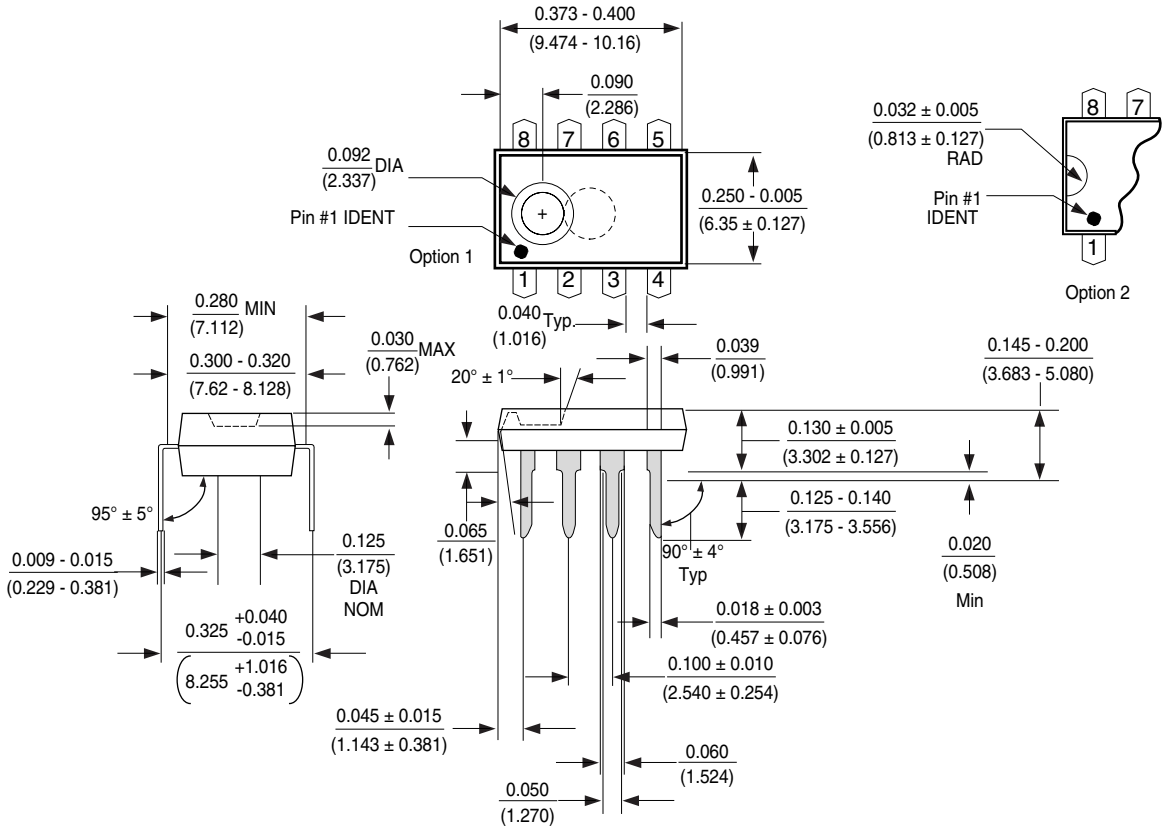
8-Pin Molded Small Outline Package (M8)
Package Number M08A



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded Thin Shrink Small Outline Package (MT8)
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

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