

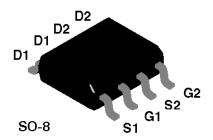
NDS9957 Dual N-Channel Enhancement Mode Field Effect Transistor

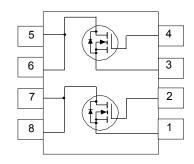
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 2.6A, 60V. $R_{DS(ON)} = 0.16\Omega$ @ $V_{GS} = 10V$.
- High density cell design for extremely low R_{DS(ON)}.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.





Absolute Maximum Ratings T_a = 25°C unless otherwise noted

Symbol	Parameter		NDS9957	Units
V _{DSS}	Drain-Source Voltage		60	V
V _{GSS}	Gate-Source Voltage		± 20	V
I _D	Drain Current - Continuous	(Note 1a)	± 2.6	A
	- Pulsed		± 10	
)	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T_{J}, T_{STG}	Operating and Storage Temperature Range	е	-55 to 150	°C
THERMA	L CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
R _{øJC}	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Symbol	Parameter	Conditions		Min	Тур	Max	Units
OFF CHA	RACTERISTICS	<u>. </u>		•			•
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$		60			V
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}$				1	μΑ
I _{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$				100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	$V_{gs} = -20 \text{ V}, V_{DS} = 0 \text{ V}$				-100	nA
ON CHAR	ACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$		1	1.5	3	V
			T _A = 125°C	0.7	1.1	2.2	
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{gs} = 10 \text{ V}, I_{D} = 2.6 \text{ A}$	<u> </u>		0.145	0.16	Ω
			T _A = 125°C		0.25	0.3	
		$V_{gs} = 4.5 \text{ V}, I_{D} = 2.1 \text{ A}$			0.19	0.25	
			T _A = 125°C		0.32	0.5	
I _{D(on)}	On-State Drain Current	$V_{GS} = 10 \text{ V}, V_{DS} = 5 \text{ V}$	10			Α	
g _{FS}	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_{D} = 2.6 \text{ A}$		4		S	
DYNAMIC	CHARACTERISTICS	T				•	
C _{iss}	Input Capacitance	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0 MHz		200		pF	
C _{oss}	Output Capacitance	T = 1.0 MHZ			60		pF
C _{rss}	Reverse Transfer Capacitance				20		pF
SWITCHIN	NG CHARACTERISTICS (Note 2)			1	,	•	1
t _{D(on)}	Tum - On Delay Time	$V_{DD} = 30 \text{ V}, I_{D} = 1 \text{ A},$			6	20	ns
ţ,	Turn - On Rise Time	V_{GS} = 10 V, R_{GEN} = 6 Ω		11	25	ns	
t _{D(off)}	Turn - Off Delay Time			17	30	ns	
t _r	Turn - Off Fall Time				4	15	ns
Q_g	Total Gate Charge	$V_{DS} = 30 \text{ V},$			7.5	12	nC
Q_{gs}	Gate-Source Charge	$I_D = 2.6 \text{ A}, V_{GS} = 10 \text{ V}$		2.8		nC	
Q_{gd}	Gate-Drain Charge			8.0		nC	

Electrical Characteristics (T _A = 25°C unless otherwise noted)									
Symbol	Parameter Conditions Min Typ Max Units								
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS									
Is	Maximum Continuos Drain-Source Diode Forward Current 1.7 A								
V _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 2.6 \text{ A} \text{ (Note 2)}$		0.9	1.2	V			

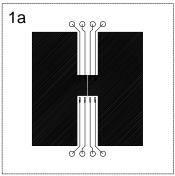
Notes:

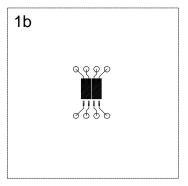
1. $R_{g,A}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{g,C}$ is guaranteed by design while R_{gCA} is determined by the user's board design.

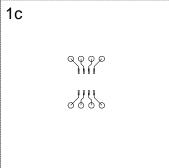
$$P_D(t) = \frac{T_J - T_A}{R_{\theta J} \, \hat{A}^{(t)}} = \frac{T_J - T_A}{R_{\theta J} \, \hat{c}^t R_{\theta C} \hat{A}^{(t)}} = I_D^2(t) \times R_{DS(ON) \cdot \P T_J}$$

Typical R_{BJA} for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- a. 78°C/W when mounted on a 0.5 in² pad of 2oz cpper.
- b. 125°C/W when mounted on a 0.02 in² pad of 2oz cpper.
- c. 135°C/W when mounted on a 0.003 in² pad of 2oz cpper.







Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%.

Typical Electrical Characteristics

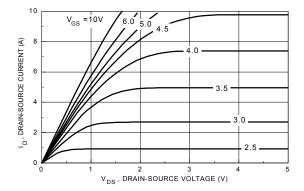


Figure 1. On-Region Characteristics.

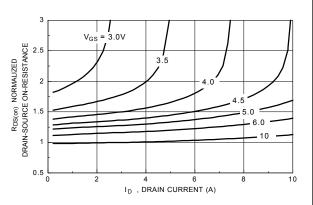


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

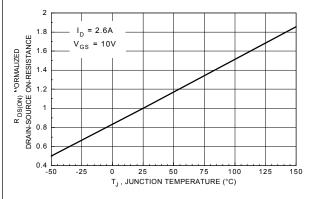


Figure 3. On-Resistance Variation with Temperature.

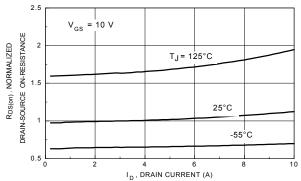


Figure 4. On-Resistance Variation with Drain Current and Temperature.

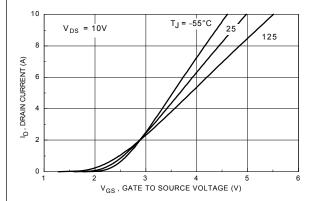


Figure 5. Transfer Characteristics.

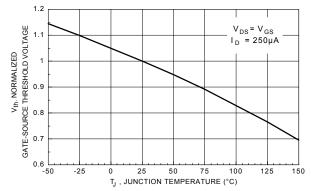


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

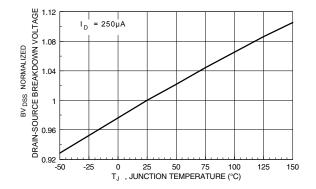


Figure 7. Breakdown Voltage Variation with Temperature.

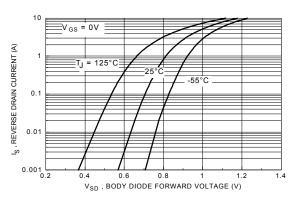


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

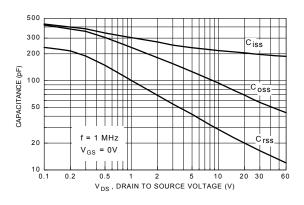


Figure 9. Capacitance Characteristics.

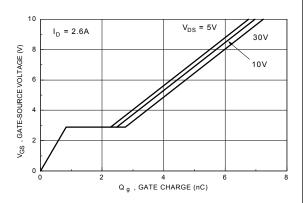


Figure 10. Gate Charge Characteristics.

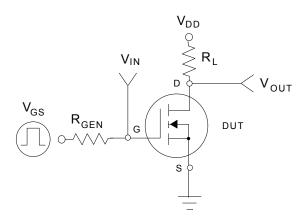


Figure 11. Switching Test Circuit

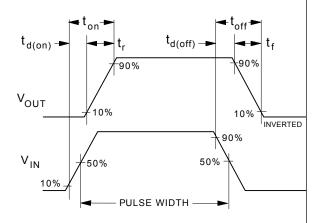
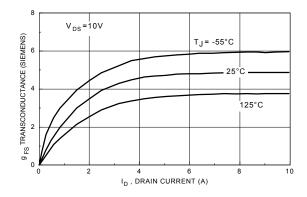


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)



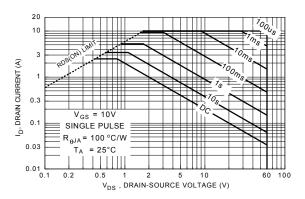


Figure 13. Transconductance Variation with Drain Current and Temperature.

Figure 14. Maximum Safe Operating Area.

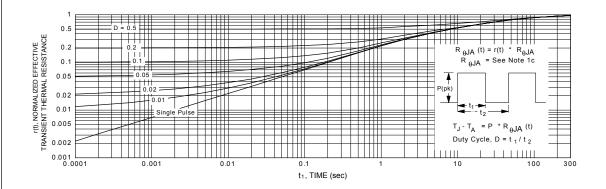
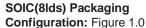


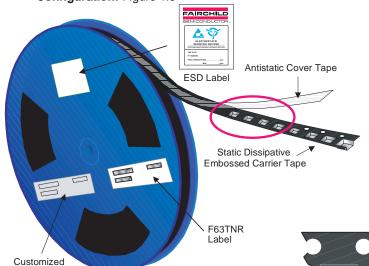
Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

SO-8 Tape and Reel Data and Package Dimensions







Packaging Description:

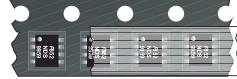
Packaging Description:

SOIC-8 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and amit-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13° or 300cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (antistatic coated). Other option comes in 500 units per 7° or 177cm diameter reel. This and some other options are further described in the Packaging Information table.

These full reles are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.

ESD Label

F63TN Label

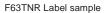




SOIC-8 Unit Orientation

343mm x 342mm x 64mm Standard Intermediate box

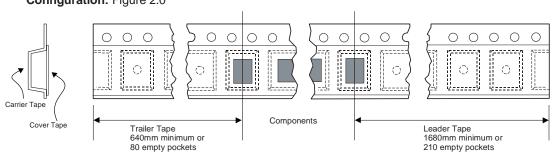
SOIC (8lds) Packaging Information Packaging Option Standard o flow code) L86Z D84Z Rail/Tube TNR Packaging type TNR TNR Qty per Reel/Tube/Bag 2.500 4.000 500 Reel Size 13" Dia 13" Dia 7" Dia Box Dimension (mm) 343y64y343 530x130x83 343y64y343 184v187v47 Max qty per Box 5,000 30,000 8,000 1,000 Weight per unit (gm) 0.0774 0.0774 0.0774 0.0774 Weight per Reel (kg) 0.6060 0.9696 0.1182 Note/Comments



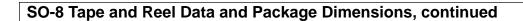
Label



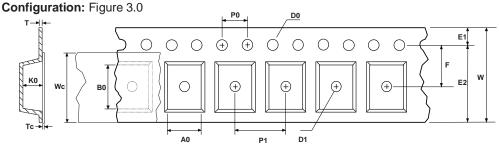
SOIC(8Ids) Tape Leader and Trailer Configuration: Figure 2.0



F63TNL



SOIC(8lds) Embossed Carrier Tape





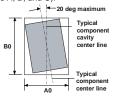
	Dimensions are in millimeter													
Pkg type	A0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	т	Wc	Тс
SOIC(8lds) (12mm)	6.50 +/-0.10	5.30 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	2.1 +/-0.10	0.450 +/- 0.150	9.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



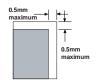
Sketch A (Side or Front Sectional View)
Component Rotation

13" Diameter Option



Sketch B (Top View)

Component Rotation



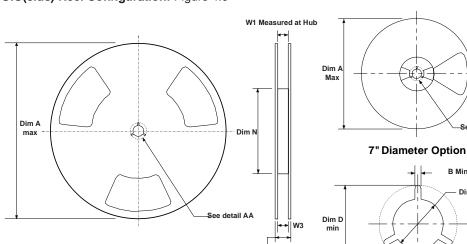
Sketch C (Top View)

Component lateral movement

Dim C

DETAIL AA

SOIC(8lds) Reel Configuration: Figure 4.0

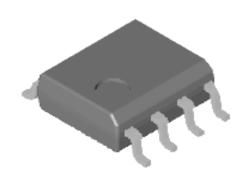


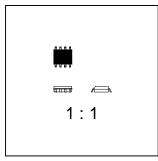
Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4

W2 max Measured at Hub

SO-8 Tape and Reel Data and Package Dimensions, continued

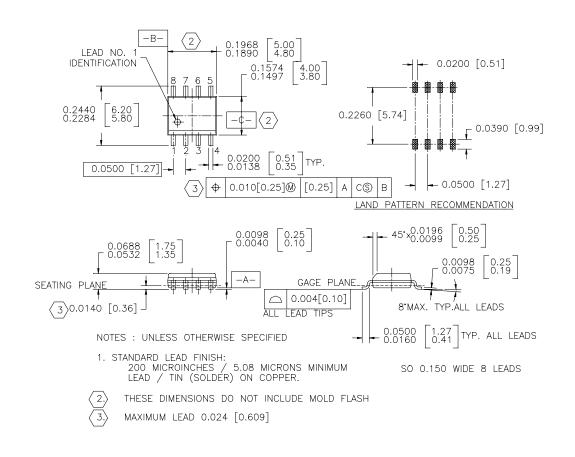
SOIC-8 (FS PKG Code S1)





Scale 1:1 on letter size paper
Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0774



TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

FACT™ QFET™ FACT Quiet Series™ QS™

FAST[®] Quiet Series[™] SuperSOT[™]-3 GTO[™] SuperSOT[™]-6

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition					
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.					
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.					
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.					
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.					