

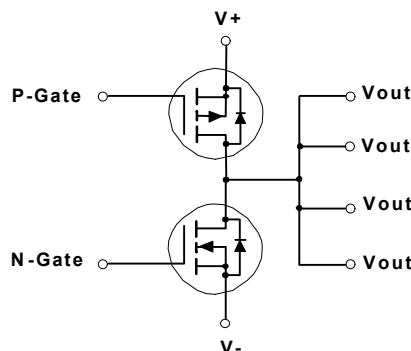
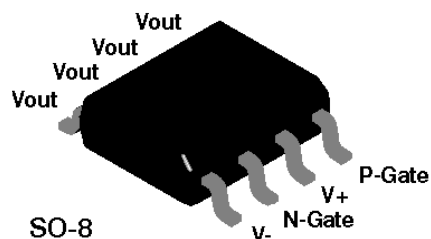
NDS8852H Complementary MOSFET Half Bridge

General Description

These Complementary MOSFET half bridge devices are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage half bridge applications or CMOS applications when both gates are connected together.

Features

- N-Channel 4.3A, 30V, $R_{DS(ON)} = 0.08\Omega$ @ $V_{GS} = 10V$.
P-Channel -3.4A, -30V, $R_{DS(ON)} = 0.13\Omega$ @ $V_{GS} = -10V$.
- High density cell design or extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Matched pair for equal input capacitance and power capability.



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
V _{DSS}	Drain-Source Voltage	30	-30	V
V _{GSS}	Gate-Source Voltage	20	-20	V
I _D	Drain Current - Continuous (Note 1a & 2)	4.3	-3.4	A
	- Pulsed	15	-10	
P _D	Maximum Power Dissipation (Note 1a)	2.5		W
	(Single Device) (Note 1b)	1.2		
	(Note 1c)	1		
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to 150		°C

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Single Device) (Note 1a)	50	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Single Device) (Note 1)	25	$^\circ\text{C/W}$

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	N-Ch	30			V
		V _{GS} = 0 V, I _D = -250 μA	P-Ch	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V T _J = 55°C	N-Ch			2	μA
						25	μA
		V _{DS} = -24 V, V _{GS} = 0 V T _J = 55°C	P-Ch			-2	μA
						-25	μA
I _{GSSF}	Gate - Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V	All			100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	V _{GS} = -20 V, V _{DS} = 0 V	All			-100	nA
ON CHARACTERISTICS (Note 3)							
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA T _J = 125°C	N-Ch	1	1.7	2.8	V
				0.7	1.2	2.2	
		V _{DS} = V _{GS} , I _D = -250 μA T _J = 125°C	P-Ch	-1	-1.6	-2.8	
				-0.85	-1.25	-2.5	
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 3.4 A T _J = 125°C	N-Ch		0.06	0.08	Ω
					0.08	0.13	
					0.08	0.11	
		V _{GS} = 4.5 V, I _D = 2.8 A V _{GS} = -10 V, I _D = -3.4 A T _J = 125°C V _{GS} = -4.5 V, I _D = -2.8 A	P-Ch		0.11	0.13	
					0.15	0.21	
					0.17	0.2	
I _{D(on)}	On-State Drain Current	V _{GS} = 10 V, V _{DS} = 5 V	N-Ch	10			A
		V _{GS} = -10 V, V _{DS} = -5 V	P-Ch	-10			
g _{FS}	Forward Transconductance	V _{DS} = 15 V, I _D = 3.4 A	N-Ch		6		S
		V _{DS} = -15 V, I _D = -3.4 A	P-Ch		4		
DYNAMIC CHARACTERISTICS							
C _{iss}	Input Capacitance	N-Channel V _{DS} = 15 V, V _{GS} = 0 V, f = 1.0 MHz	N-Ch		300		pF
			P-Ch		330		
C _{oss}	Output Capacitance		N-Ch		190		pF
			P-Ch		190		
C _{rss}	Reverse Transfer Capacitance	P-Channel V _{DS} = -15 V, V _{GS} = 0 V, f = 1.0 MHz	N-Ch		70		pF
			P-Ch		70		

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 3)							
t _{D(on)}	Turn - On Delay Time	N-Channel V _{DD} = 10 V, I _D = 1 A, V _{GEN} = 10 V, R _{GEN} = 6 Ω	N-Ch		10	15	ns
			P-Ch		9	40	
t _r	Turn - On Rise Time	P-Channel V _{DD} = -10 V, I _D = -1 A, V _{GEN} = -10 V, R _{GEN} = 6 Ω	N-Ch		13	20	ns
			P-Ch		21	40	
t _{D(off)}	Turn - Off Delay Time		N-Ch		21	50	ns
			P-Ch		21	90	
t _f	Turn - Off Fall Time		N-Ch		5	50	ns
			P-Ch		8	50	
Q _g	Total Gate Charge	N-Channel V _{DS} = 10 V, I _D = 3.4 A, V _{GS} = 10 V	N-Ch		9.5	27	nC
			P-Ch		10	25	
Q _{gs}	Gate-Source Charge	P-Channel V _{DS} = -10 V, I _D = -3.4 A, V _{GS} = -10 V	N-Ch		1.5		
			P-Ch		1.6		
Q _{gd}	Gate-Drain Charge		N-Ch		2.6		
			P-Ch		2.7		

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain-Source Diode Forward Current	N-Ch			2.1	A
			P-Ch		-2.1	
V _{SD}	Drain-Source Diode Forward Voltage	N-Ch		0.8	1.2	V
			P-Ch	-0.8	-1.2	
t _{rr}	Reverse Recovery Time	N-Ch			100	ns
			P-Ch		100	

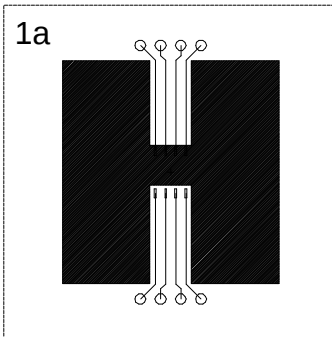
Notes:

- R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.

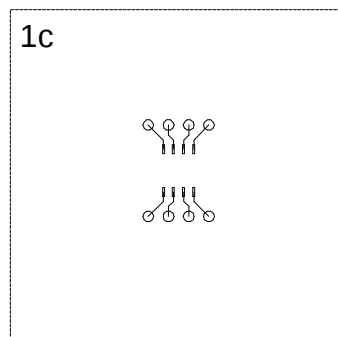
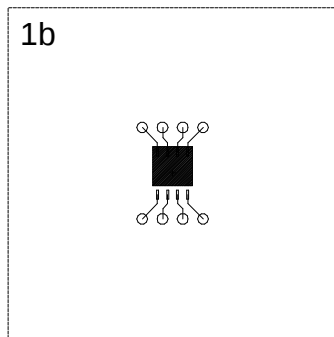
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(on)} \theta_{TJ}$$

Typical R_{θJA} using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- 50°C/W when mounted on a 1 in² pad of 2oz copper.
- 105°C/W when mounted on a 0.04 in² pad of 2oz copper.
- 125°C/W when mounted on a 0.006 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper



- Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

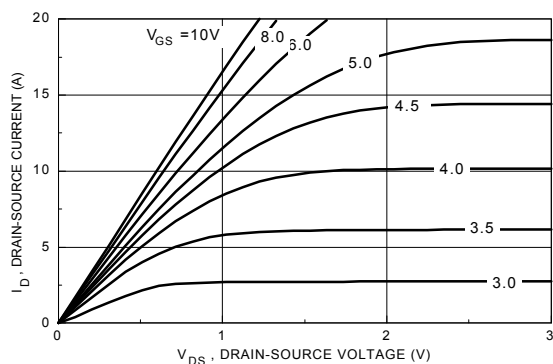


Figure 1. N-Channel On-Region Characteristics.

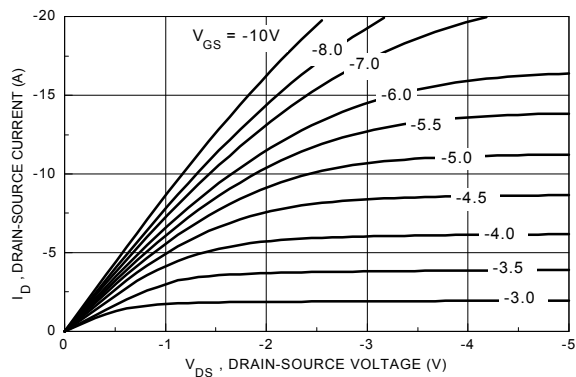


Figure 2. P-Channel On-Region Characteristics.

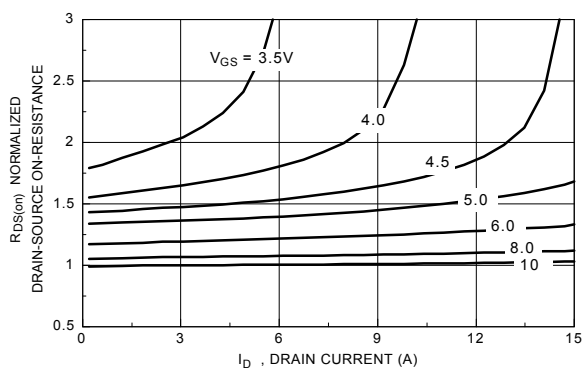


Figure 3. N-Channel On-Resistance Variation with Gate Voltage and Drain Current.

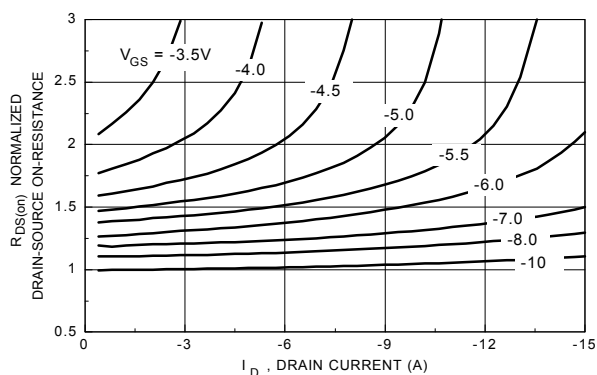


Figure 4. P-Channel On-Resistance Variation with Gate Voltage and Drain Current.

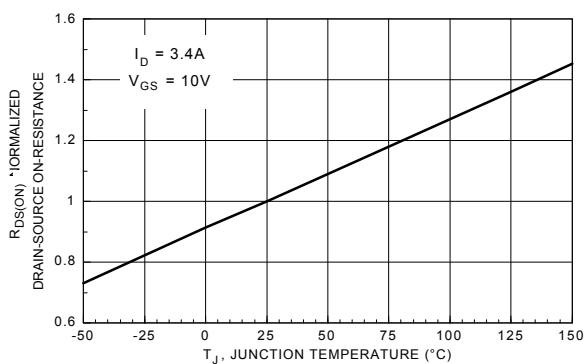


Figure 5. N-Channel On-Resistance Variation with Temperature.

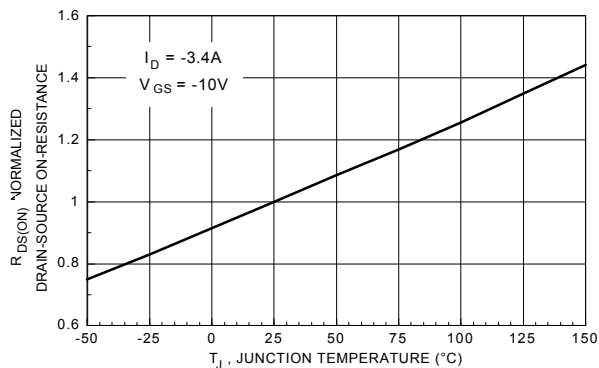


Figure 6. P-Channel On-Resistance Variation with Temperature.

Typical Electrical Characteristics

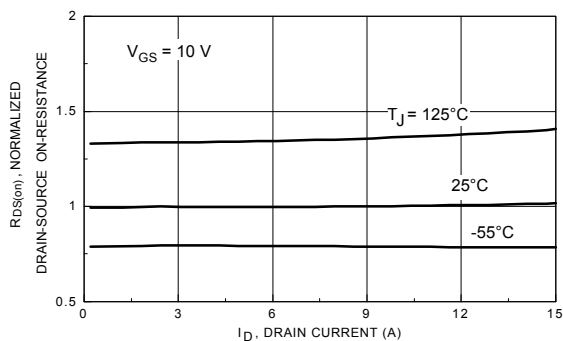


Figure 7. N-Channel On-Resistance Variation with Drain Current and Temperature.

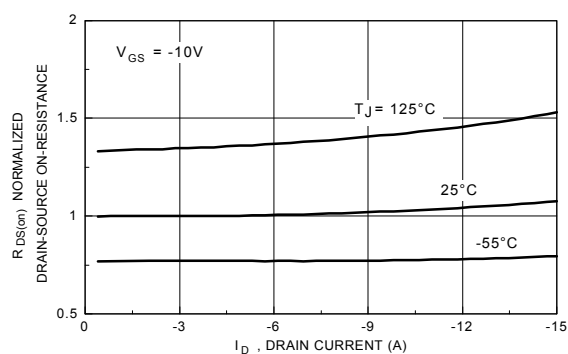


Figure 8. P-Channel On-Resistance Variation with Drain Current and Temperature.

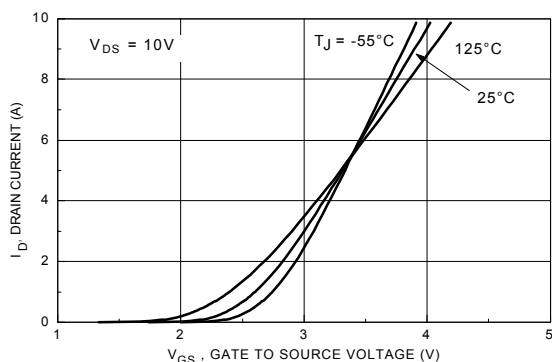


Figure 9. N-Channel Transfer Characteristics.

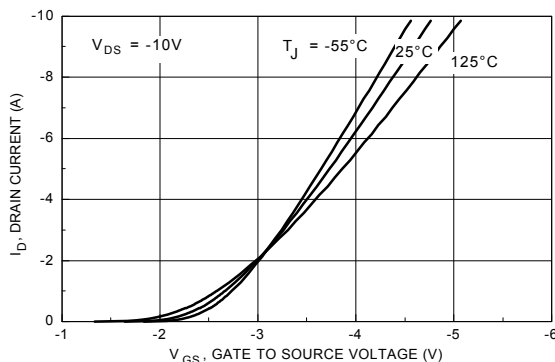


Figure 10. P-Channel Transfer Characteristics.

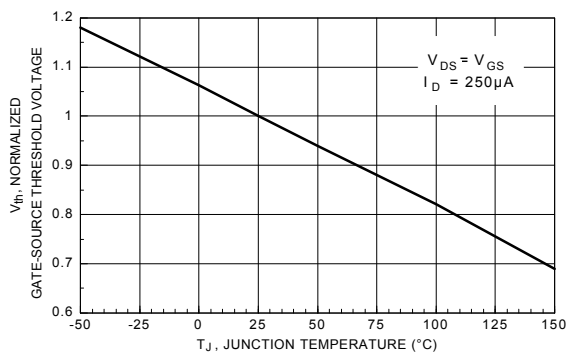


Figure 11. N-Channel Gate Threshold Variation with Temperature.

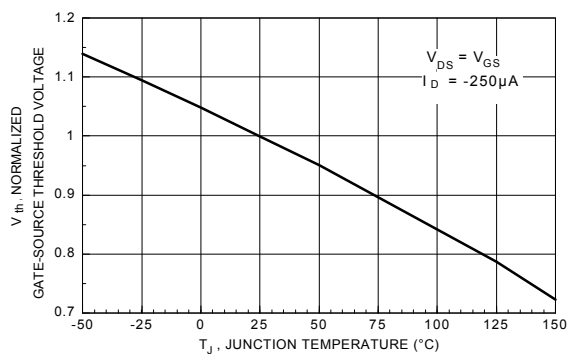


Figure 12. P-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics

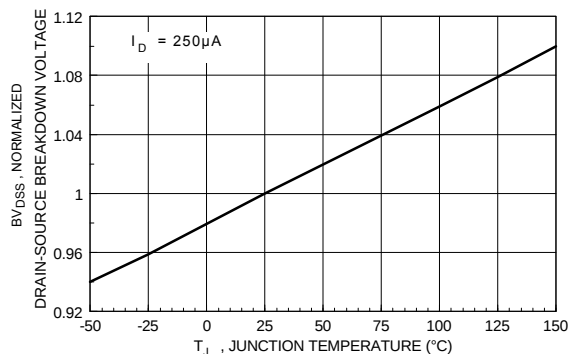


Figure 13. N-Channel Breakdown Voltage Variation with Temperature.

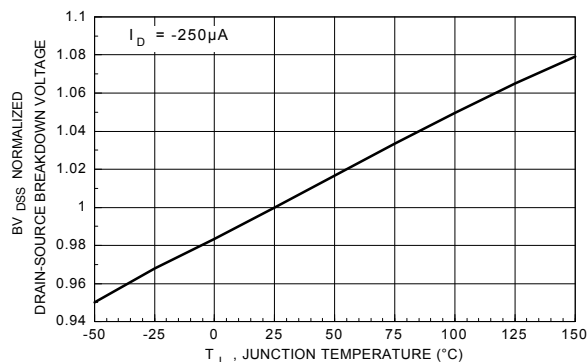


Figure 14. P-Channel Breakdown Voltage Variation with Temperature.

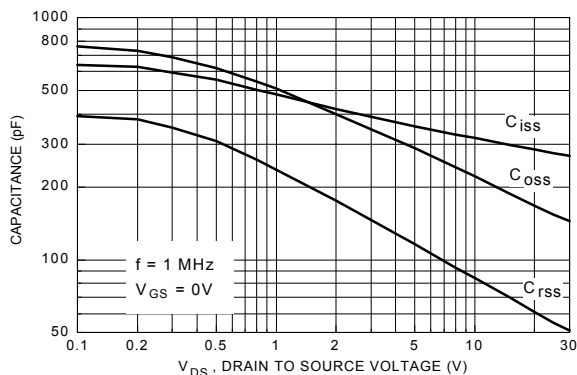


Figure 15. N-Channel Capacitance Characteristics.

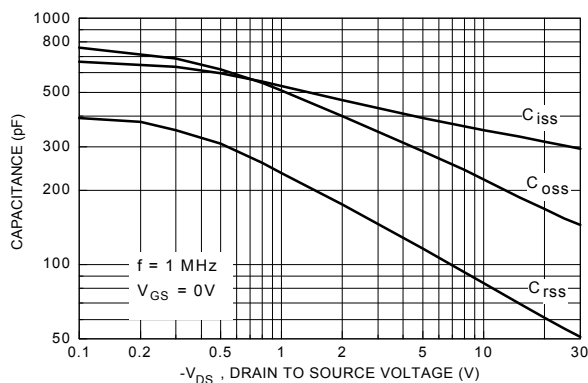


Figure 16. P-Channel Capacitance Characteristics.

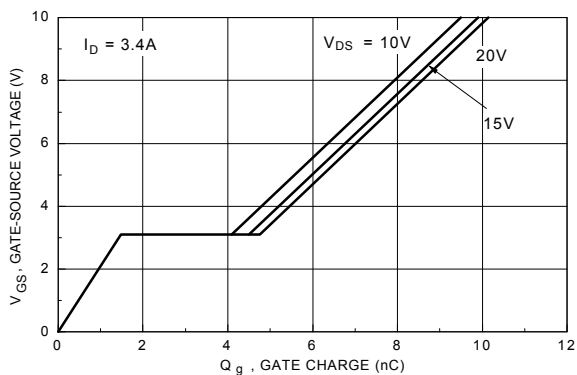


Figure 17. N-Channel Gate Charge Characteristics.

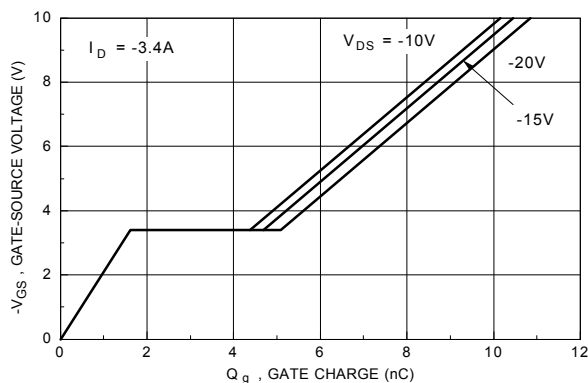


Figure 18. P-Channel Gate Charge Characteristics.

Typical Electrical and Thermal Characteristics

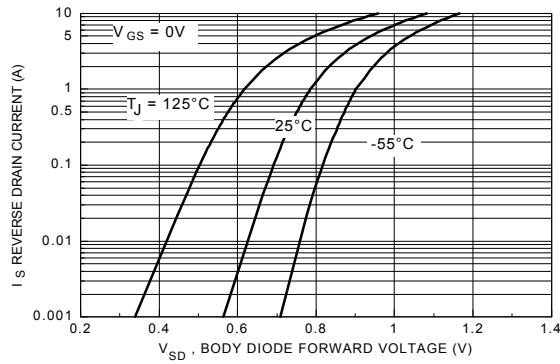


Figure 19. N-Channel Body Diode Forward Voltage Variation with Current and Temperature.

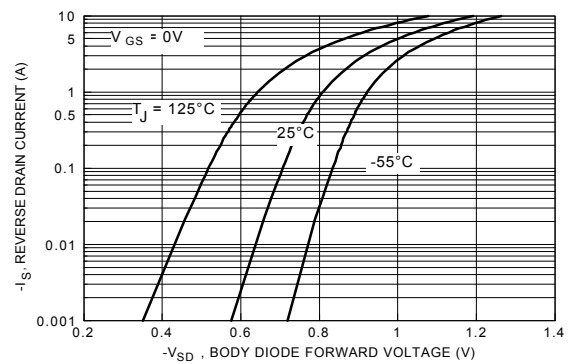


Figure 20. P-Channel Body Diode Forward Voltage Variation with Current and Temperature.

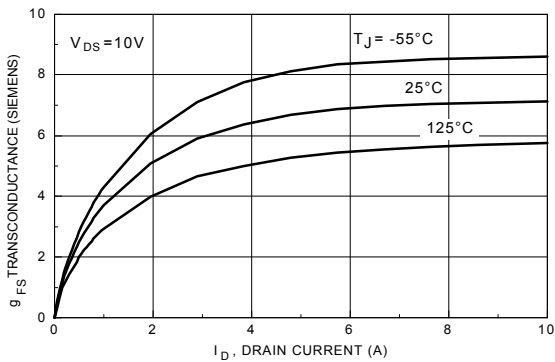


Figure 21. N-Channel Transconductance Variation with Drain Current and Temperature.

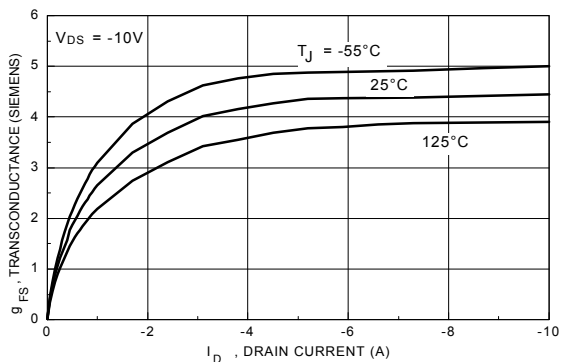


Figure 22. P-Channel Transconductance Variation with Drain Current and Temperature.

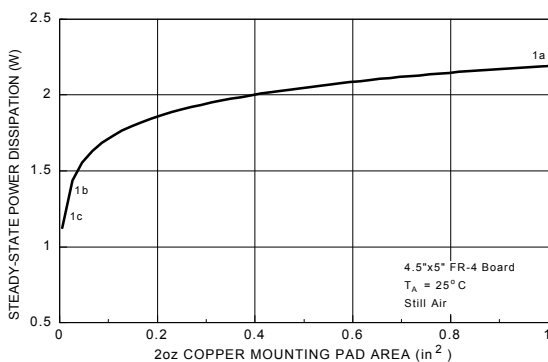


Figure 23. SO-8 Single Device DC Power Dissipation versus Copper Mounting Pad Area.

Typical Thermal Characteristics

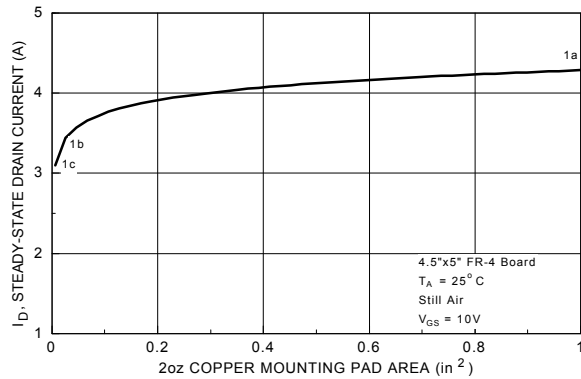


Figure 24. N-Ch Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

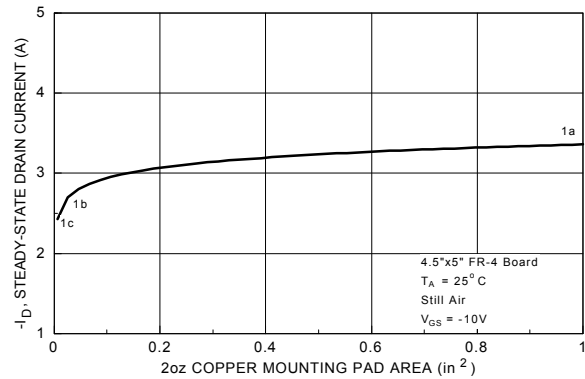


Figure 25. P-Ch Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

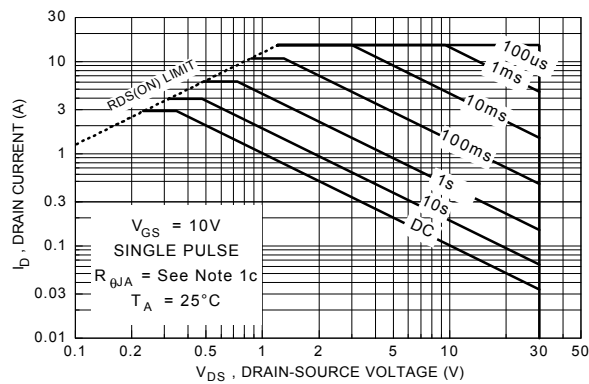


Figure 26. N-Ch Maximum Safe Operating Area.

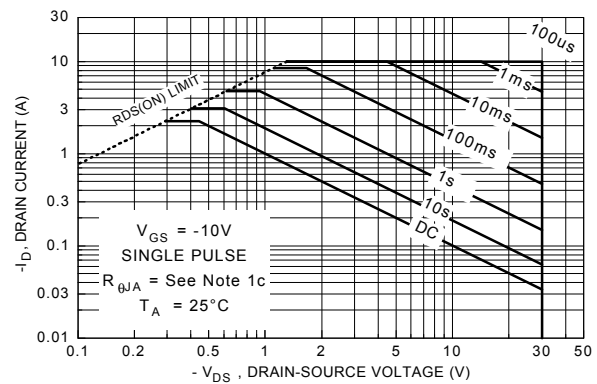


Figure 27. P-Ch Maximum Safe Operating Area.

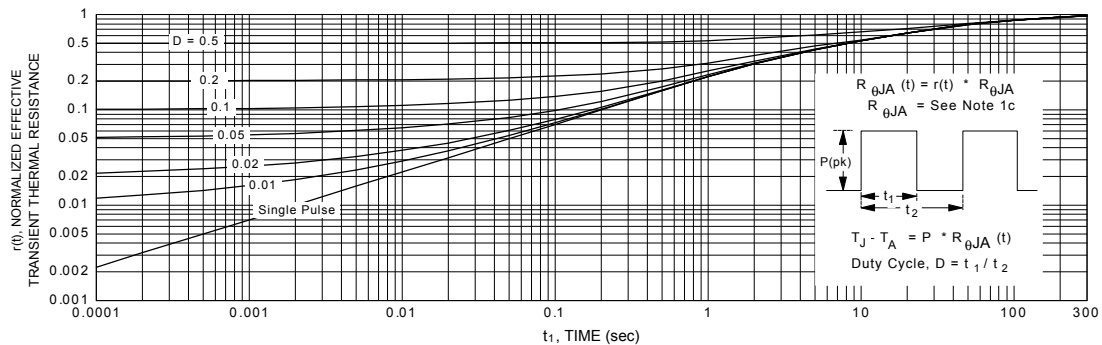


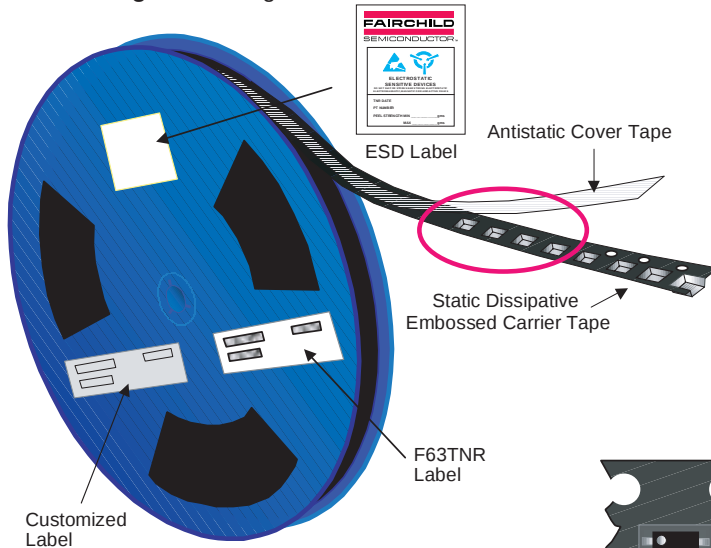
Figure 28. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

SO-8 Tape and Reel Data and Package Dimensions



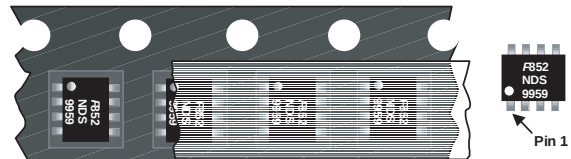
SOIC(8lds) Packaging Configuration: Figure 1.0



Packaging Description:

SOIC-8 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13" or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 500 units per 7" or 177cm diameter reel. This and some other options are further described in the Packaging Information table.

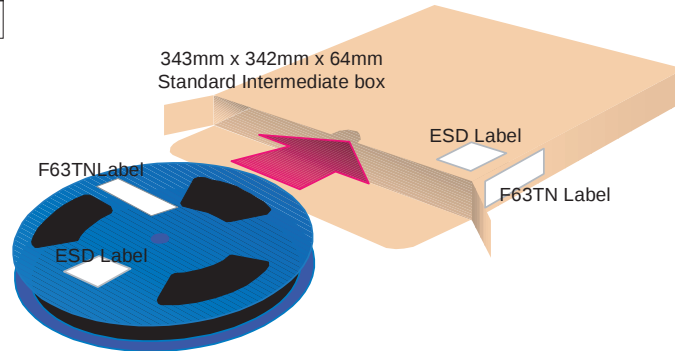
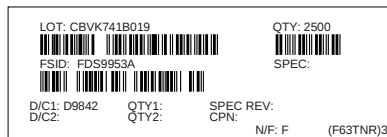
These full reels are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.



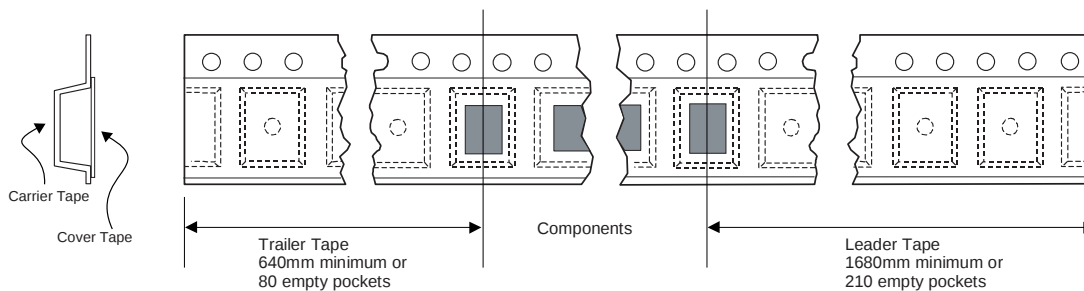
SOIC-8 Unit Orientation

SOIC (8lds) Packaging Information				
Packaging Option	Standard (no flow code)	L86Z	F011	D84Z
Packaging type	TNR	Rail/Tube	TNR	TNR
Qty per Reel/Tube/Bag	2,500	95	4,000	500
Reel Size	13" Dia	-	13" Dia	7" Dia
Box Dimension (mm)	343x64x343	530x130x83	343x64x343	184x187x47
Max qty per Box	5,000	30,000	8,000	1,000
Weight per unit (gm)	0.0774	0.0774	0.0774	0.0774
Weight per Reel (kg)	0.6060	-	0.9696	0.1182
Note/Comments				

F63TNR Label sample

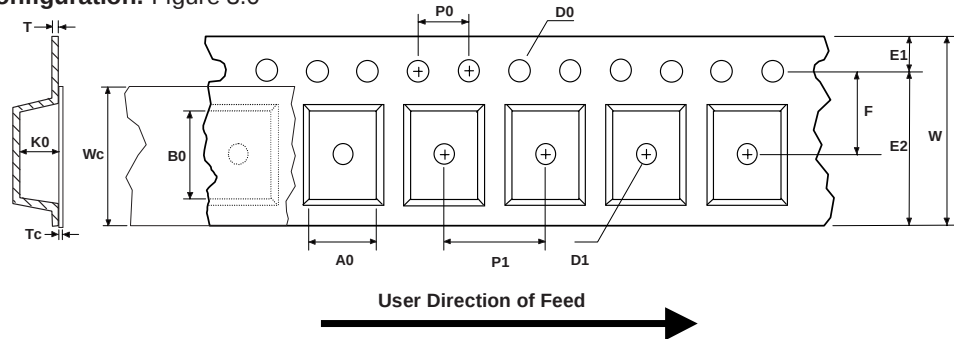


SOIC(8lds) Tape Leader and Trailer Configuration: Figure 2.0



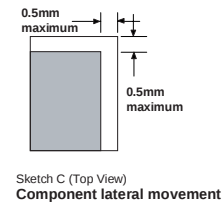
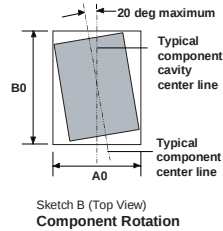
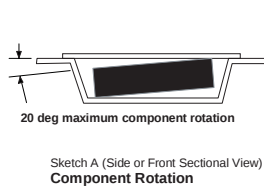
SO-8 Tape and Reel Data and Package Dimensions, continued

SOIC(8lds) Embossed Carrier Tape Configuration: Figure 3.0

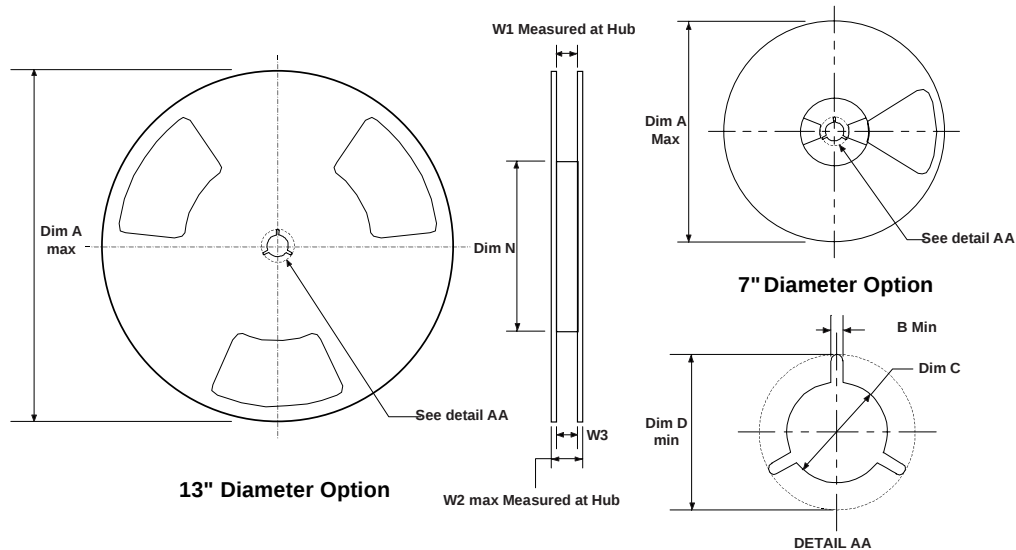


Dimensions are in millimeter														
Pkg type	A0	B0	W	D0	D1	E1	E2	F	P1	P0	K0	T	Wc	Tc
SOIC(8lds) (12mm)	6.50 +/-0.10	5.30 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	2.1 +/-0.10	0.450 +/-0.150	9.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



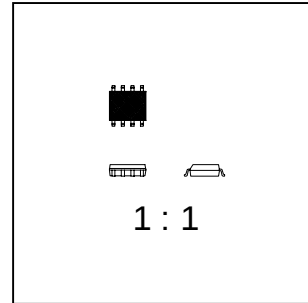
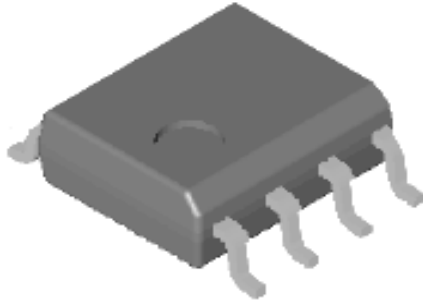
SOIC(8lds) Reel Configuration: Figure 4.0



Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4

SO-8 Tape and Reel Data and Package Dimensions, continued

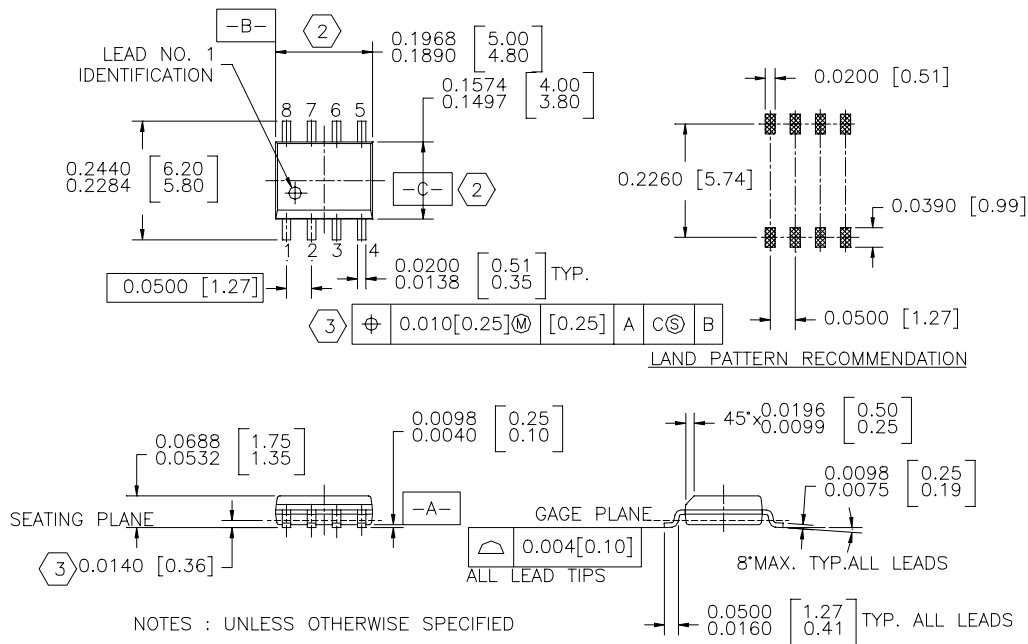
SOIC-8 (FS PKG Code S1)



Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0774



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MICROWIRE™
POP™
PowerTrench™
QFET™
QS™
Quiet Series™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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