

NDP7050L / NDB7050L

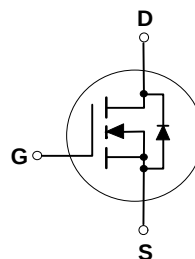
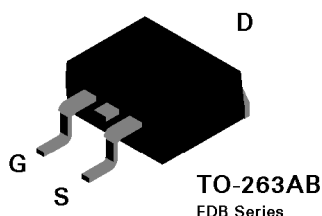
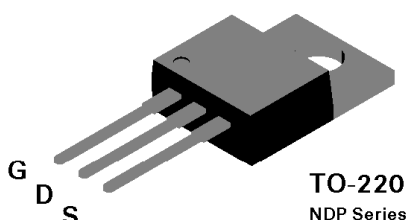
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

These logic level N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 75A, 50V, $R_{DS(ON)} = 0.015\Omega$ @ $V_{GS} = 5V$
- Low drive requirements allowing operation directly from logic drivers. $V_{GS(TH)} < 2.0V$.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D²PAK) package for both through hole and surface mount applications.



Absolute Maximum Ratings $T_c = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	NDP7050L	NDB7050L	Units
V_{DS}	Drain-Source Voltage	50		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1\text{ M}\Omega$)	50		V
V_{GSS}	Gate-Source Voltage - Continuous	± 20		V
	- Nonrepetitive ($t_p < 50\text{ }\mu\text{s}$)	± 40		
I_D	Drain Current - Continuous	75		A
	- Pulsed	225		
P_D	Total Power Dissipation @ $T_c = 25^\circ\text{C}$	150		W
	Derate above 25°C	1		W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-65 to 175		$^\circ\text{C}$

Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)						
W _{DSS}	Single Pulse Drain-Source Avalanche Energy	V _{DD} = 25 V, I _D = 75 A			550	mJ
I _{AR}	Maximum Drain-Source Avalanche Current				75	A
OFF CHARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	50			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 50 V, V _{GS} = 0 V			250	μA
		T _J = 125°C			1	mA
I _{GSSF}	Gate - Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	V _{GS} = -20 V, V _{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	1	1.3	2	V
		T _J = 125°C	0.65	0.8	1.5	
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} = 5 V, I _D = 37.5 A		0.01	0.015	Ω
		T _J = 125°C		0.016	0.024	
I _{D(on)}	On-State Drain Current	V _{GS} = 5 V, V _{DS} = 10 V	75			A
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 37.5 A	15	67		S
DYNAMIC CHARACTERISTICS						
C _{ISS}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz		4200	4000	pF
C _{OSS}	Output Capacitance			1100	1600	pF
C _{RSS}	Reverse Transfer Capacitance			310	800	pF
SWITCHING CHARACTERISTICS (Note 1)						
t _{D(on)}	Turn - On Delay Time	V _{DD} = 30 V, I _D = 75 A, V _{GS} = 5 V, R _{GEN} = 10Ω R _{GS} = 10 Ω		23	40	nS
t _r	Turn - On Rise Time			460	600	nS
t _{D(off)}	Turn - Off Delay Time			100	150	nS
t _f	Turn - Off Fall Time			270	400	nS
Q _g	Total Gate Charge	V _{DS} = 48 V, I _b = 75 A, V _{GS} = 5 V		86	115	nC
Q _{gs}	Gate-Source Charge			13		nC
Q _{gd}	Gate-Drain Charge			62		nC

Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I _S	Maximum Continuos Drain-Source Diode Forward Current				75	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current				225	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 37.5 A (Note 1) T_J = 125°C		0.92	1.3	V
				0.85	1.2	
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _F = 60A, dI _F /dt = 100 A/μs		108	150	ns
I _{rr}	Reverse Recovery Current			4.6	10	A
THERMAL CHARACTERISTICS						
R _{θJC}	Thermal Resistance, Junction-to-Case				1	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient				62.5	°C/W

Note:

1. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

Typical Electrical Characteristics

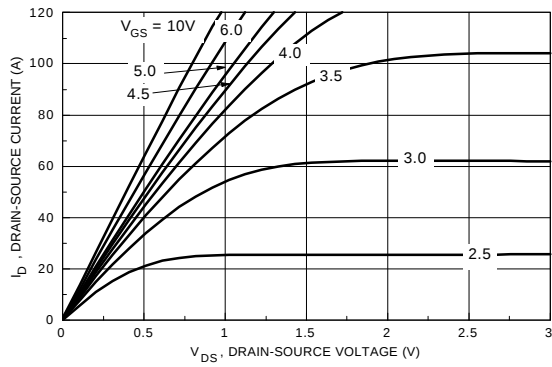


Figure 1. On-Region Characteristics

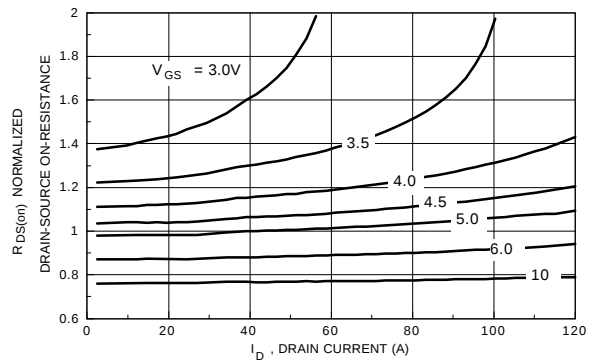


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

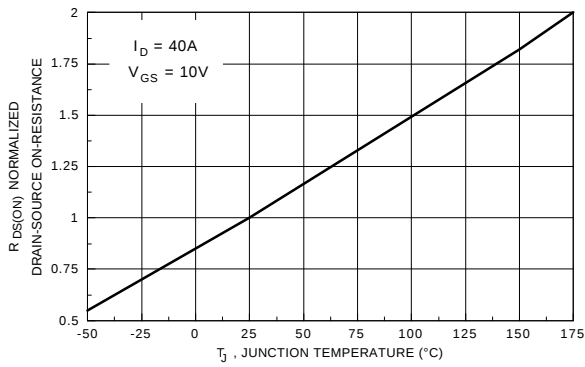


Figure 3. On-Resistance Variation with Temperature

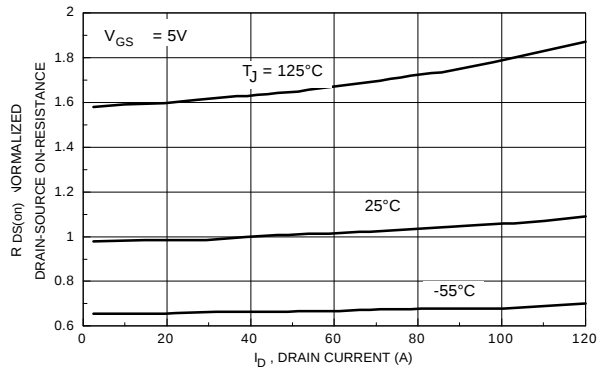


Figure 4. On-Resistance Variation with Drain Current and Temperature

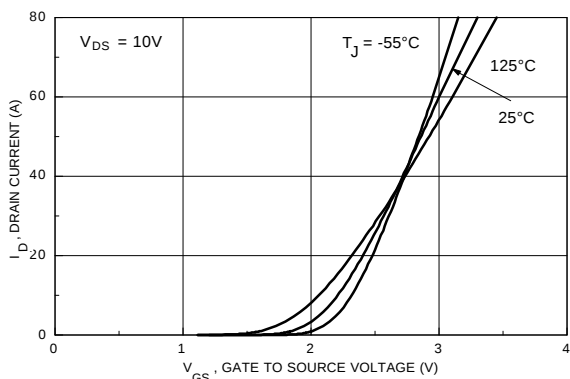


Figure 5. Transfer Characteristics

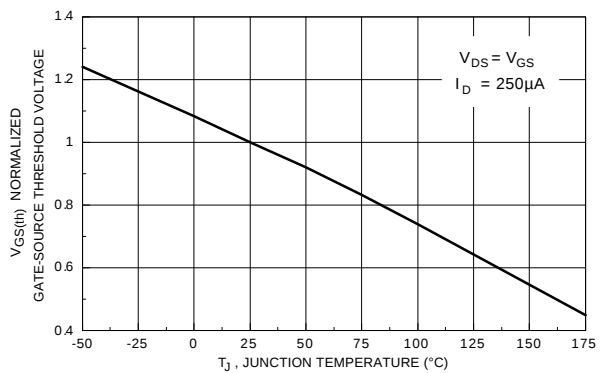


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

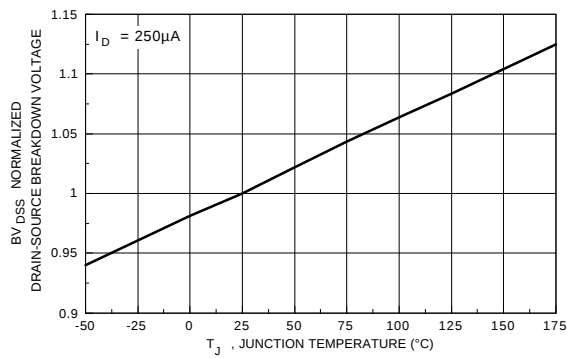


Figure 7. Breakdown Voltage Variation with Temperature

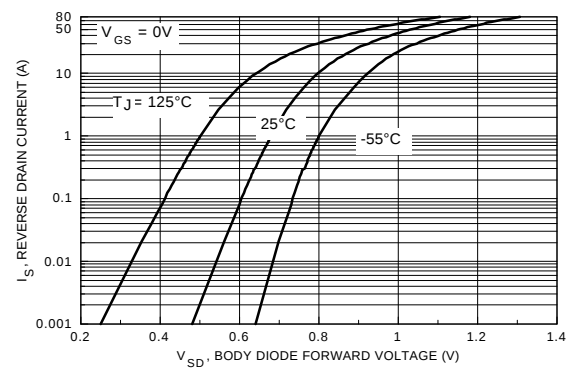


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

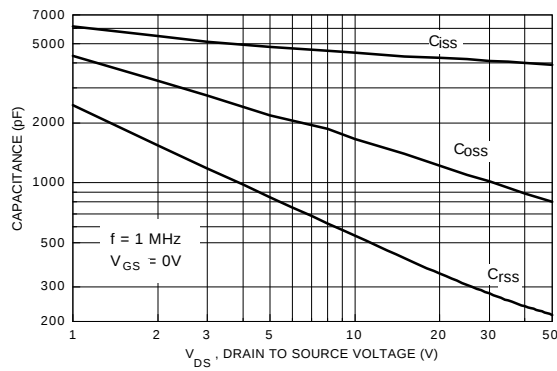


Figure 9. Capacitance Characteristics

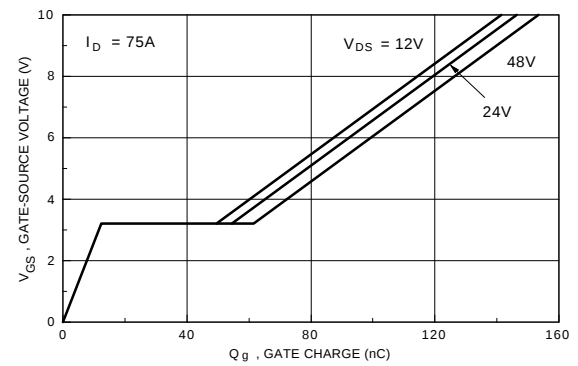


Figure 10. Gate Charge Characteristics

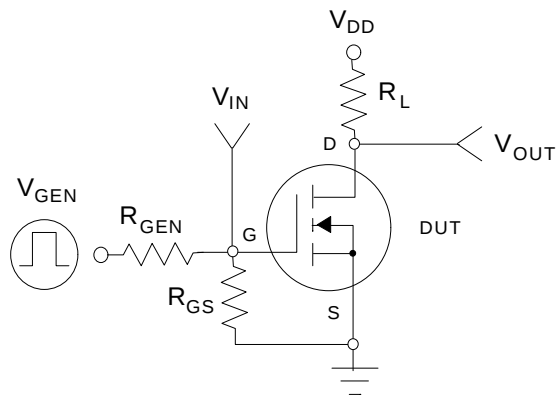


Figure 11. Switching Test Circuit

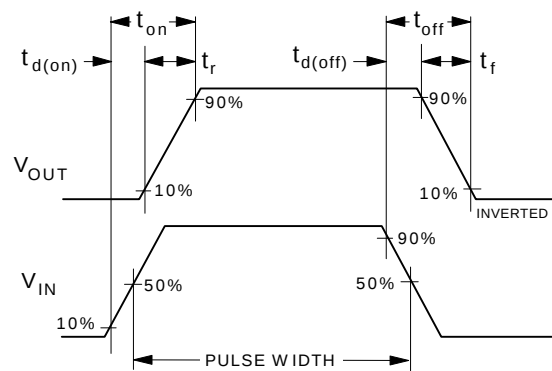


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

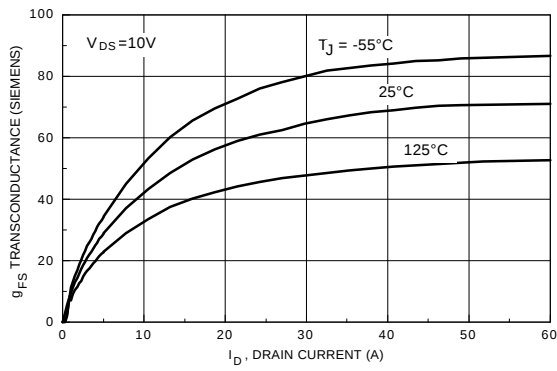


Figure 13. Transconductance Variation with Drain Current and Temperature

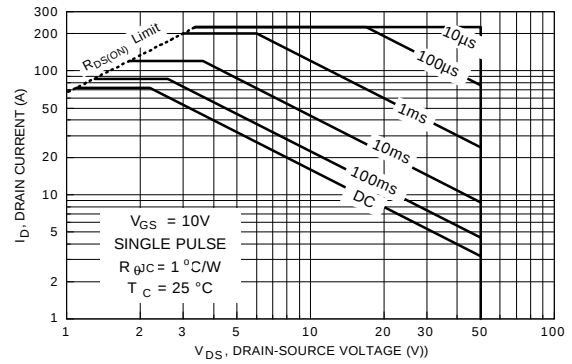


Figure 14. Maximum Safe Operating Area

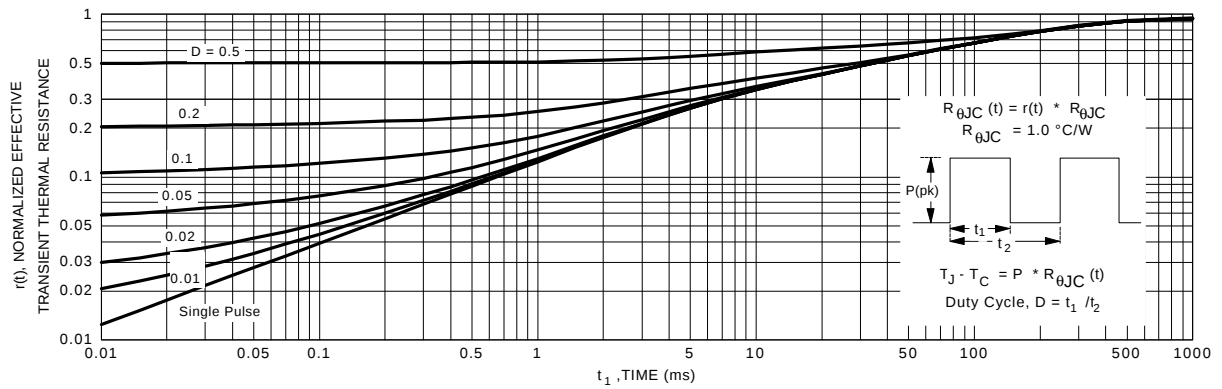


Figure 15. Transient Thermal Response Curve