

## NDC632P

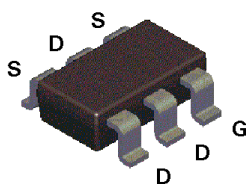
### P-Channel Logic Level Enhancement Mode Field Effect Transistor

#### General Description

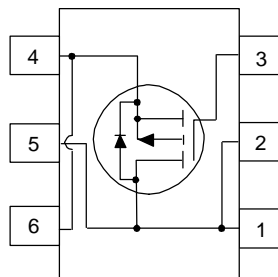
These P-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

#### Features

- -2.7A, -20V.  $R_{DS(ON)} = 0.14\Omega$  @  $V_{GS} = -4.5V$   
 $R_{DS(ON)} = 0.2\Omega$  @  $V_{GS} = -2.7V$ .
- Proprietary SuperSOT™-6 package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low  $R_{DS(ON)}$ .
- Exceptional on-resistance and maximum DC current capability.



SuperSOT™-6



#### Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	NDC632P	Units
$V_{DS}$	Drain-Source Voltage	-20	V
$V_{GSS}$	Gate-Source Voltage - Continuous	-8	V
$I_D$	Drain Current - Continuous	-2.7	A
	- Pulsed	-10	
$P_D$	Maximum Power Dissipation (Note 1a)	1.6	W
	(Note 1b)	1	
	(Note 1c)	0.8	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

#### THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	30	$^\circ\text{C/W}$

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	-20			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -16 V, V <sub>GS</sub> = 0 V			-1	μA
		T <sub>J</sub> = 55°C			-10	μA
I <sub>GSSF</sub>	Gate - Body Leakage, Forward	V <sub>GS</sub> = 8 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate - Body Leakage, Reverse	V <sub>GS</sub> = -8 V, V <sub>DS</sub> = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-0.4	-0.7	-1	V
		T <sub>J</sub> = 125°C	-0.3	-0.5	-0.8	
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = - 2.7 A		0.1	0.14	Ω
		T <sub>J</sub> = 125°C		0.145	0.28	
		V <sub>GS</sub> = -2.7 V, I <sub>D</sub> = - 2.2 A		0.152	0.2	
I <sub>D(on)</sub>	On-State Drain Current	V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> = -5 V	-10			A
		V <sub>GS</sub> = -2.7 V, V <sub>DS</sub> = -5 V	-4			
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = -10 V, I <sub>D</sub> = - 2.7 A		6		S
DYNAMIC CHARACTERISTICS						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		550		pF
C <sub>oss</sub>	Output Capacitance			260		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			75		pF
SWITCHING CHARACTERISTICS (Note 2)						
t <sub>D(on)</sub>	Turn - On Delay Time	V <sub>DD</sub> = -5 V, I <sub>D</sub> = -1 A,		10	20	ns
t <sub>r</sub>	Turn - On Rise Time	V <sub>GEN</sub> = -4.5 V, R <sub>GEN</sub> = 6 Ω		40	60	ns
t <sub>D(off)</sub>	Turn - Off Delay Time			25	40	ns
t <sub>f</sub>	Turn - Off Fall Time			17	30	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = -5 V,		8.7	15	nC
Q <sub>gs</sub>	Gate-Source Charge	I <sub>D</sub> = -2.7 A, V <sub>GS</sub> = -4.5 V		1.7		nC
Q <sub>gd</sub>	Gate-Drain Charge			1.8		nC

ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I <sub>S</sub>	Continuous Source Diode Current				-1.3	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -1.3 A (Note 2)		-0.77	-1.2	V

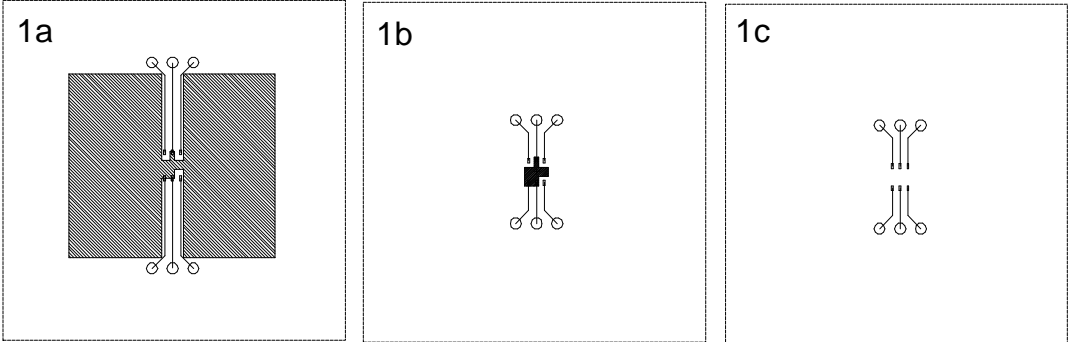
Notes:

1. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(on)} @ T_J$$

Typical R<sub>θJA</sub> using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- a. 78°C/W when mounted on a 1 in<sup>2</sup> pad of 2oz copper.
- b. 125°C/W when mounted on a 0.01 in<sup>2</sup> pad of 2oz copper.
- c. 156°C/W when mounted on a 0.003 in<sup>2</sup> pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

## Typical Electrical Characteristics

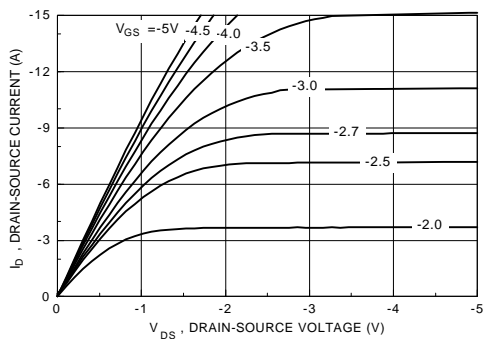


Figure 1. On-Region Characteristics.

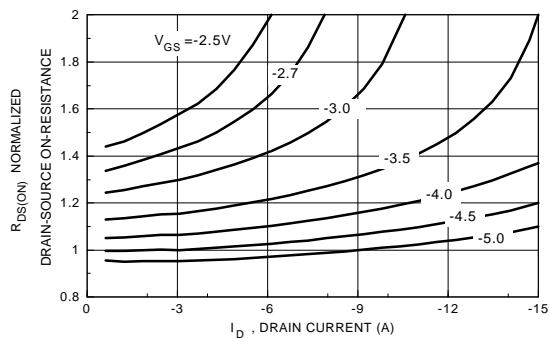


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

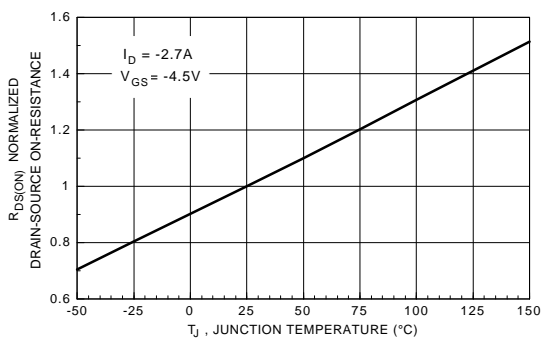


Figure 3. On-Resistance Variation with Temperature.

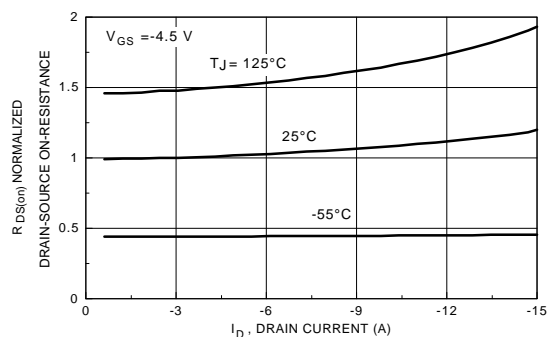


Figure 4. On-Resistance Variation with Drain Current and Temperature.

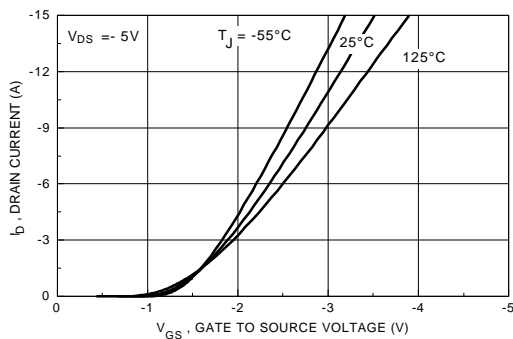


Figure 5. Transfer Characteristics.

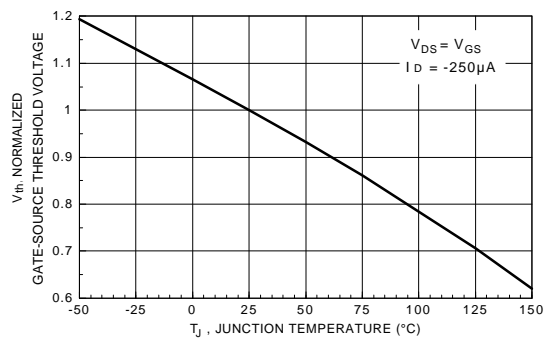
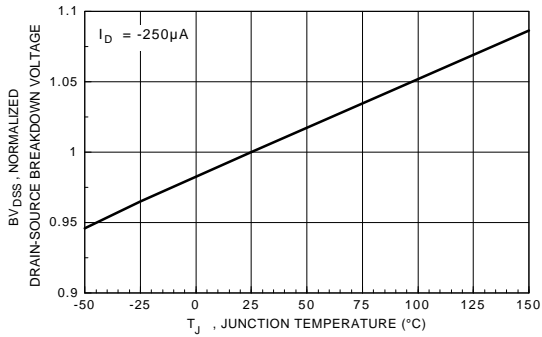
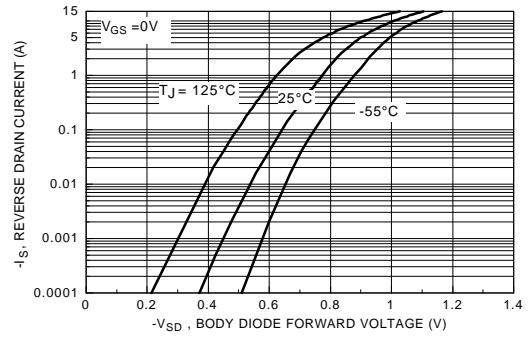


Figure 6. Gate Threshold Variation with Temperature.

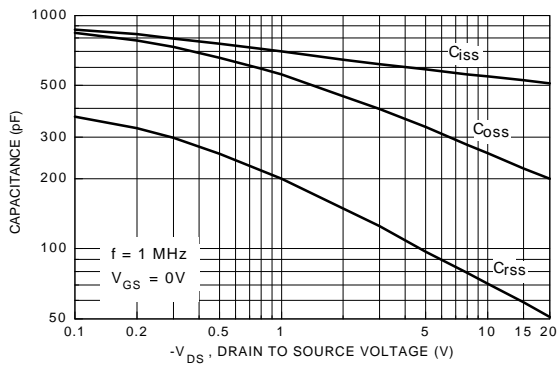
## Typical Electrical Characteristics (continued)



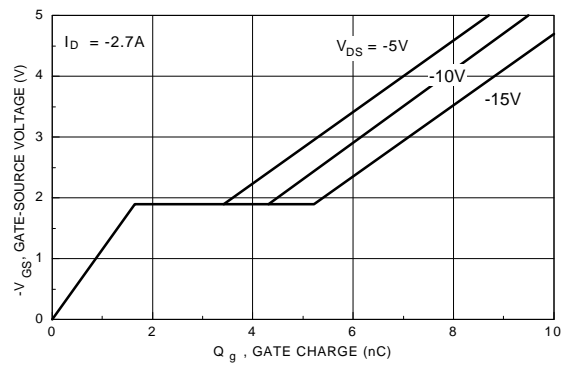
**Figure 7. Breakdown Voltage Variation with Temperature.**



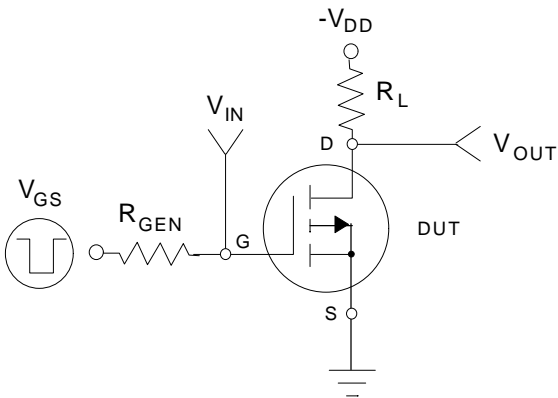
**Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature.**



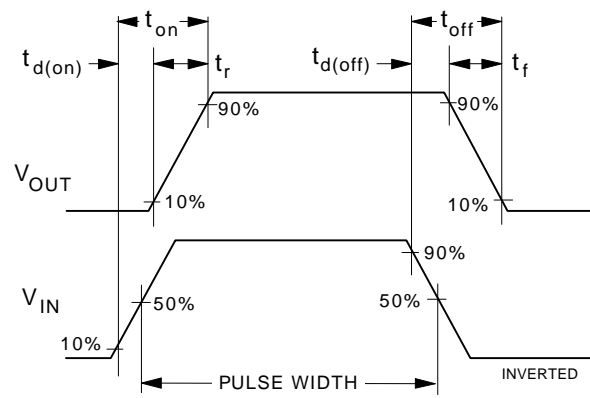
**Figure 9. Capacitance Characteristics.**



**Figure 10. Gate Charge Characteristics.**

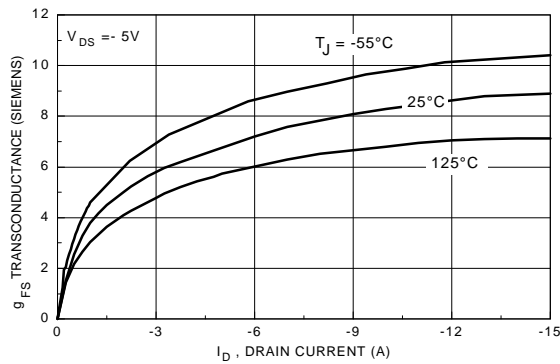


**Figure 11. Switching Test Circuit.**

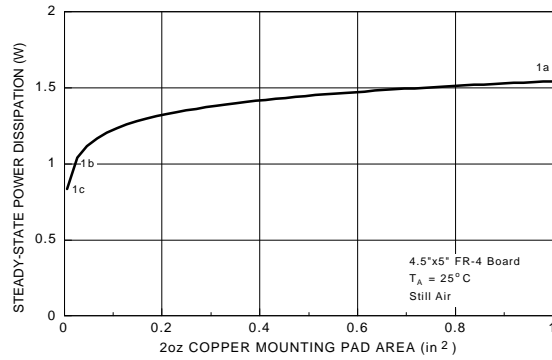


**Figure 12. Switching Waveforms.**

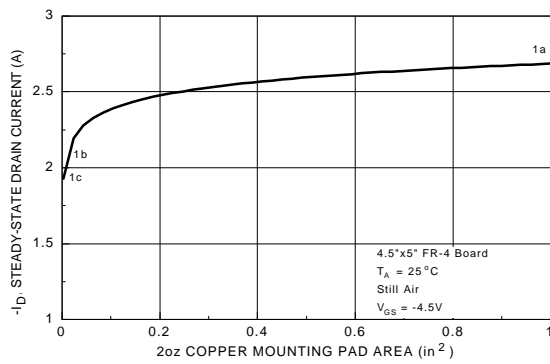
## Typical Electrical and Thermal Characteristics (continued)



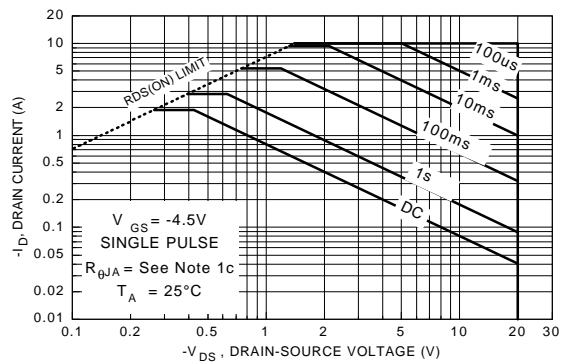
**Figure 13. Transconductance Variation with Drain Current and Temperature.**



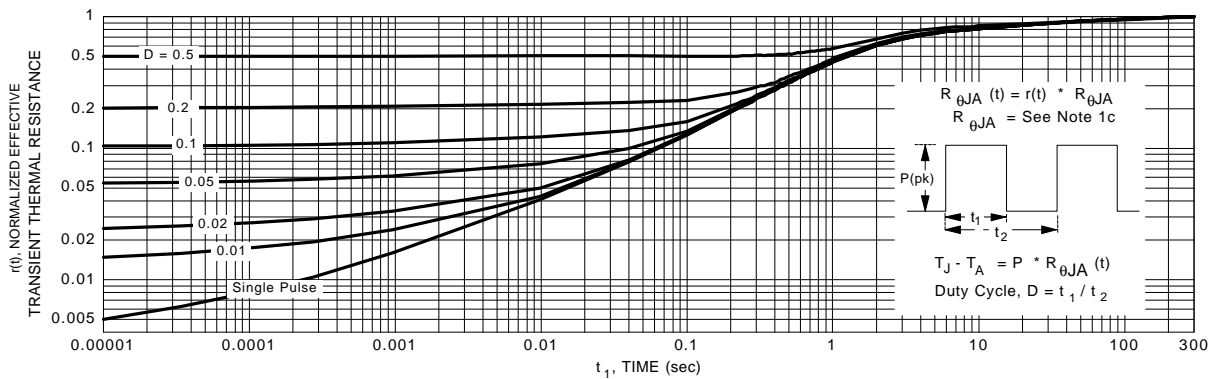
**Figure 14. SuperSOT™-6 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.**



**Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.**



**Figure 16. Maximum Safe Operating Area**



**Figure 17. Transient Thermal Response Curve.**

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

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