

MM82C19 16-Line to 1-Line Multiplexer

General Description

The MM82C19 multiplex 16 digital lines to 1 output. A 4-bit address code determines the particular 1-of-16 inputs which is routed to the output. The data is inverted from input to output.

A strobe override places the output of MM82C19 in the high-impedance state.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

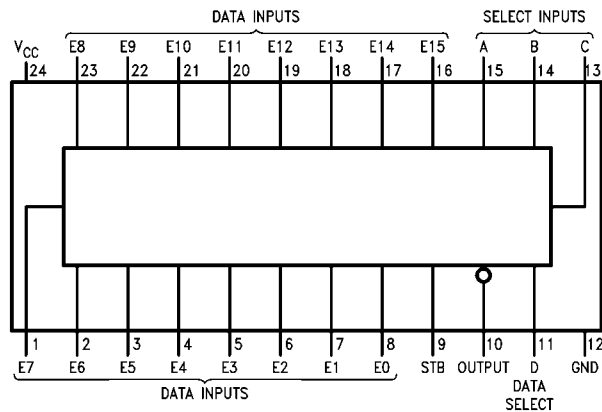
Features

- Wide supply voltage range: 3.0V to 15V
- Guaranteed noise margin: 1.0V
- High noise immunity: 0.45 V_{CC} (typ.)
- TTL compatibility: Drive 1 TTL Load

Ordering Code:

Order Number	Package Number	Package Description
MM82C19N	N24A	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-011, 0.600" Wide

Connection Diagram



Truth Table

MM82C19

				Inputs																Output	
D	C	B	A	STROBE	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14	E15	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	High-Z
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	0
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	1
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	0
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	1
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0
0	1	1	1	1	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0
1	0	0	1	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1
1	0	0	1	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0
1	0	1	0	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
1	0	1	0	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	0
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	1
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	0
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	1
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	0
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	1
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	0
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	0
1	1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1
1	1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0

Logic Diagram

The logic diagram illustrates a 16-to-1 multiplexer circuit. It features 16 data inputs labeled E0 through E15, each preceded by an inverter. A strobe input, labeled STROBE, is also inverted. The circuit is composed of four stages of 4-to-1 multiplexers, each implemented with four 2-input AND gates and one 4-input OR gate. The first stage selects between inputs E0-E3 based on strobe and address bit A. The second stage selects between inputs E4-E7 based on address bit B. The third stage selects between inputs E8-E11 based on address bit C. The fourth stage selects between inputs E12-E15 based on address bit D. The outputs of these four stages are combined in a final 4-to-1 multiplexer to produce the OUTPUT. The output is a push-pull stage consisting of a PMOS transistor connected to VCC and an NMOS transistor connected to ground, with a buffer inverter preceding the NMOS transistor. Address bits A, B, C, and D are shown with both true and complemented signals.

Logic Diagram

The diagram illustrates a 16-to-1 multiplexer circuit. It features 16 data inputs labeled E0 through E15, each followed by an inverter. There are four select inputs labeled A, B, C, and D, each followed by an inverter to provide both the input and its complement. A strobe input is also present, followed by an inverter. The circuit is composed of 16 2-input AND gates in the first stage, which combine the data inputs with the select inputs. These are followed by four 3-input AND gates that incorporate the strobe signal. The outputs of these four gates are then combined by a single 4-input OR gate. The output of the OR gate is connected to a CMOS output stage, consisting of a PMOS transistor connected to VCC and an NMOS transistor connected to ground, with the output node labeled 'OUTPUT'.

Absolute Maximum Ratings(Note 1)

Voltage at Any Pin	-0.3V to $V_{CC} + 0.3V$
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3.0V to 15V
V_{CC}	18V
Lead Temperature (soldering, 10 seconds)	260°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristic table provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted.

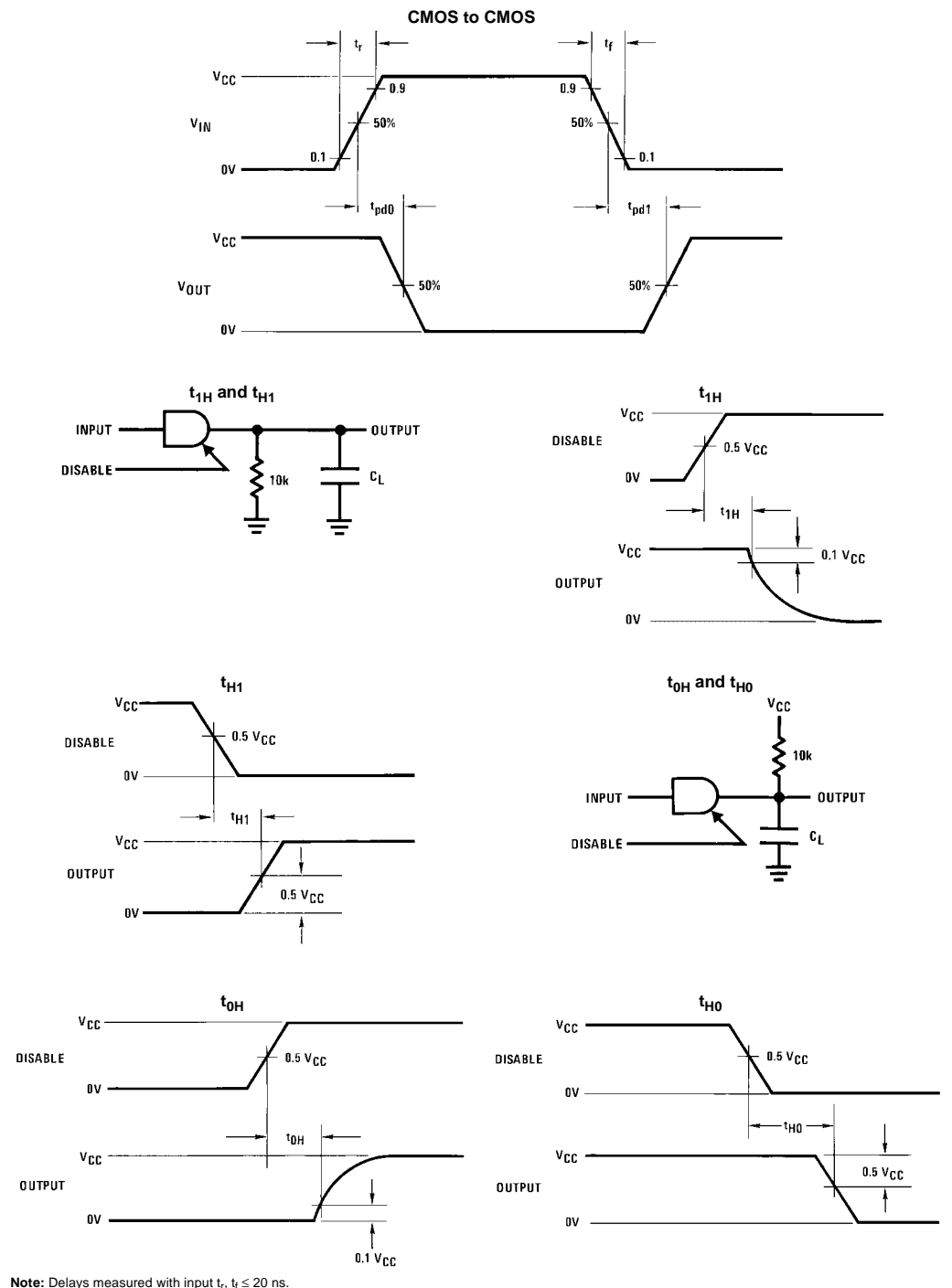
Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$	3.5 8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$			1.5 2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0V, I_O = -10 \mu A$ $V_{CC} = 10V, I_O = -10 \mu A$	4.5 9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0V, I_O = +10 \mu A$ $V_{CC} = 10V, I_O = +10 \mu A$			0.5 1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	V
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		μA
I_{OZ}	Output Current in High Impedance State MM82C19	$V_{CC} = 15V, V_O = 15V$ $V_{CC} = 15V, V_O = 0V$	-1.0	0.005 -0.005	1.0	μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	300	μA
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	74C, 82C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	74C, 82C, $V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	74C, 82C, $V_{CC} = 4.75V, I_O = -1.6 mA$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	74C, 82C, $V_{CC} = 4.75V, I_O = 1.6 mA$			0.4	V
Output Drive (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25^\circ C$	-4.35	-8		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V, V_{OUT} = 0V, T_A = 25^\circ C$	-20	-40		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25^\circ C$	4.35	8		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25^\circ C$	20	40		mA

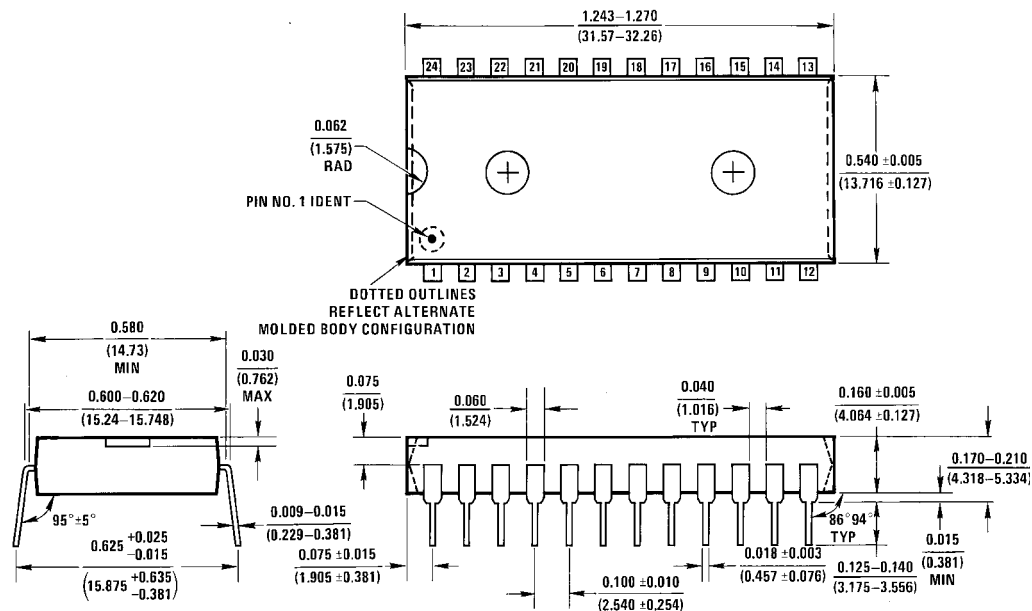
AC Electrical Characteristics (Note 2) $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0} , t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Inputs to Output	$V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 5.0\text{V}$, $C_L = 150\text{ pF}$ $V_{CC} = 10\text{V}$, $C_L = 150\text{ pF}$		250 110 290 120	600 300 650 330	ns
t_{pd0} , t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Select Inputs to Output	$V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$		290 120	650 330	ns
t_{pd0} , t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Strobe to Output MM74C150	$V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$		120 55	300 150	ns
t_{1H} , t_{0H}	Delay from Strobe to High Impedance State MM82C19	$V_{CC} = 5.0\text{V}$, $R_L = 10\text{k}$, $C_L = 5\text{ pF}$ $V_{CC} = 10\text{V}$, $R_L = 10\text{k}$, $C_L = 5\text{ pF}$		80 60	200 150	ns
t_{H1} , t_{H0}	Delay from Strobe to Logical "1" Level or to Logical "0" Level (from High Impedance State) MM82C19	$V_{CC} = 5.0\text{V}$, $R_L = 10\text{k}$, $C_L = 5\text{ pF}$ $V_{CC} = 10\text{V}$, $R_L = 10\text{k}$, $C_L = 5\text{ pF}$		80 30	250 120	ns
C_{IN}	Input Capacitance	Any Input (Note 3)		5.0		pF
C_{OUT}	Output Capacitance MM82C19	(Note 3)		11.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 4)		100		pF

Note 2: AC Parameters are guaranteed by DC correlated testing.**Note 3:** Capacitance is guaranteed by periodic testing.**Note 4:** C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see Family Characteristics, application note AN-90.

Switching Time Waveforms





**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-011, 0.600" Wide
Package Number N24A**

LIFE SUPPORT POLICY

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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