

October 1987 Revised May 2002

# MM74C157 Quad 2-Input Multiplexers

## **General Description**

The MM74C157 multiplexers are monolithic complementary MOS (CMOS) integrated circuits constructed with N-and P-channel enhancement transistors. They consist of four 2-input multiplexers with common select and enable inputs. When the enable input is at logical "0" the four outputs assume the values as selected from the inputs. When the enable input is at logical "1", the outputs assume logical "0". Select decoding is done internally resulting in a single select input only.

#### **Features**

■ Supply voltage range: 3V to 15V■ High noise immunity: 0.45 V<sub>CC</sub> (typ.)

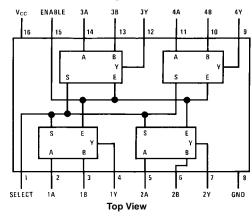
■ Low power: 50 nW (typ.)

■ Tenth power TTL compatible: Drive 2 LPTTL loads

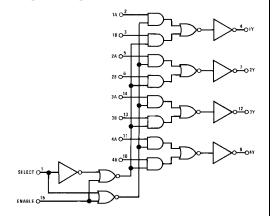
# **Ordering Code:**

Order Number	Package Number	Package Description			
MM74C157N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide			

## **Connection Diagram**



## **Logic Diagram**



## **Truth Table**

Enable	Select	Α	В	Output Y
1	Х	Х	Х	0
0	0	0	Х	0
0	0	1	Х	1
0	1	X	0	0
0	1	X	1	1

## Absolute Maximum Ratings(Note 1)

 $\begin{tabular}{llll} Voltage at Any Pin & -0.3V to $V_{CC}$ + 0.3V \\ Operating Temperature Range & -55^{\circ}C to +125^{\circ}C \\ Storage Temperature Range & -65^{\circ}C to +150^{\circ}C \\ Maximum $V_{CC}$ Voltage & 18V \\ \end{tabular}$ 

Power Dissipation (P<sub>D</sub>)

Dual-In-Line 700 mW Small Outline 500 mW

Operating V<sub>CC</sub> Range 3V to 15V

Lead Temperature

(Soldering, 10 seconds) 260°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

## **DC Electrical Characteristics**

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Тур	Max	Units	
CMOS TO	смоѕ	•			•	•	
V <sub>IN(1)</sub>	Logical "1" Input Voltage	V <sub>CC</sub> = 5V	3.5			V	
		$V_{CC} = 10V$	8.0			v	
V <sub>IN(0)</sub>	Logical "0" Input Voltage	V <sub>CC</sub> = 5V			1.5	V	
		V <sub>CC</sub> = 10V			2.0	v	
V <sub>OUT(1)</sub>	Logical "1" Output Voltage	V <sub>CC</sub> = 5V	4.5			V	
		$V_{CC} = 10V$	9.0			v	
V <sub>OUT(0)</sub>	Logical "0" Output Voltage	V <sub>CC</sub> = 5V			0.5	V	
		V <sub>CC</sub> = 10V			1.0	v	
I <sub>IN(1)</sub>	Logical "1" Input Current	V <sub>CC</sub> = 15V		0.005	1.0	μΑ	
I <sub>IN(0)</sub>	Logical "0" Input Current	V <sub>CC</sub> = 15V	-1.0	-0.005		μΑ	
Icc	Supply Current	V <sub>CC</sub> = 15V		0.05	60	μΑ	
CMOS TO	TENTH POWER INTERFACE	<u> </u>			•		
V <sub>IN(1)</sub>	Logical "1" Input Voltage	V <sub>CC</sub> = 4.75V	V <sub>CC</sub> - 1.5			V	
V <sub>IN(0)</sub>	Logical "0" Input Voltage	V <sub>CC</sub> = 4.75V			0.8	V	
V <sub>OUT(1)</sub>	Logical "1" Output Voltage	$V_{CC} = 4.75V$ , $I_{O} = -360 \mu A$	2.4			V	
V <sub>OUT(0)</sub>	Logical "0" Output Voltage	$V_{CC} = 4.75V, I_{O} = 360 \mu A$			0.4	V	
OUTPUT D	DRIVE (See Family Characteristics	Data Sheet) (Short Circuit Current)			•		
I <sub>SOURCE</sub>	Output Source Current	$V_{CC} = 5V, V_{IN(0)} = 0V$	-1.75			mA	
		$T_A = 25^{\circ}C$ , $V_{OUT} = 0V$					
I <sub>SOURCE</sub>	Output Source Current	$V_{CC} = 10V, V_{IN(0)} = 0V$	-8.0			mA	
		$T_A = 25$ °C, $V_{OUT} = 0$ V					
I <sub>SINK</sub>	Output Sink Current	$V_{CC} = 5V, V_{IN(1)} = 5V$	1.75			mA	
		$T_A = 25^{\circ}C$ , $V_{OUT} = V_{CC}$					
I <sub>SINK</sub>	Output Sink Current	$V_{CC} = 10V, V_{IN(1)} = 10V$	8.0			mA	
		$T_A = 25$ °C, $V_{OUT} = V_{CC}$					

## AC Electrical Characteristics (Note 2)

 $T_{\Delta} = 25^{\circ}C$ ,  $C_{L} = 50$  pF, unless otherwise specified

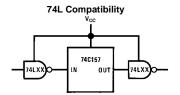
Symbol	Parameter	Conditions	Min	Тур	Max	Units
t <sub>pd0</sub> , t <sub>pd1</sub>	Propagation Delay from	V <sub>CC</sub> = 5.0V		150	250	ns
	Data to Output	$V_{CC} = 10V$		70	110	
$t_{pd0}, t_{pd1}$	Propagation Delay from	$V_{CC} = 5V$		180	300	ns
	Select to Output	$V_{CC} = 10V$		80	130	
t <sub>pd0</sub> , t <sub>pd1</sub>	Propagation Delay from	V <sub>CC</sub> = 5V		180	300	ns
	Enable to Output	$V_{CC} = 10V$		80	130	
C <sub>IN</sub>	Input Capacitance	(Note 3)		5		pF
C <sub>PD</sub>	Power Dissipation	(Note 4)		20		pF
	Capacitance					

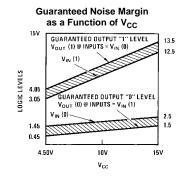
Note 2: AC Parameters are guaranteed by DC correlated testing.

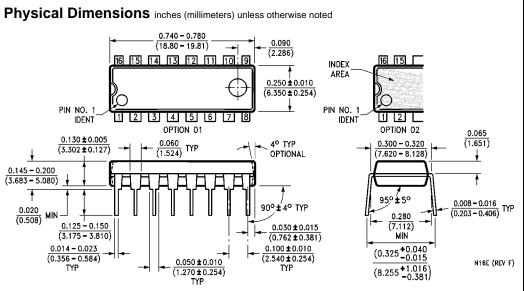
Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C<sub>PD</sub> determines the no load AC power consumption of any CMOS device. For complete explanation, see Family Characteristics, Application Note AN-90.

## **Typical Applications**







16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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