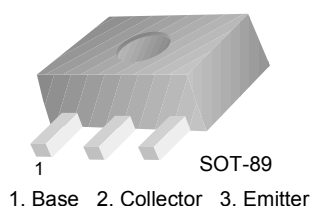


KSA1203

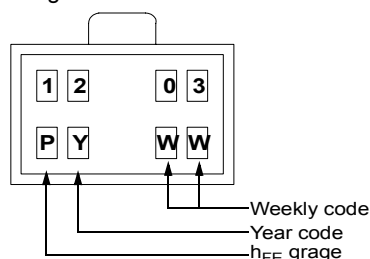
PNP Epitaxial Silicon Transistor

Low Frequency Power Amplifier

- 3W Output application
- Collector Power Dissipation $P_C=1\sim 2W$: Mounted on Ceramic Board
- Complement to KSC2883



Marking



Absolute Maximum Ratings $T_a = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{CBO}	Collector-Base Voltage	-30	V
V_{CEO}	Collector-Emitter Voltage	-30	V
V_{EBO}	Emitter-Base Voltage	-5	V
I_C	Collector Current	-1.5	A
I_B	Base Current	-0.3	A
P_C P_C^*	Collector Power Dissipation	500 1,000	mW mW
T_J	Junction Temperature	150	$^\circ\text{C}$
T_{STG}	Storage Temperature	-55 ~ 150	$^\circ\text{C}$

* Mounted on Ceramic Board (250mm² × 0.8mm)

Electrical Characteristics $T_a = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
BV_{CEO}	Collector-Emitter Breakdown Voltage	$I_C = -10\text{mA}$, $I_B = 0$	-30			V
BV_{EBO}	Emitter-Base Breakdown Voltage	$I_E = -1\text{mA}$, $I_C = 0$	-5			V
I_{CBO}	Collector Cut-off Current	$V_{CB} = -30\text{V}$, $I_E = 0$			-100	nA
I_{EBO}	Emitter Cut-off Current	$V_{BE} = -5\text{V}$, $I_C = 0$			-100	nA
h_{FE}	DC Current Gain	$V_{CE} = -2\text{V}$, $I_C = -500\text{mA}$	100		320	
$V_{CE}(\text{sat})$	Collector-Emitter Saturation Voltage	$I_C = -1.5\text{A}$, $I_B = -30\text{mA}$			-2.0	V
$V_{BE}(\text{on})$	Base-Emitter On Voltage	$V_{CE} = -2\text{V}$, $I_C = -500\text{mA}$			-1.0	V
f_T	Current Gain Bandwidth Product	$V_{CE} = -2\text{V}$, $I_C = -500\text{mA}$		120		MHz
C_{ob}	Output Capacitance	$V_{CB} = -10\text{V}$, $I_E = 0$, $f = 1\text{MHz}$			50	pF

h_{FE} Classification

Classification	O	Y
h_{FE}	100 ~ 200	160 ~ 320

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
1203	KSA1203	SOT-89	13"	--	4,000

Typical Performance Characteristics

Figure 1. Static Characteristic

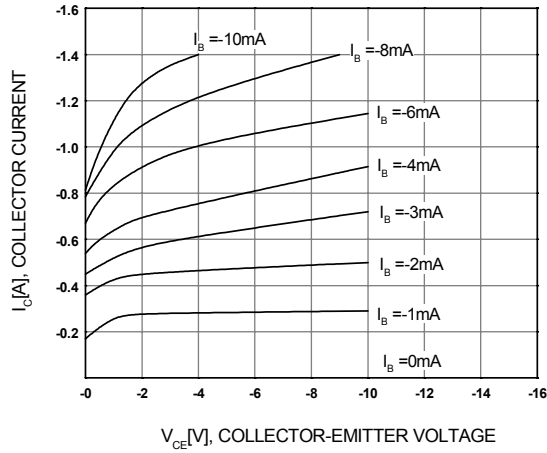


Figure 2. DC Current Gain

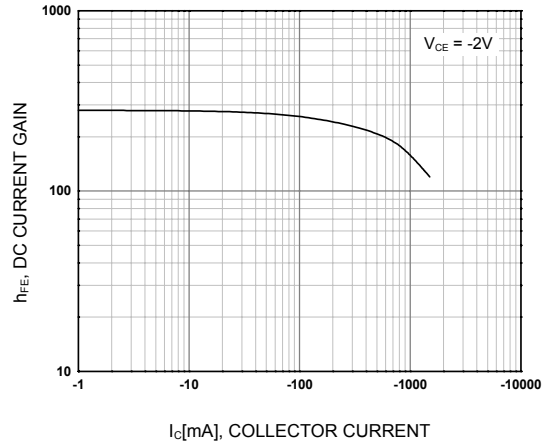


Figure 3. Collector-Emitter Saturation Voltage

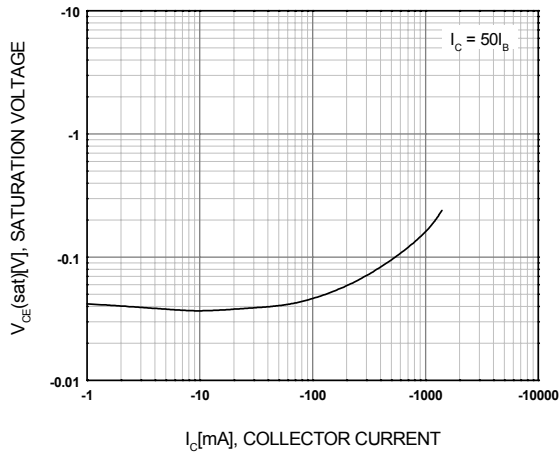


Figure 4. Base-Emitter On Voltage

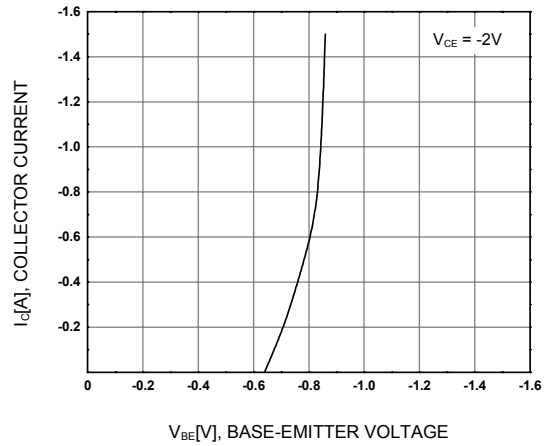


Figure 5. Safe Operating Area

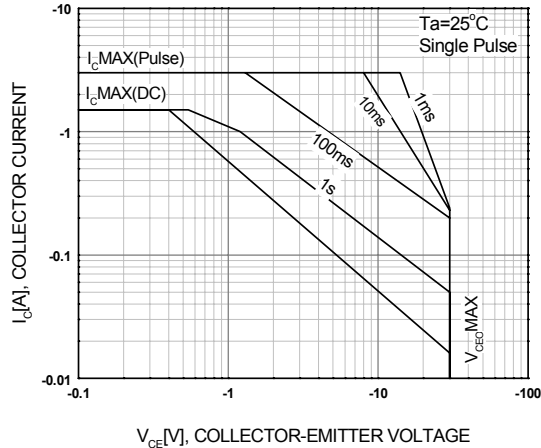
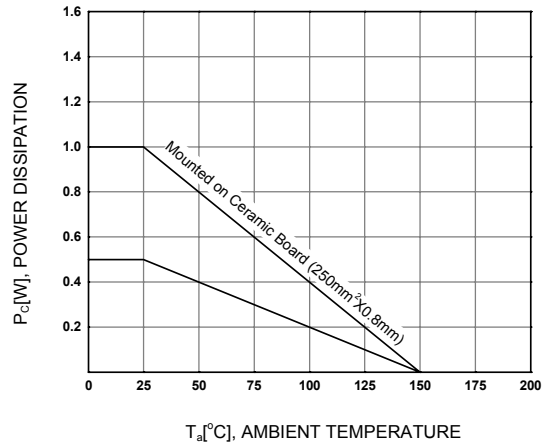


Figure 6. Power Derating



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