

## **AN4003**

### **PC POWER SUPPLY DESIGN WITH KA3511**

**Sang-Tae Im**

#### **1. GENERAL DESCRIPTION**

The KA3511 is a fixed-frequency improved-performance pulse-width modulation control circuit with complete housekeeping circuitry for use in the secondary side of SMPS (Switched mode power supply). It contains various functions, which are precision voltage reference, over voltage protection, under voltage protection, remote on/off control, power good signal generator and etc.

##### **OVP (Over voltage protection) section**

It has OVP functions for +3.3V, +5V, +12V and PT outputs. The circuit is made up of a comparator with four detecting inputs and without hysteresis voltage. Especially, PT (Pin16) is prepared for an extra OVP input or another protection signal.

##### **UVP (Under voltage protection) section**

It also has UVP functions for +3.3V, +5V, +12V outputs. The block is made up of a comparator with three detecting inputs and without hysteresis voltage.

##### **Remote on/off section**

Remote on/off section is used to control SMPS externally. If a high signal is supplied to the remote on/off input, PWM signal becomes a high state and all secondary outputs are grounded. The remote on/off signal is transferred with some on-delay and off-delay time of 8ms, 24ms respectively.

##### **Precision reference section**

The reference voltage trimmed to  $\pm 2\%$  ( $4.9V \leq V_{ref} \leq 5.1V$ )

##### **PG (Power good signal generator) section**

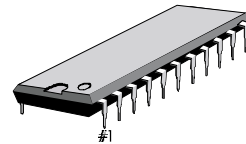
Power good signal generator is to monitor the voltage level of power supply for safe operation of a microprocessor.

KA3511 requires few external components to accomplish a complete housekeeping circuits for SMPS. The KA3511 is available in a 22-pin dual in-line package.

## ORDERING INFORMATION

Device	Package	Operating Temperature
KA3511	22 DIP	-25°C ~ 85°C

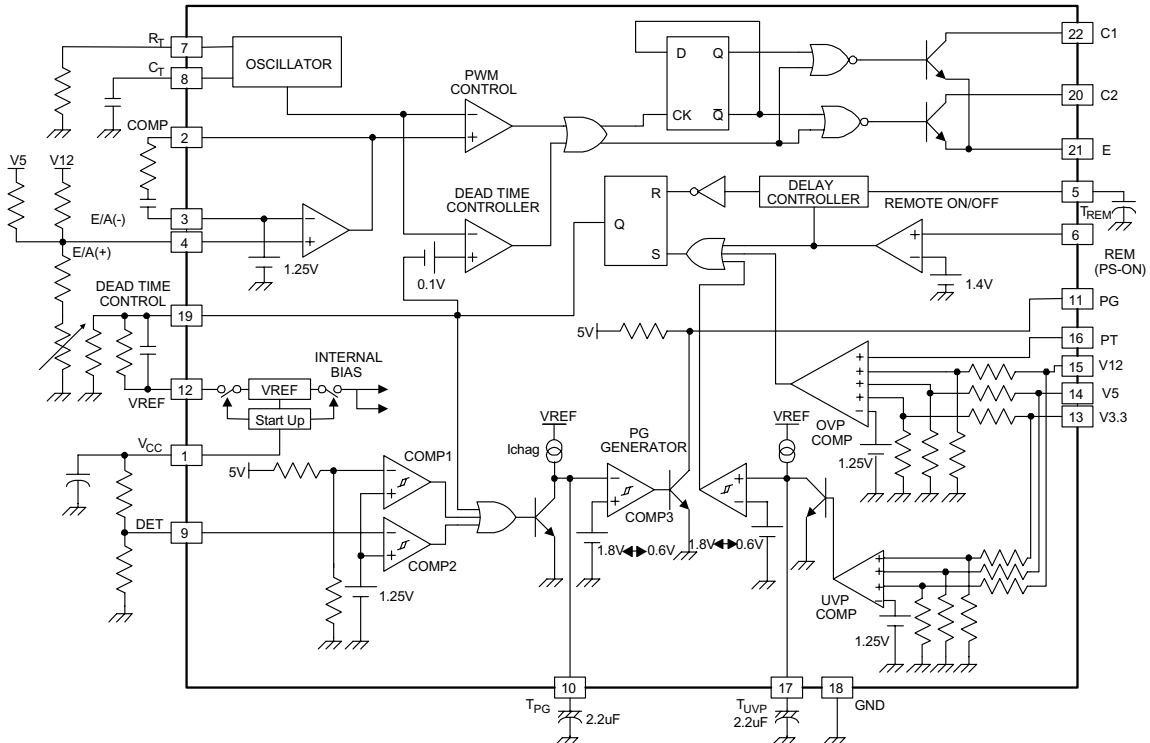
22-DIP-400



## FEATURES

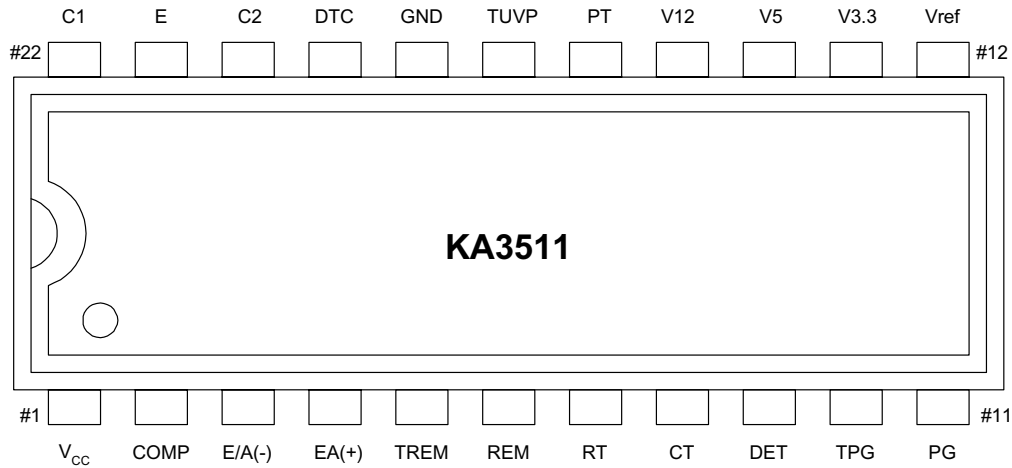
- Complete PWM control and house keeping circuitry
- Few external components
- Precision voltage reference trimmed to 2%
- Dual output for push-pull operation
- Each output TR for 200mA sink current
- Variable duty cycle by dead time control
- Soft start capability by using dead time control
- Double pulse suppression logic
- Over voltage protection for 3.3V / 5V / 12V
- Under voltage protection for 3.3V / 5V / 12V
- One more external input for various protection (PT)
- Remote on/off control function (PS-ON)
- Latch function controlled by remote and protection input
- Power good signal generator with hysteresis
- 22-Pin dual in-line package

## 2. BLOCK DIAGRAM



Rev C, November 1999

### 3. PIN DESCRIPTION



Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	V <sub>CC</sub>	I	Supply voltage	12	Vref	O	Precision reference VTG
2	COMP	O	E/A output	13	V3.3	I	OVP, UVP input for 3.3V
3	E/A(-)	I	E/A (-) input	14	V5	I	OVP, UVP input for 5V
4	E/A(+)	I	E/A (+) input	15	V12	I	OVP, UVP input for 12V
5	TREM	–	Remote on/off delay	16	PT	I	Extra protection input
6	REM	I	Remote on/off input	17	T <sub>UVP</sub>	–	UVP delay
7	RT	–	Oscillation freq. setting R	18	GND	–	Signal ground
8	CT	–	Oscillation freq. setting C	19	DTC	I	Deadtime control input
9	DET	I	Detect input	20	C2	O	Output 2
10	T <sub>PG</sub>	–	PG delay	21	E	–	Power ground
11	PG	O	Power good signal output	22	C1	O	Output 1

Pin No.	Name	Function
1	V <sub>CC</sub>	Supply voltage. Operating range is 14V~30V. V <sub>CC</sub> =20V, Ta=25°C at test.
2	COMP	Error amplifier output. It is connected to non-inverting input of pulse width modulator comparator.
3	E/A(-)	Error amplifier inverting input. Its reference voltage is always 1.25V.
4	E/A(+)	Error amplifier non-inverting input feedback voltage. This pin may be used to sense power supply output voltage.
5	TREM	Remote on/off delay. Ton/Toff=8ms/24ms (Typ.) with C=0.1μF. Its high/low threshold voltage is 1.8V/0.6V.
6	REM	Remote on/off input. It is TTL operation and its threshold voltage is 1.4V. Voltage at this pin can reach normal 4.6V, with absolutely maximum voltage, 5.25V. If REM = "Low", PWM = "Low". That means the main SMPS is operational. When REM = "High", then PWM = "High" and the main SMPS is turned-off.
7	RT	Oscillation frequency setting R. (Test Condition R <sub>T</sub> =10kΩ)
8	CT	Oscillation frequency setting C. (Test Condition C <sub>T</sub> =0.01μF)
9	DET	Under-voltage detect pin. Its threshold voltage is 1.25V Typ.
10	T <sub>PG</sub>	PG delay. Td=250ms (Typ) with C <sub>PG</sub> =2.2μF. The high/low threshold voltage are 1.8V/0.6V and the voltage of Pin10 is clamped at 2.9V for noise margin.
11	PG	Power good output signal. PG = "High" means that the power is "Good" for operation and PG = "Low" means "Power fail".
12	Vref	Precision voltage reference trimmed to 2%. (Typical Value = 5.03V)
13	V3.3	Over voltage protection for output 3.3V. (Typical Value = 4.1V)
14	V5	Over voltage protection for output 5V. (Typical Value = 6.2V)
15	V12	Over voltage protection for output 12V. (Typical Value = 14.2V)
16	PT	This is prepared for an extra OVP input or another protection signal. (Typical Value = 1.25V)
17	T <sub>UVP</sub>	Timing pin for under voltage protection blank-out time. Its threshold voltage is 1.8V and clamped at 2.9V after full charging. Target of delay time is 250ms and it is realized through external (C=2.2μF).
18	GND	Signal ground.
19	DTC	Deadtime control input. The dead-time control comparator has an effective 120mV input offset which limits the minimum output dead time. Dead time may be imposed on the output by setting the dead time control input to a fixed voltage, ranging between 0V to 3.3V.
20	C2	Output drive pin for push-pull operation.
21	E	Power ground.
22	C1	Output drive pin for push-pull operation.

Rev C, November 1999

#### 4. ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply voltage	$V_{CC}$	40	V
Collector output voltage	$V_{C1}, V_{C2}$	40	V
Collector output current	$I_{C1}, I_{C2}$	200	mA
Power dissipation	$P_D$	1	W
Operating temperature	$T_{OPR}$	-25 to 85	°C
Storage temperature	$T_{STG}$	-65 to 150	°C

#### TEMPERATURE CHARACTERISTICS

Characteristic	Symbol	Value			Unit
		Min.	Typ.	Max.	
Temperature coefficient of Vref ( $-25\text{ }^{\circ}\text{C} \leq T_a \leq 85\text{ }^{\circ}\text{C}$ )	$\Delta V_{ref}/\Delta T$	–	0.01	–	%/°C

## 5. ELECTRICAL CHARACTERISTICS ( $V_{CC}=20V$ , $T_A=25^{\circ}C$ )

Characteristic	Symbol	Test Condition	Value			Unit
			Min.	Typ.	Max.	
REFERENCE SECTION						
Reference output voltage	Vref	Iref=1mA	4.9	5	5.1	V
Line regulation	ΔVref.LINE	14V≤VCC≤30V	–	2.0	25	mV
Load regulation	ΔVref.LOAD	1mA≤Iref≤10mA	–	1.0	15	mV
Temperature coefficient of Vref <sup>(1)</sup>	ΔVref/ΔT	-25°C≤Ta≤85°C	–	0.01	–	%/°C
Short-circuit output current	ISC	Vref=0	15	35	75	mA
OSCILLATOR SECTION						
Oscillation frequency	fosc	CT=0.01μF, RT=12k	–	10	–	kHz
Frequency change with temperature <sup>(1)</sup>	fosc/T	CT=0.01μF, RT=12k	–	2	–	%
DEAD TIME CONTROL SECTION						
Input bias current	IB(DT)		–	-2.0	-10	μA
Maximum duty voltage	DCMAX	Pin19 (DTC)=0V	45	48	50	%
Input threshold voltage	VTH(DT)	Zero Duty Cycle	–	3.0	3.3	V
		Max. Duty Cycle	0	–	–	
ERROR AMP SECTION						
Inverting reference voltage	Vref(EA)		1.20	1.25	1.30	%
Input bias current	IB(EA)	VCOMP=2.5V	–	-0.1	-1.0	μA
Open-loop voltage gain <sup>(1)</sup>	GVO	0.5V≤VCOMP≤3.5V	70	95	–	dB
Unit-gain bandwidth <sup>(1)</sup>	BW		–	650	–	kHz
Output sink current	ISINK	VCOMP=0.7V	0.3	0.9	–	mA
Output source current	ISOURCE	VCOMP=3.5V	-2.0	-4.0	–	mA
PWM COMPARATOR SECTION						
Input threshold voltage	VTH(PWM)	Zero Duty Cycle	–	4	4.5	V
OUTPUT SECTION						
Output saturation voltage	VCE(SAT)	IC=200mA	–	1.1	1.3	V
Collector off-state current	IC(off)	VCC=VC=30V, VE=0V	–	2	100	μA
Rising time	TR		–	100	200	ns
Falling time	TF		–	50	200	ns
PROTECTION SECTION						
Over voltage protection for 3.3V	VOVP1		3.8	4.1	4.3	V

Rev C, November 1999

## 5. ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Test Condition	Value			Unit
			Min.	Typ.	Max.	
Over voltage protection for 5V	V <sub>OVP2</sub>	–	5.8	6.2	6.6	V
Over voltage protection for 12V	V <sub>OVP3</sub>	–	13.5	14.2	15.0	V
Input threshold voltage for PT	V <sub>PT</sub>	–	1.20	1.25	1.30	
Under voltage protection for 3.3V	V <sub>UVP1</sub>	–	2.1	2.3	2.5	V
Under voltage protection for 5V	V <sub>UVP2</sub>	–	3.7	4.0	4.3	V
Under voltage protection for 12V	V <sub>UVP3</sub>	–	9.2	10	10.8	V
Charging current for UVP delay	I <sub>CHG.UVP</sub>	C=2.2μF, V <sub>TH</sub> =1.8V	-10	-15	-23	μA
UVP Delay Time	T <sub>D.UVP</sub>	C=2.2μF	100	260	500	ms
<b>REMOTE ON/OFF SECTION</b>						
REM on input voltage	V <sub>REMH</sub>	I <sub>REM</sub> = -200μA	2.0	–	–	V
REM off input voltage	V <sub>REML</sub>	–	–	–	0.8	V
REM off input bias voltage	I <sub>REML</sub>	V <sub>REM</sub> =0.4V	–	–	-1.6	mA
REM on open voltage	V <sub>REM(OPEN)</sub>	–	2.0	–	5.25	V
REM on delay time	T <sub>on</sub>	C=0.1μF	4	8	14	ms
REM off delay time	T <sub>off</sub>	C=0.1μF	16	24	34	ms
<b>REMOTE ON/OFF SECTION<sup>(2)</sup></b>						
Detecting input voltage	V <sub>IN(DET)</sub>	–	1.20	1.25	1.30	V
Detecting V5 voltage	V <sub>5(DET)</sub>	–	4.1	4.3	4.5	V
Hysteresis voltage 1	HY1	COMP1, 2	10	40	80	mV
Hysteresis voltage 2	HY2	COMP3	0.6	1.2	–	V
PG output load resistor	R <sub>PG</sub>	–	0.5	1	2	kΩ
Charging current for PG delay	I <sub>CHG.PG</sub>	C=2.2μF, V <sub>TH</sub> =1.8V	-10	-15	-23	μA
PG delay time	T <sub>D.PG</sub>	C=2.2μF	100	260	500	ms
PG output saturation voltage	V <sub>SAT(PG)</sub>	I <sub>PG</sub> =10mA	–	0.4	0.2	V
<b>TOTAL DEVICE</b>						
Standby supply current	I <sub>CC</sub>	–	–	10	20	mA

### Notes:

- These Parameters, although guaranteed over their recommended operating conditions are not 100% tested in production.
- REM on delay time (Pin6 REM: “L” → “H”),  
REM off delay time (Pin6 REM: “H” → “L”)

## 6. BLOCK DESCRIPTION & APPLICATION INFORMATION

### 6.1 OSCILLATOR BLOCK

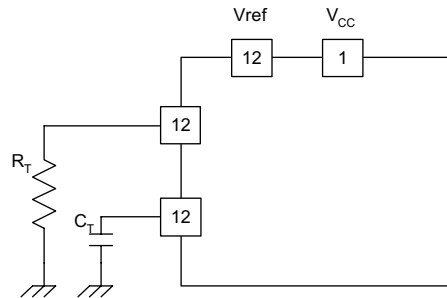


Figure 1. Oscillator  $R_T$ ,  $C_T$

The KA3511 is a fixed-frequency pulse width modulation control circuit. An internal-linear sawtooth oscillator is frequency-programmable by two external components,  $R_T$  and  $C_T$ . The oscillator frequency is determined by

$$f_{osc} = \frac{1.1}{R_T \times C_T}$$

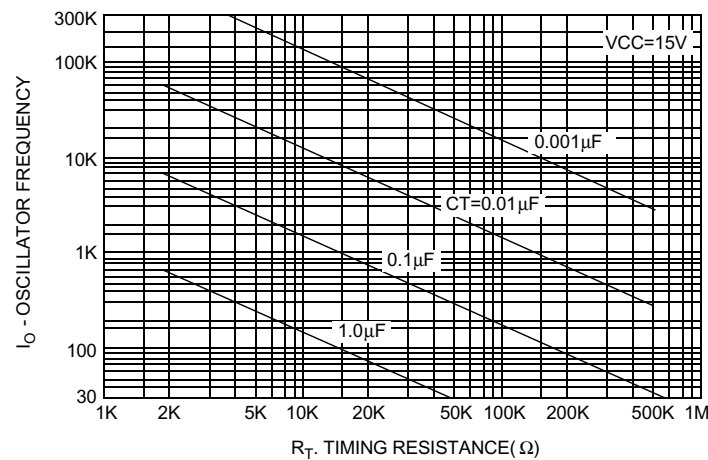


Figure 2. Oscillator Frequency vs. Timing Resistance

### 6.2 PWM CONTROL BLOCK

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor  $C_T$  to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip-flop clock-input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the timing diagram shown in Figure 4)

Rev C, November 1999



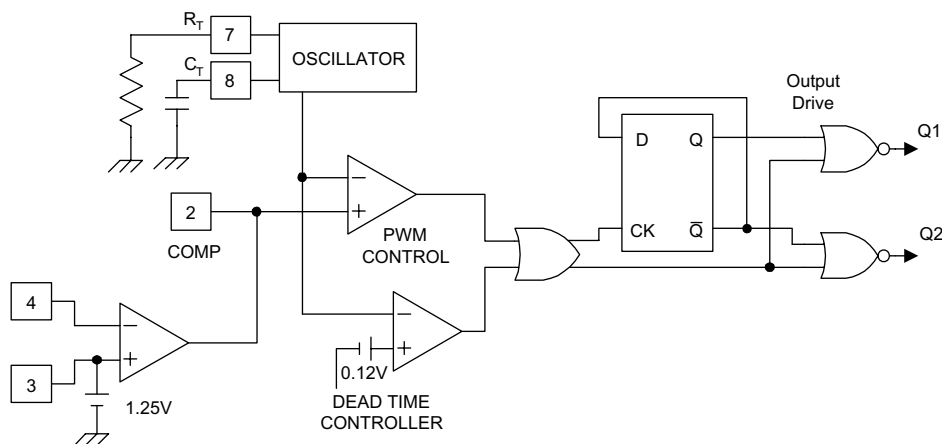


Figure 3. PWM Control Block

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feedback input. The dead-time control comparator has an effective 120mV input offset which limits the minimum output dead time. Dead time may be imposed on the output by setting the dead time control input to a fixed voltage, ranging between 0V to 3.3V.

The pulse width modulator comparator provides a means for the error amplifier to adjust the output pulse width from the maximum percent on-time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5V to 3.5V. The error amplifier may be used to sense power-supply output voltage, and its output is connect to noninverting input of the pulse width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

When capacitor  $C_T$  is discharged, a positive pulse is generated on the output of the dead time comparator, which clocks the pulse-steering flip-flop and inhibits the output transistors, Q1 and Q2. The pulse-steering flip-flop directs the modulated pulses to each of the two output transistors always for push-pull operation. The output frequency is equal to half that of the oscillator.

The KA3511 has an internal 5.0V reference capable of sourcing up to 10mA of load current for external bias circuits. The reference has an internal accuracy of  $\pm 2\%$  with typical thermal drift of less than 50mV over an operating temperature range of  $-25^\circ\text{C}$  to  $85^\circ\text{C}$

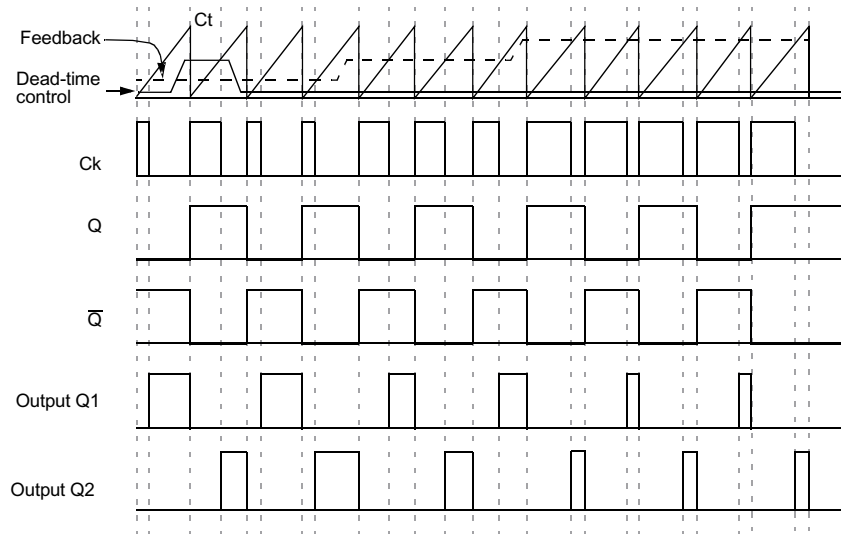


Figure 4. Operating Waveform

### 6.3 DEADTIME CONTROL for SOFT-START

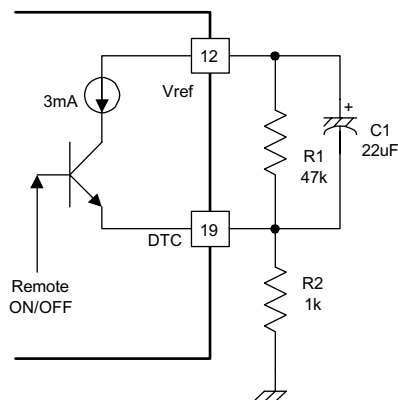


Figure 5. Soft-Start Circuit

Deadtime control for soft-start makes a power supply output rising time (Typ. 15ms) to reduce output ringing voltage for 3.3V, 5V, and 12V. If output rising time is too fast, output ringing voltage reaches OVP level.

You can make a soft start function by add external components R1, R2 and C1 (refer to figure 5). At first the main power is turned-on, the deadtime control voltage keeps high state ( = 3V), and then go to the low voltage( = 105mV) that divided by R1, R2.

$$V_{DTC\ LOW} = \frac{R2}{R1 + R2} \times V_{ref}(5V) = 104.9mV$$

So Output Duty Ratio will change from the minimum duty ratio to the maximum duty ratio.

Also, if the remote voltage is high, the deadtime control voltage will keep 3V ( $=3\text{mA} \times R2 (1\text{k}\Omega)$ ) by the internal 3mA current source for soft start. Therefore, when the remote voltage is low, the deadtime control voltage will be changed from 3V to almost ground potential. And its soft start time dependent on external capacitor C1.

## 6.4 OUTPUT VOLTAGE REGULATION

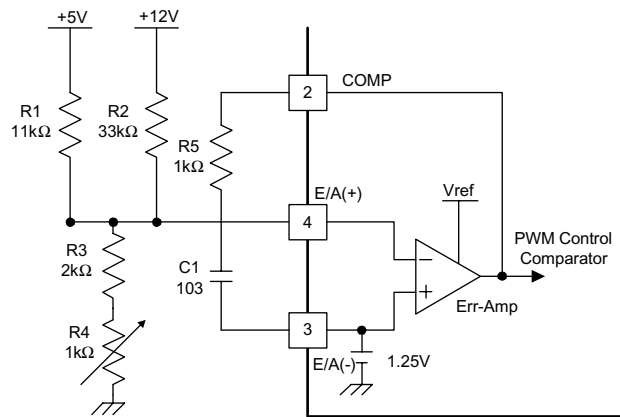


Figure 6. Output Regulation Circuit

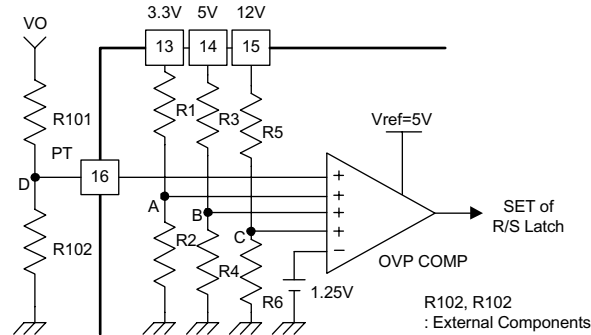
+5V/+12V output voltages are determined by resistor ratio of R1,R2,R3 and R4. The resistor value can be changed by set condition and requirements.

R5, C1 are the compensation circuit for stability.

If output voltage (+5V or +12V) is increase, duty ratio of main power switch will be reduced by PWM control comparator signal and error amplifier output. Therefore the output voltage will be reduced.

On the contrary, if output voltage (+5V or +12V) is reduce, duty ratio of main power switch will be increased by PWM control comparator signal and error amplifier output. Therefore the output voltage will be increased. So the output voltage of power supply will be regulated.

## 6.5 OVP BLOCK



OVP function is simply realized by connecting Pin13, Pin14, Pin15 to each secondary output. R1, 2, 3, 4, 5, 6 are internal resistors of the IC. Each OVP level is determined by resistor ratio and the typical values are 4.1V/6.2V/14.2V.

### OVP Detecting voltage for +3.3V

$$V_{OVP1}(+3.3V) = \frac{R_1 + R_2}{R_2} \times V_A = \frac{R_1 + R_2}{R_2} \times V_{ref} = 4.1V$$

### OVP Detecting voltage for +5V

$$V_{OVP2}(+5V) = \frac{R_3 + R_4}{R_4} \times V_B = \frac{R_3 + R_4}{R_4} \times V_{ref} = 6.2V$$

### OVP Detecting voltage for +12V

$$V_{OVP3}(+12V) = \frac{R_5 + R_6}{R_6} \times V_C = \frac{R_5 + R_6}{R_6} \times V_{ref} = 14.2V$$

Especially, pin16 (PT) is prepared for extra OVP input or another protection signal. That is, if you want over voltage protection of extra output voltage, then you can make a function with two external resistors.

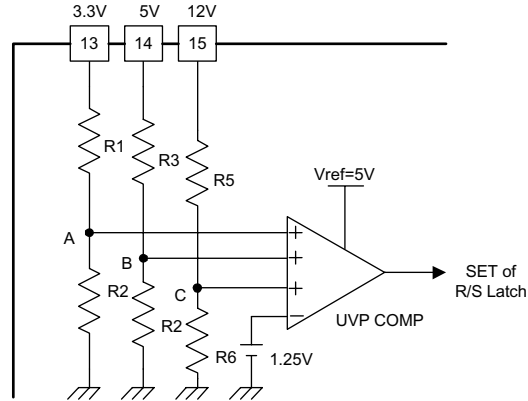
### OVP Detecting voltage for PT

$$V_{PT} = \frac{R_{101} + R_{102}}{R_{102}} \times V_D = \frac{R_{101} + R_{102}}{R_{102}} \times V_{ref}$$

In the case of OVP, system designer should know a fact that the main power can be dropped after a little time because of system delay, even if PWM is triggered by OVP.

So when the OVP level is tested with a set, you should check the secondary outputs (+3.3V/+5V/+12V) and PG (Pin11) simultaneously. you can know the each OVP level as checking each output voltage in just time that PG (Pin11) is triggered from high to low.

## 6.6 UVP BLOCK



The KA3511 has UVP functions for +3.3V, +5V, +12V Outputs. The block is made up of three input comparators. Each UVP level is determined by resistor ratio and the typical values are 2.3V/4V/10V.

### UVP Detecting voltage for +3.3V

$$V_{\text{UVP } 1}(+3.3\text{V}) = \frac{R_1 + R_2}{R_2} \times V_A = \frac{R_1 + R_2}{R_2} \times V_{\text{ref}} = 2.3\text{V}$$

### UVP Detecting voltage for +5V

$$V_{\text{UVP } 2}(+5\text{V}) = \frac{R_1 + R_2}{R_2} \times V_A = \frac{R_1 + R_2}{R_2} \times V_{\text{ref}} = 4\text{V}$$

### UVP Detecting voltage for +12V

$$V_{\text{UVP } 3}(+12\text{V}) = \frac{R_1 + R_2}{R_2} \times V_A = \frac{R_1 + R_2}{R_2} \times V_{\text{ref}} = 10\text{V}$$

## 6.7 REMOTE ON/OFF & DELAY BLOCK

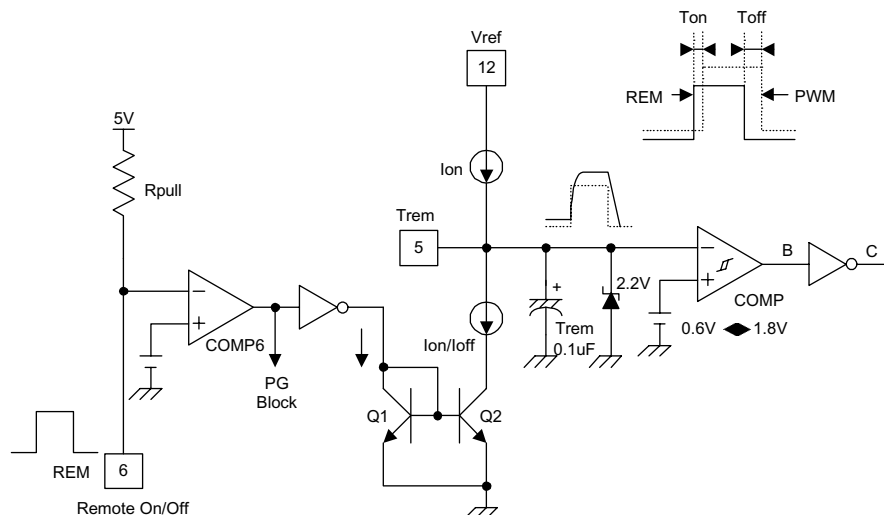


Figure 9. Remote ON/OFF Delay Block

Remote ON/OFF section is controlled by a microprocessor. If a high signal is supplied to the remote ON/OFF input (Pin6), the output of COMP6 becomes high status. The output signal is transferred to ON/OFF delay block and PG block.

If no signal is supplied to Pin6, Pin6 maintains high status (=5V) for Rpull.

When Remote ON/OFF is high, it produces PWM (Pin6) “High” signal after ON delay time (about 8ms) for stabilizing system.

Then, all outputs (+3.3V, +5V, +12V) are grounded.

When Remote ON/OFF is changed to “Low”, it produces PWM “Low” signal after OFF delay time (about 24ms) for stabilizing the system.

If REM is low, then PWM is low. That means the main SMPS is operational. When REM is high, PWM is high and the main SMPS is turned-off.

ON/OFF delay Time can be calculated by following equation.

$$T_{on} = K_1 \times \frac{C_{trem} \times \Delta V_{on}}{I_{on}} \approx 0.95 \times \frac{0.1 \mu F \times 2V}{23 \mu A} = 8.2 \text{ msec}$$

$$T_{off} = K_2 \times \frac{C_{trem} \times \Delta V_{off}}{I_{off}} \approx 0.8 \times \frac{0.1 \mu F \times 2.1 V}{8 \mu A} = 24 \text{ msec}$$

(K1, K2: Constant value gotten by test)

In above equation, typical capacitor value is 0.1uF. If the capacitor is changed to larger value, it can cause malfunction in case of AC power on at remote High. Because PWM maintains low status and main power turns on for on delay time. So you should use 0.1uF or smaller capacitor.

## 6.8 R/S FLIP FLOP (LATCH) BLOCK

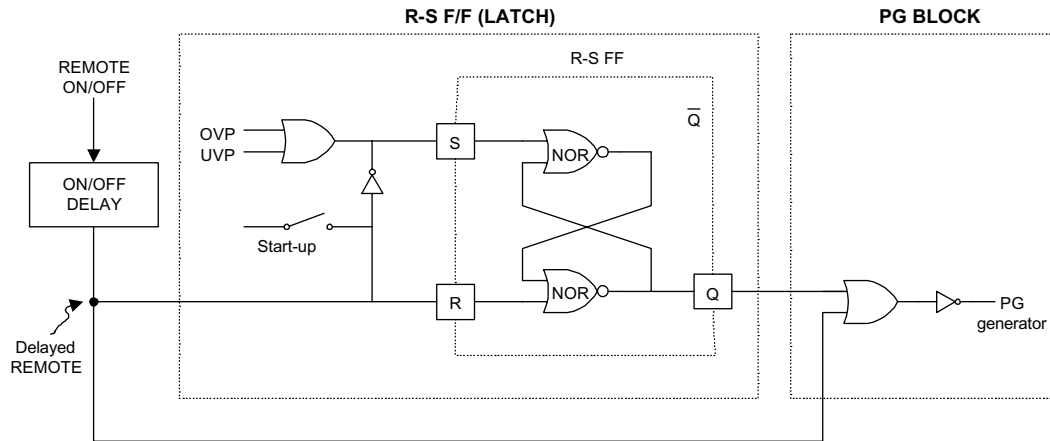


Figure 10. R-S F/F Block Diagram

OVP+	SET	RESET	Qn+1	Qn+1
Low	Low	Low	Qn	Qn
Low	Low	High	High	High
High	High	Low	High	Low
High	Low	High	Low	High

There is a R-S F/F (Latch) circuit for shutdown operation in the KA3511. R-S F/F (Latch) is controlled by OVP, UVP, and some delayed remote ON/OFF signal.

If any output of OVP or UVP is High, SET signal of R-S F/F is high status and it produces PWM "High" and main power is turned off. When remote signal is high, its delayed output signal is supplied to RESET port of R-S F/F and it produces SET low. So output Q is low status. At this time, PWM maintains high status by delayed remote high signal.

After main power is turned-off by OVP/UVP and initialized by remote, if remote signal is changed to low, main power becomes operational.

When you test KA3511, Remote ON/OFF signal should be toggled once for initializing.

## 6.9 POWER GOOD SIGNAL GENERATOR

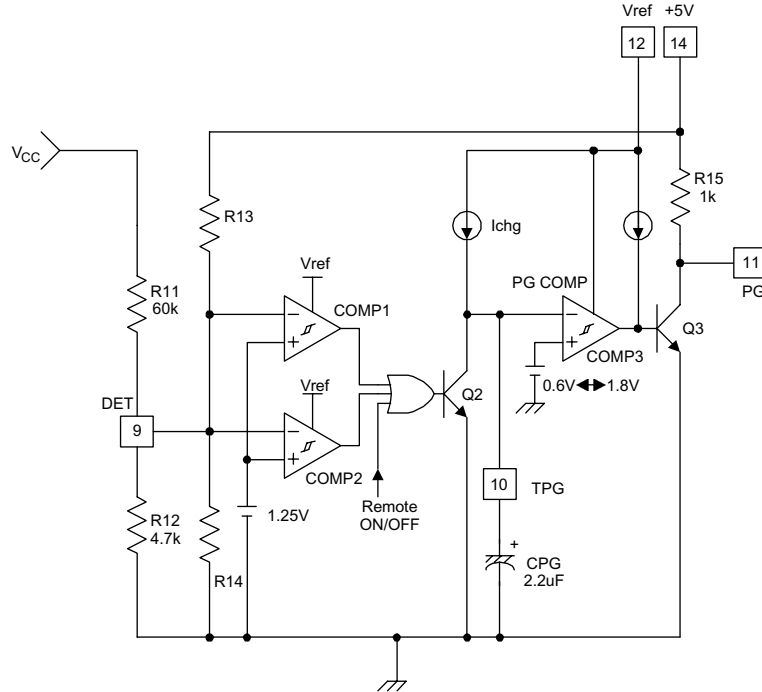


Figure 11. PG Signal Generator Block

Power good signal generator circuits generate “ON & OFF” signal depending on the status of output voltage to prevent the malfunctions of following systems like microprocessor and etc. from unstable outputs at power on & off. At power on, it produces PG “High” signal after some delay (about 250ms) for stabilizing outputs.

At power off, it produces PG “Low” signal without delay by sensing the status of power source for protecting following systems.  $V_{CC}$  detection point can be calculated by following equation. recommended values of R11, R12 are external components.

$$V_{DET} = 1.25V \times \left(1 + \frac{R11}{R12}\right) = 17.2V$$

COMP3 creates PG “Low” without delay when +5V output falls to less than 4.3V to prevent some malfunction at transient status, thus it improves system stability.

When remote On/Off signal is high, it generates PG “Low” signal without delay. It means that PG becomes “Low” before main power is grounded.

PG delay time ( $T_d$ ) is determined by capacitor value, threshold voltage of COMP3 and the charging current and its equation is as following.

$$T_d = \frac{\Delta V}{I_{chg}} \approx \frac{PG \times V_{th}}{I_{chg}} = \frac{2.2\mu F \times 2V}{18\mu A} \approx 250ms$$



Considering the lightning surge and noise, there are two types of protections. One is a few seconds delay between TPG and PG for safe operation and another is some noise margin of Pin10.

$$\text{Noise\_Margin\_of\_T}_{\text{PG}} = V_{10}(\text{max}) - V_{\text{th}}(\text{L}) = 2.9\text{V} - 0.6\text{V} = 2.3\text{V}$$

## 7. ABOUT TEST METHOD

You can verify the KA3511 with a SMPS set. But you should pay attention to the device damage problem by increasing  $V_{\text{CC}}$ . You should remove the sub-board after +5Vsb drops to 0V and  $V_{\text{CC}}$  of KA3511 is grounded and then fan stops under the Remote Low.

- OVP function of +3.3V/+5V/+12V

You can test OVP for +3.3V/+5V/+12V by shorting Pin16 and Pin17 to GND.

- UVP function of +3.3V/+5V/+12V

You can simply test UVP for +3.3V/+5V/+12V by shorting Pin16 to GND.

- OVP input threshold voltage for PT

The test condition is remote “Low” and you increase the supply voltage of pin16 using a DC power supply. When the voltage is over  $1.2 \times V$ , main power supply will shutdown. So, you can measure the shutdown point of main power supply, and that will be a OVP input threshold voltage for PT.

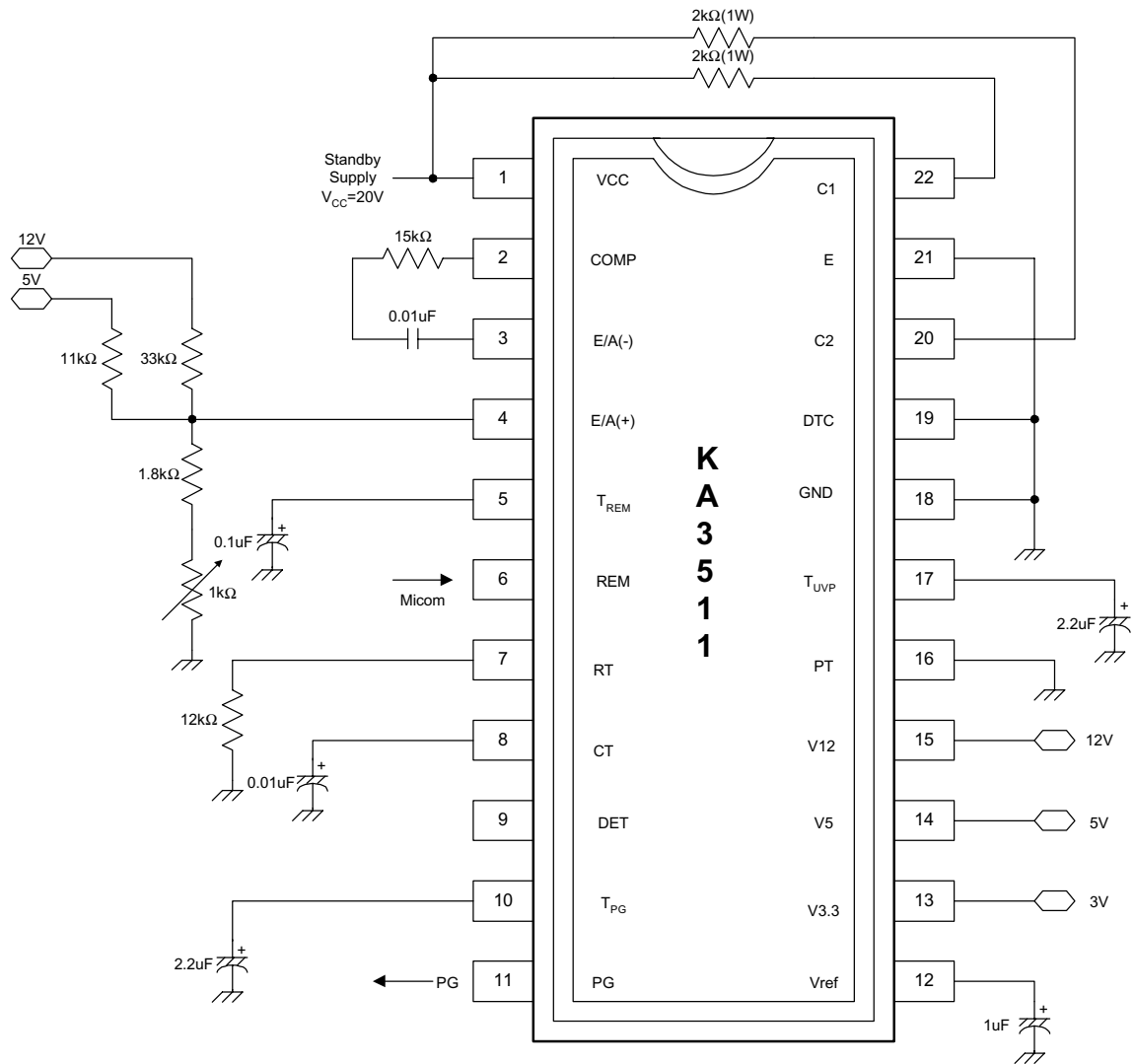
- Remote On/Off delay time

You can measure the time difference of remote On/Off and the main power supply output as toggling the remote On/Off.

- PG delay time

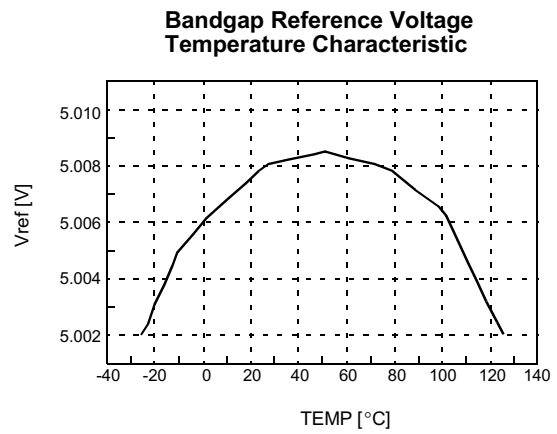
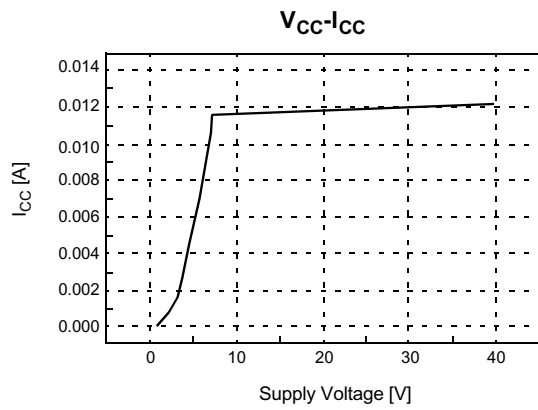
In AC power-on time, secondary outputs are turned on and then after some delay time PG output is triggered from low to high. You can measure the time difference of +5V and PG in turn-on time.

## 8. HOUSE KEEPING CIRCUIT

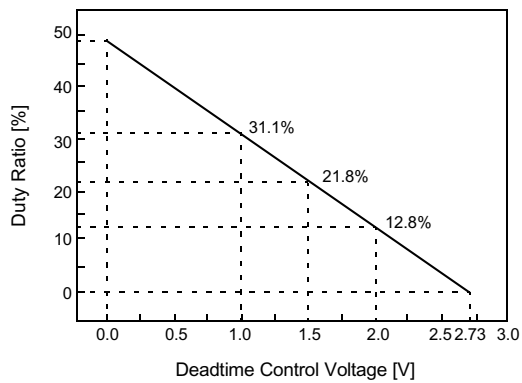


Using the KA3511 requires few external components to accomplish a complete housekeeping circuits for SMPS.

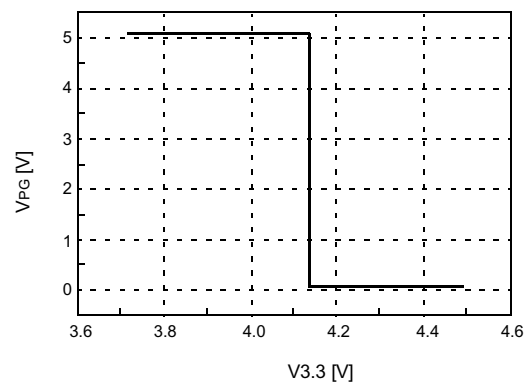
## 9. TYPICAL CHARACTERISTICS



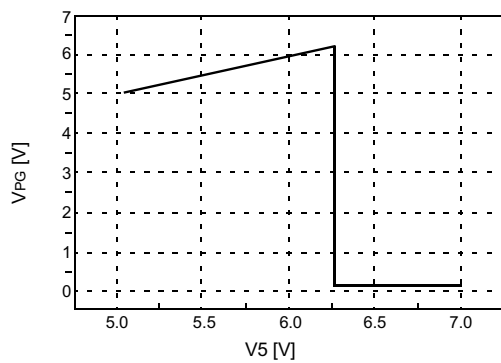
**PIN19(Dead Time Control Voltage)-Duty Cycle**



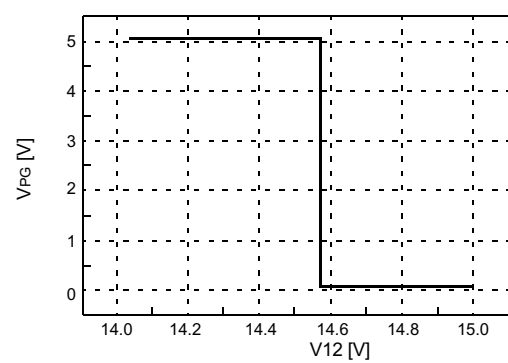
**OVP for 3.3V**

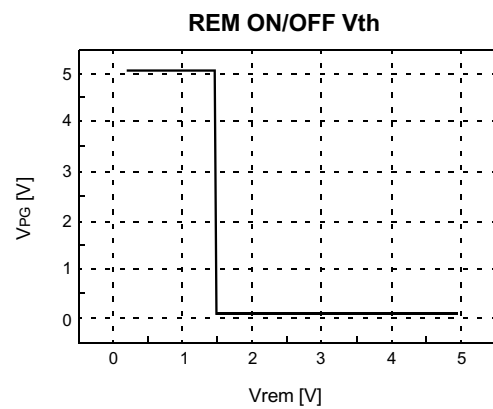
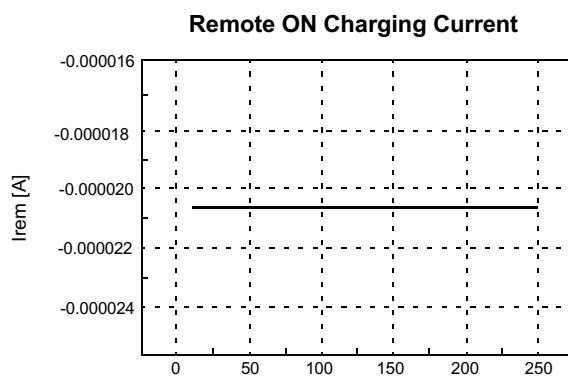
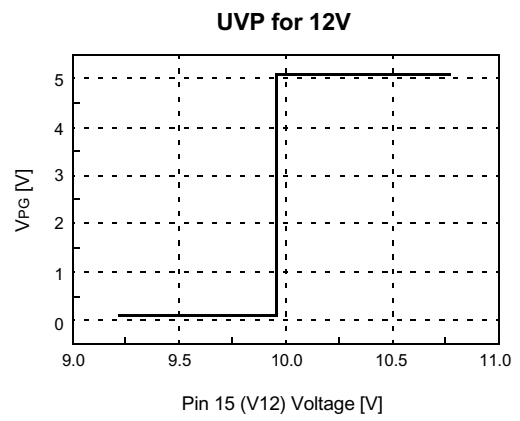
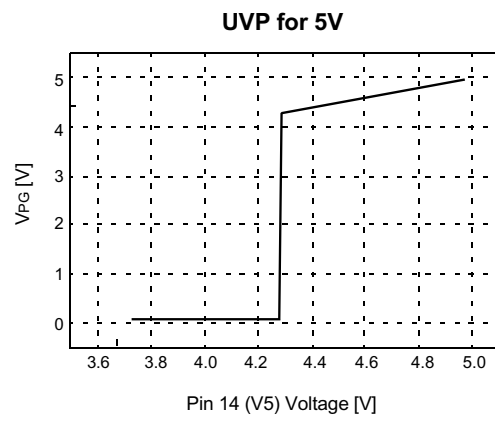
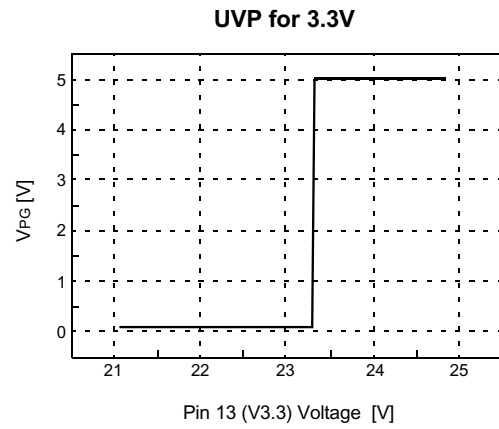
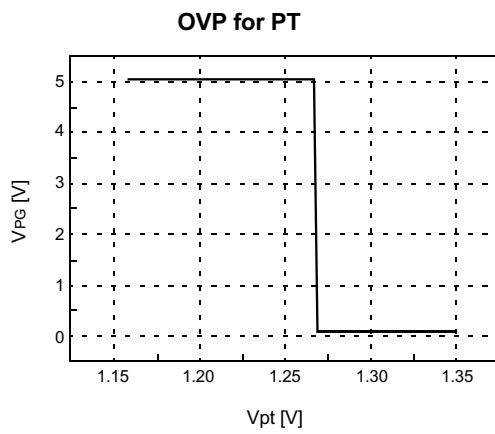


**OVP for 5V**

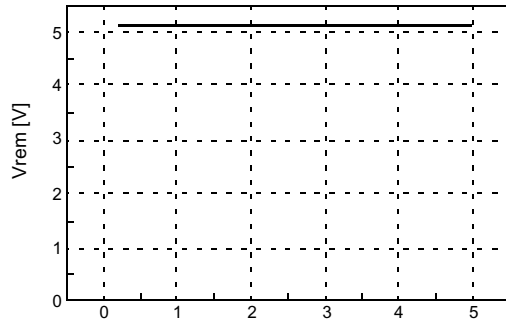


**OVP for 12V**

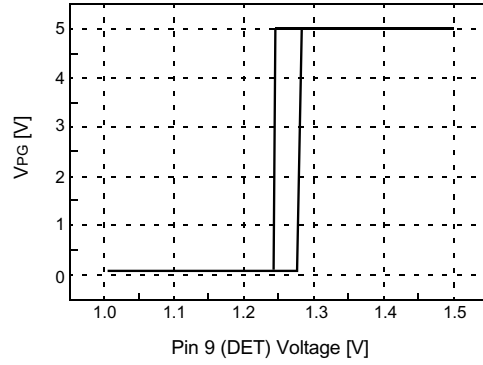




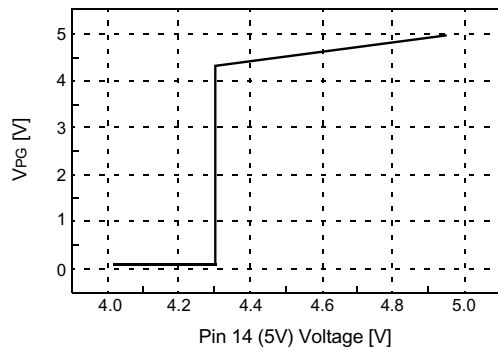
**Remote ON Open Voltage**



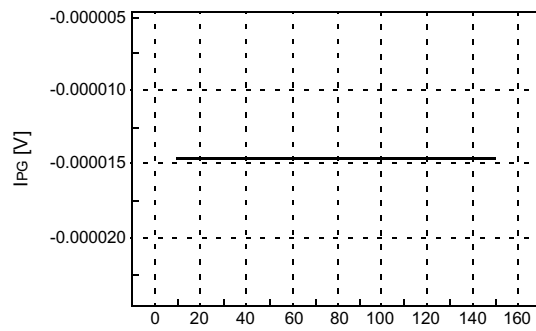
**Detecting  $V_{CC}$  Voltage (DET)**



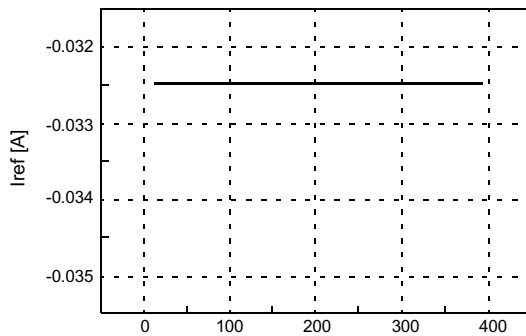
**Detecting V5 Voltage**



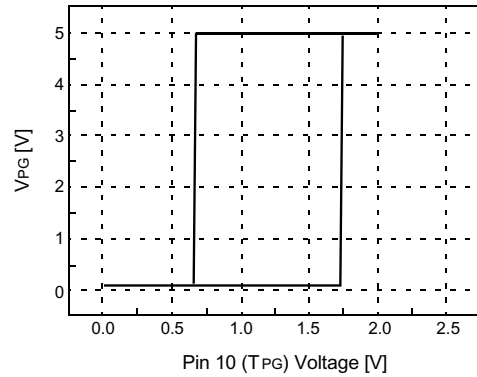
**Charging Current for PG**



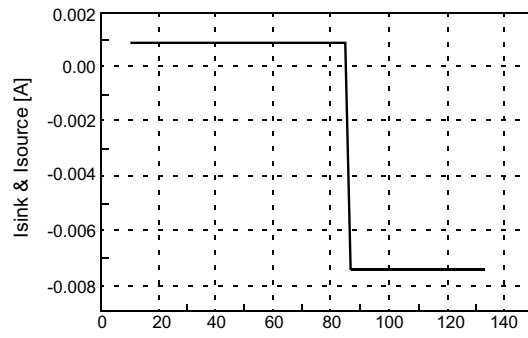
**Short Circuit Current**



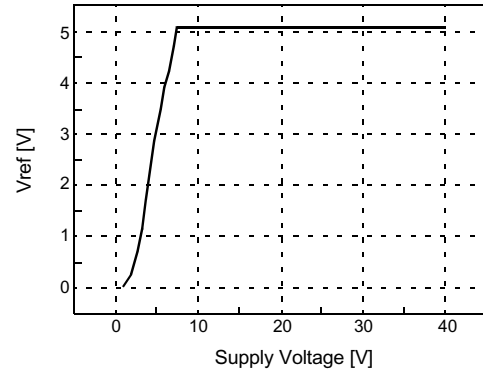
**Hysteresis Voltage 2**



**Error Amp Sink Current**

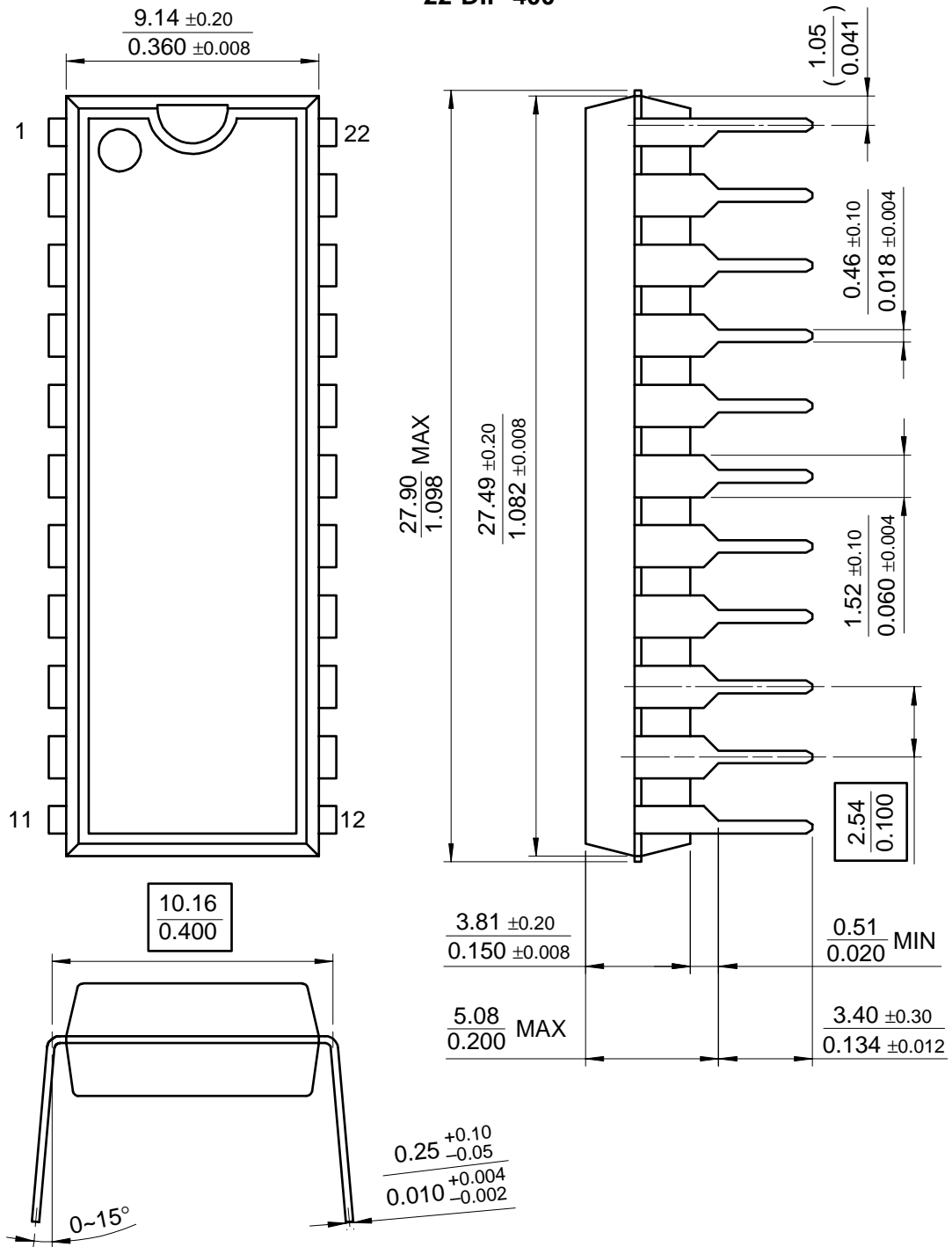


**Reference Voltage**



## 10. PACKAGE DIMENSION

### 22-DIP-400



Rev C, November 1999

## 11. EXPERIMENTAL RESULT

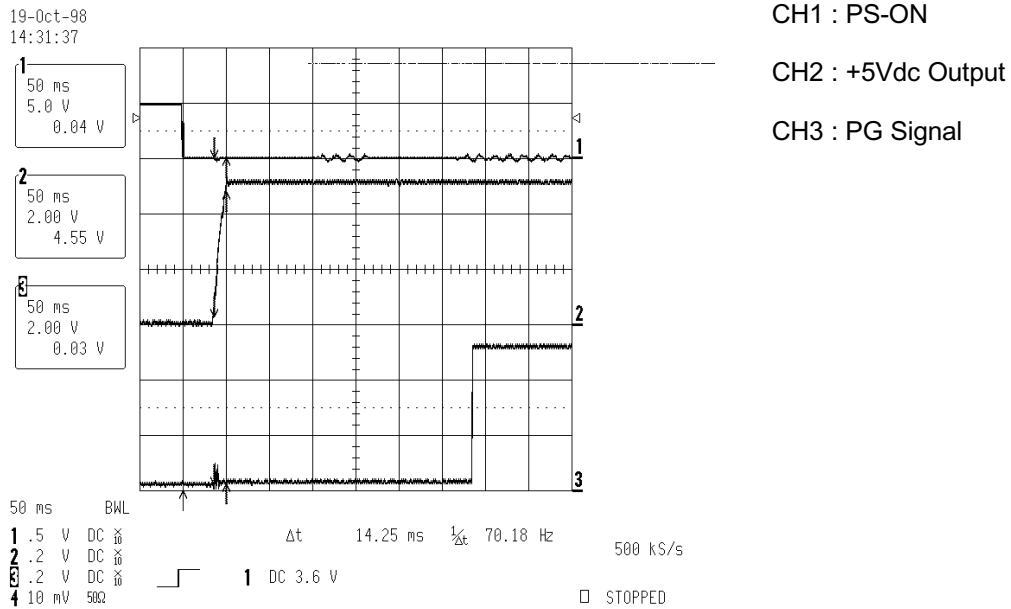


Figure 12. Rising Time of +5Vdc Output Voltage

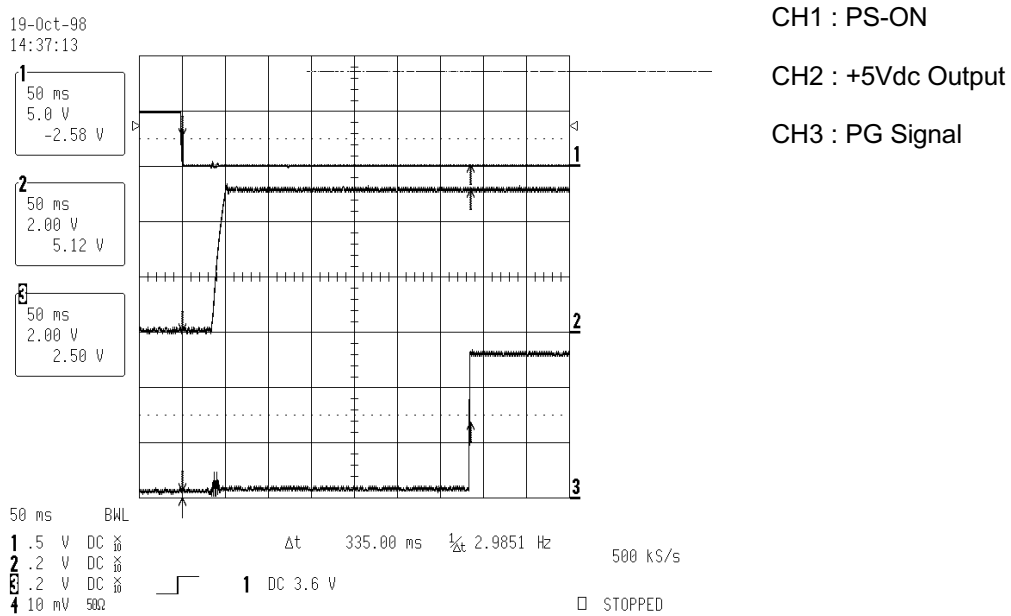


Figure 13. PG Signal Delay Time



19-Oct-98  
14:41:17

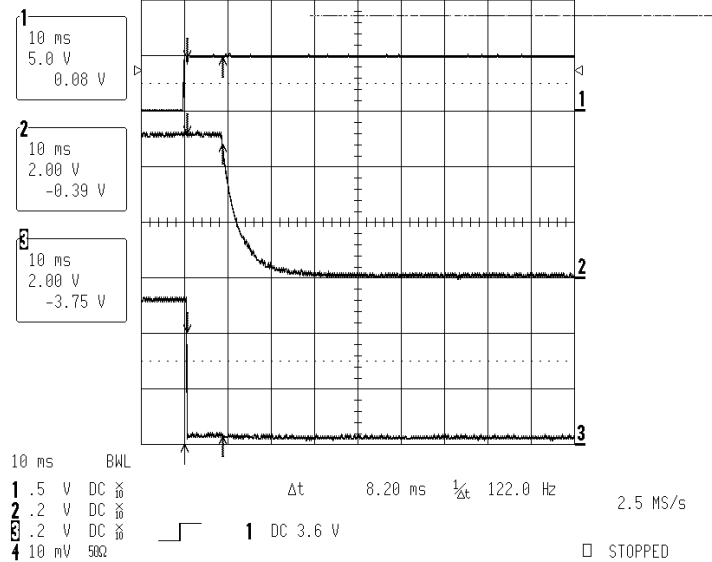


Figure 14. Power Down Warning

19-Oct-98  
15:06:51

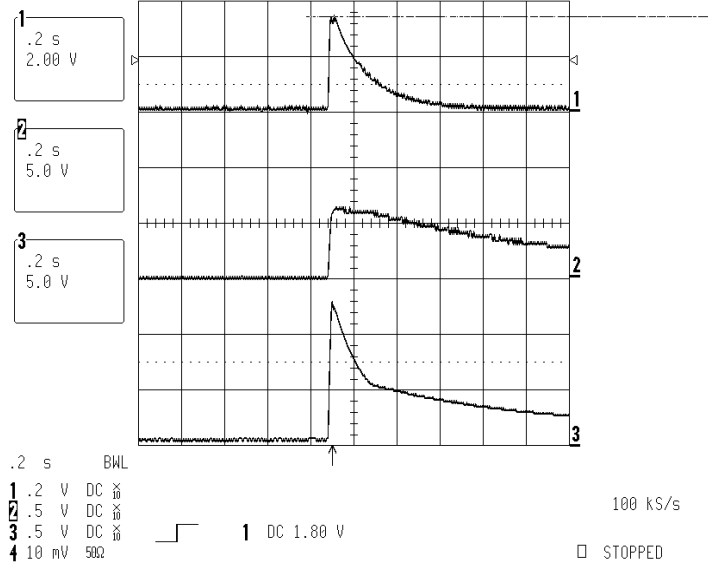


Figure 15. No Load Protection

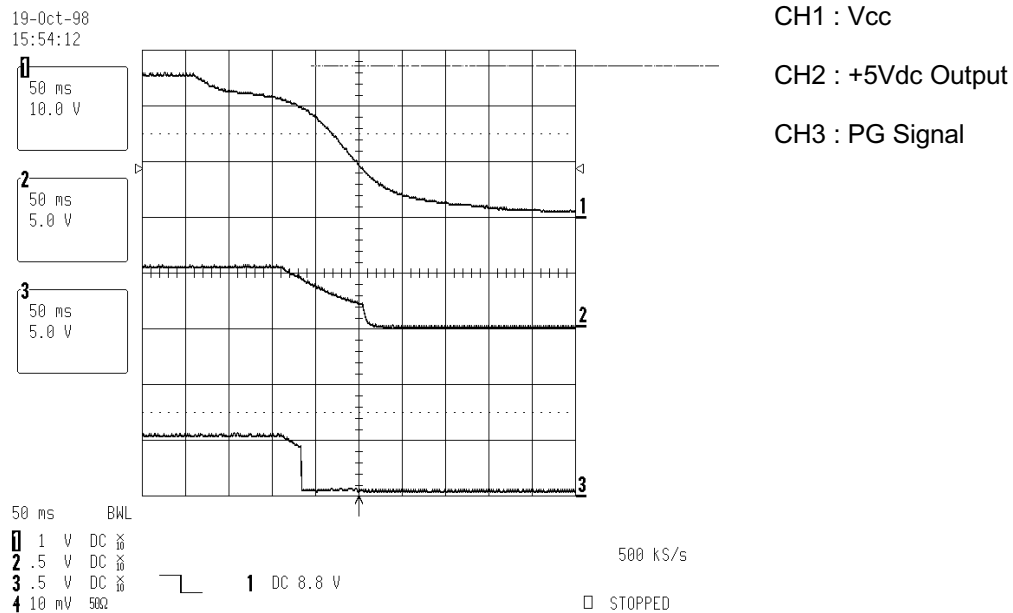


Figure 16. Vcc, +5Vdc Output vs. PG Signal (High)

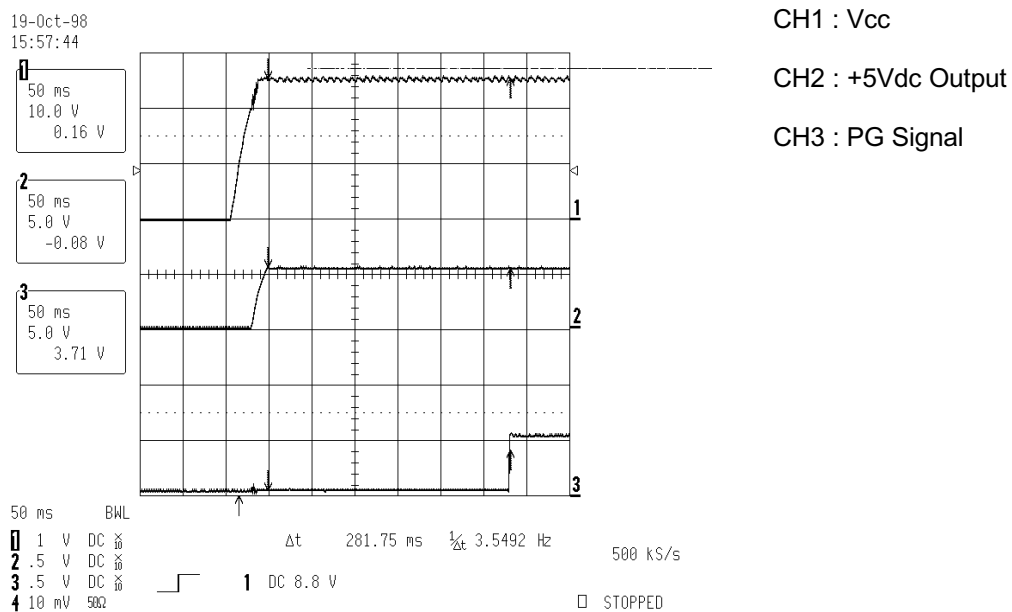
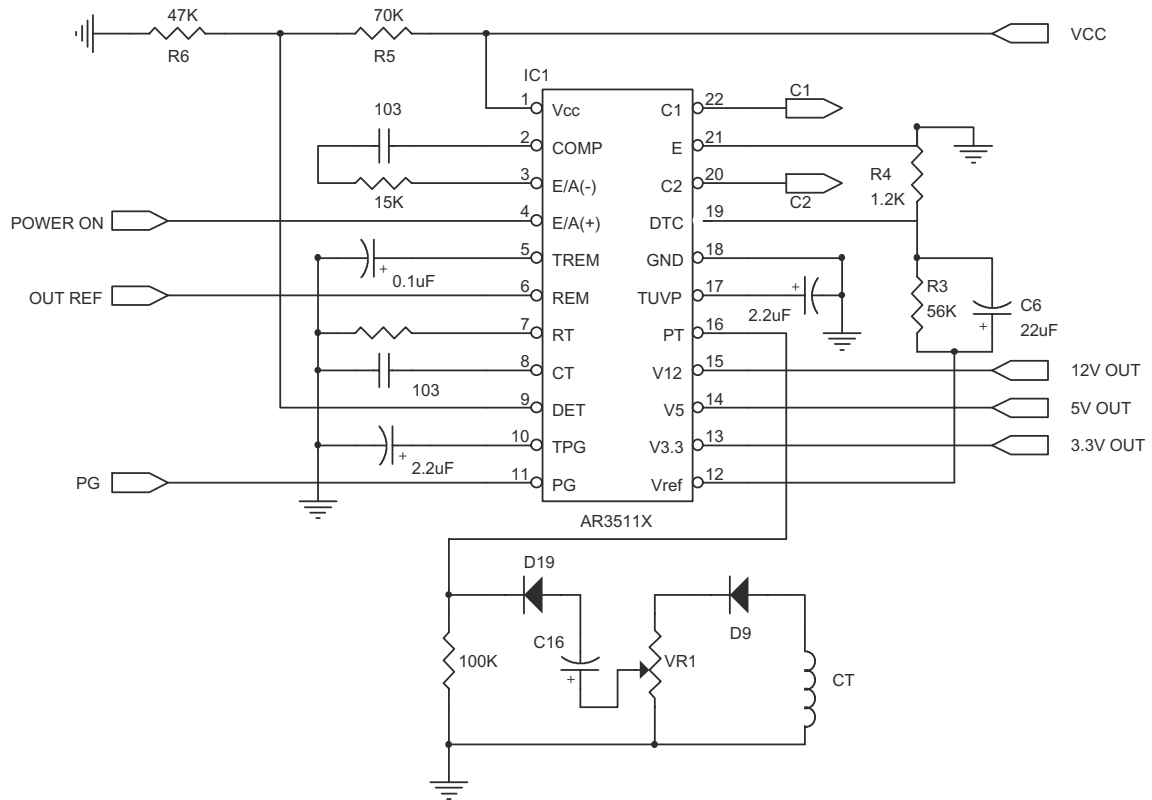


Figure 16. Vcc, +5Vdc Output vs. PG Signal (Low)

## 12. APPLICATION CIRCUIT



### Reference

1. Power Electronics by Marvin J. Fisher
2. Principles Of Power Electronics by Kassakian

### AUTHOR:

Sang-Tae Im: P-IC Application Team  
 Tel. 82-32-680-1275  
 Fax. 82-32-680-1317  
 E-mail. sangtae.im@Fairchildsemi.co.kr

## TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™  
CoolFET™  
CROSSVOLT™  
E<sup>2</sup>CMOS™  
FACT™  
FACT Quiet Series™  
FAST®  
FASTr™  
GTO™  
HiSeC™

ISOPLANAR™  
MICROWIRE™  
POP™  
PowerTrench®  
QFET™  
QS™  
Quiet Series™  
SuperSOT™-3  
SuperSOT™-6  
SuperSOT™-8

TinyLogic™  
UHC™  
VCX™

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.