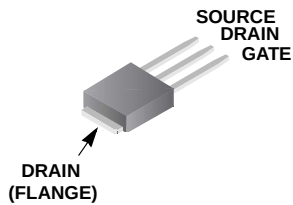


**16A, 100V, 0.090 Ohm, N-Channel,
UltraFET® Power MOSFETs**

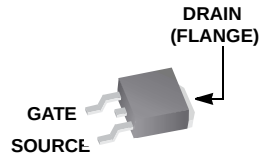
Packaging

JEDEC TO-251AA

JEDEC TO-252AA

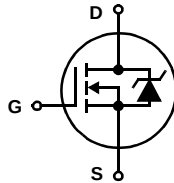


HUFA75617D3



HUFA75617D3S

Symbol



Features

- Ultra Low On-Resistance
 - $r_{DS(ON)} = 0.090\Omega$, $V_{GS} = 10V$
- Simulation Models
 - Temperature Compensated PSPICE® and SABER™ Electrical Models
 - Spice and SABER Thermal Impedance Models
 - www.fairchildsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUFA75617D3	TO-251AA	75617D
HUFA75617D3S	TO-252AA	75617D

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the variant in tape and reel, e.g., HUFA75617D3ST.

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	HUFA75617D3, HUFA75617D3S	UNITS
Drain to Source Voltage (Note 1)	100	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	100	V
Gate to Source Voltage	± 20	V
Drain Current		
Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 10V$) (Figure 2)	16	A
Continuous ($T_C = 100^\circ\text{C}$, $V_{GS} = 10V$) (Figure 2)	11	A
Pulsed Drain Current	Figure 4	
Pulsed Avalanche Rating	Figures 6, 14, 15	
Power Dissipation	64	W
Derate Above 25°C	0.43	W/ $^\circ\text{C}$
Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief TB334.	260	$^\circ\text{C}$

NOTE: $T_J = 25^\circ\text{C}$ to 150°C .

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: <http://www.aecouncil.com/>

Reliability data can be found at: <http://www.fairchildsemi.com/products/discrete/reliability/index.html>.

All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

HUFA75617D3

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 11)	100	-	-	V	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 95V, V _{GS} = 0V	-	-	1	μA	
		V _{DS} = 90V, V _{GS} = 0V, T _C = 150°C	-	-	250	μA	
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V	-	-	±100	nA	
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA (Figure 10)	2	-	4	V	
Drain to Source On Resistance	r _{DS(ON)}	I _D = 16A, V _{GS} = 10V (Figure 9)	-	0.080	0.090	¾	
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	R _{θJC}	TO-251, TO-252	-	-	2.34	°C/W	
Thermal Resistance Junction to Ambient	R _{θJA}		-	-	100	°C/W	
SWITCHING SPECIFICATIONS (V _{GS} = 10V)							
Turn-On Time	t _{ON}	V _{DD} = 50V, I _D = 16A V _{GS} = 10V, R _{GS} = 12Ω (Figures 18, 19)	-	-	60	ns	
Turn-On Delay Time	t _{d(ON)}		-	6	-	ns	
Rise Time	t _r		-	35	-	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	44	-	ns	
Fall Time	t _f		-	28	-	ns	
Turn-Off Time	t _{OFF}		-	-	108	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 20V	V _{DD} = 50V, I _D = 16A, I _{g(REF)} = 1.0mA (Figures 13, 16, 17)	-	31	39	nC
Gate Charge at 10V	Q _{g(10)}	V _{GS} = 0V to 10V		-	18	22	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0V to 2V		-	1.3	1.6	nC
Gate to Source Gate Charge	Q _{gs}			-	2.7	-	nC
Gate to Drain "Miller" Charge	Q _{gd}			-	6.4	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz (Figure 12)	-	570	-	pF	
Output Capacitance	C _{OSS}		-	125	-	pF	
Reverse Transfer Capacitance	C _{RSS}		-	20	-	pF	

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 16\text{A}$	-	-	1.25	V
		$I_{SD} = 7\text{A}$	-	-	1.00	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 16\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	80	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 16\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	170	nC

Typical Performance Curves

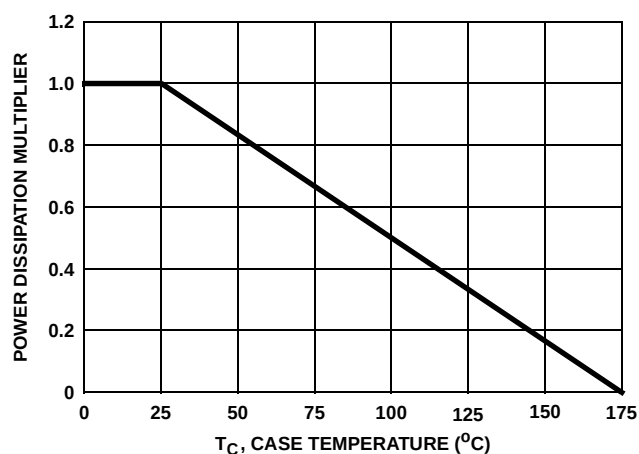


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

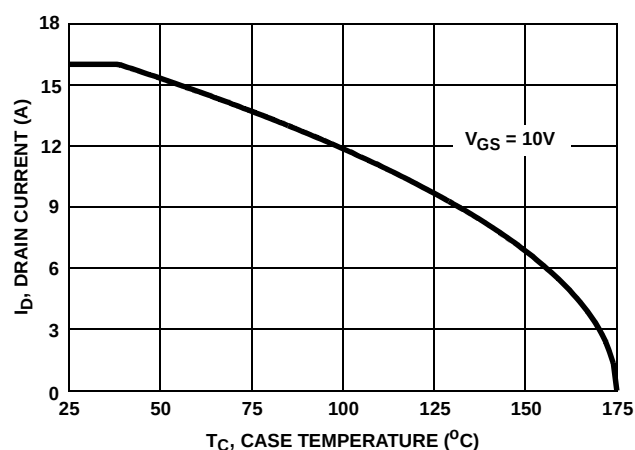


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

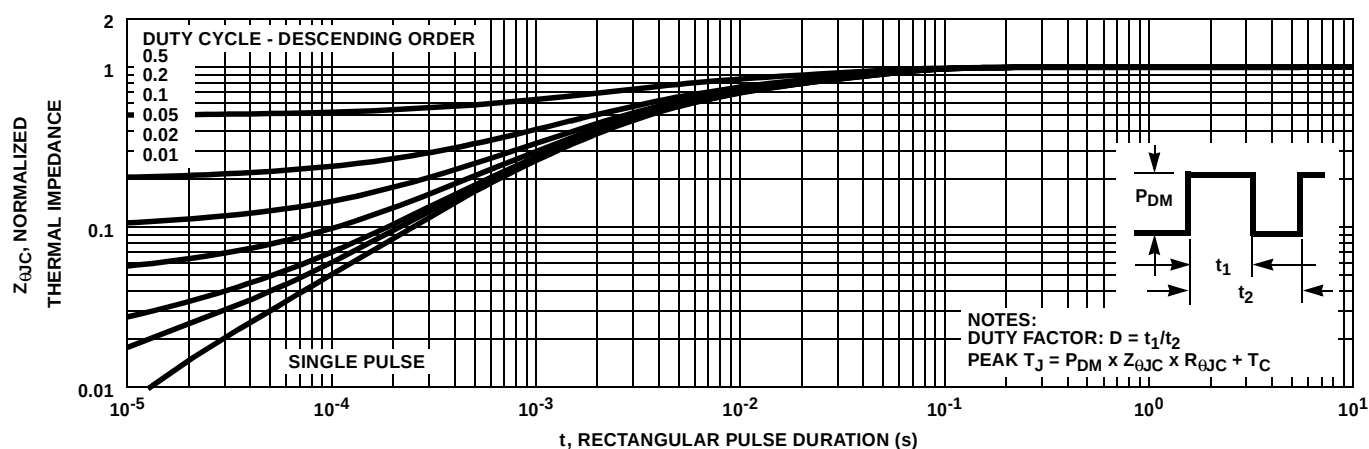


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

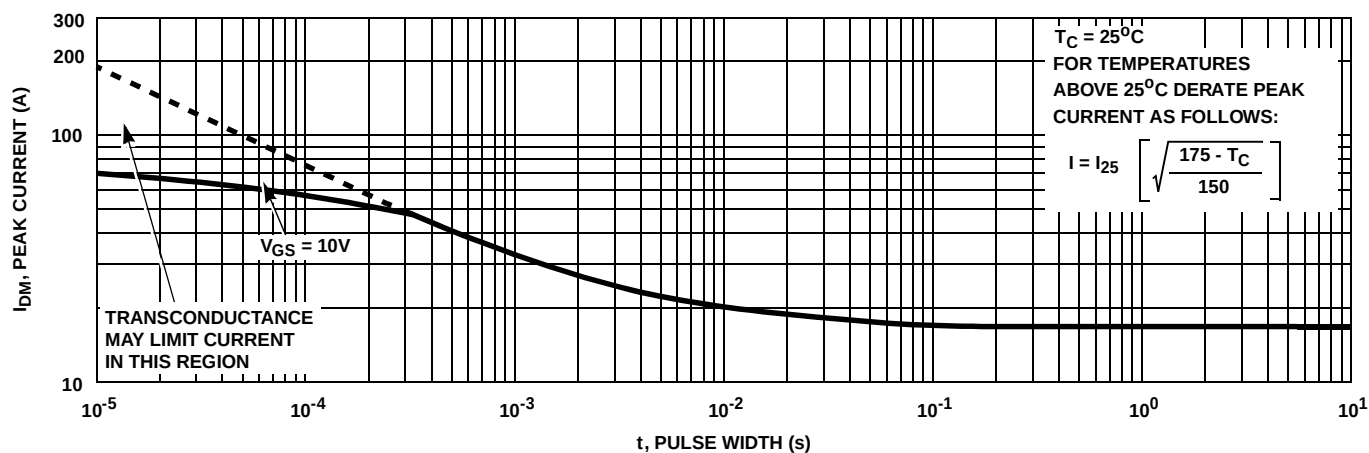


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

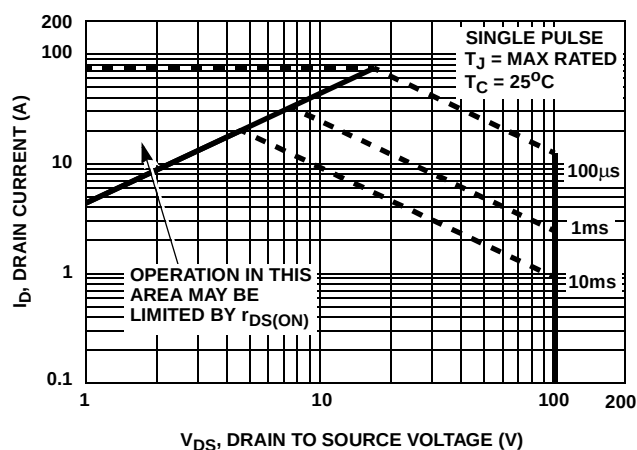
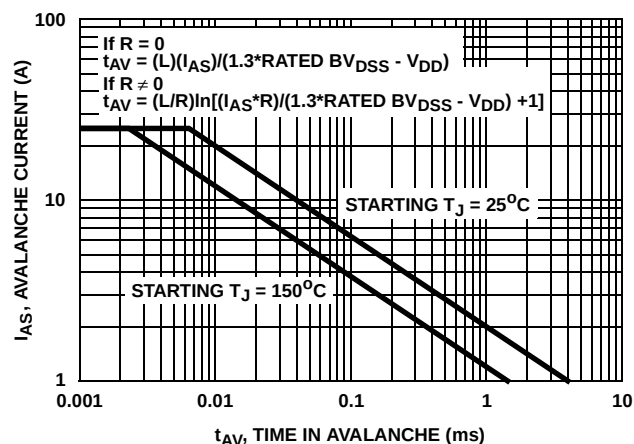


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

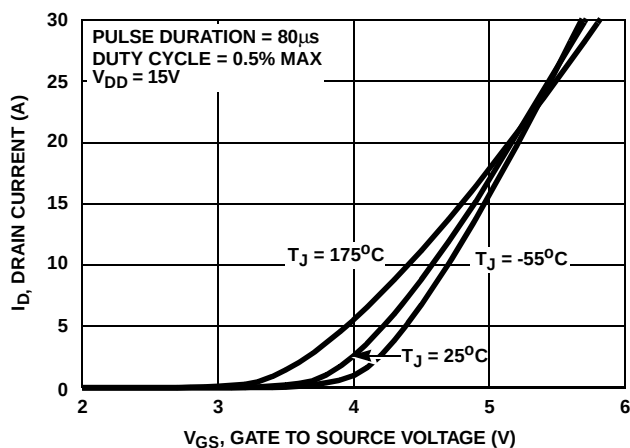


FIGURE 7. TRANSFER CHARACTERISTICS

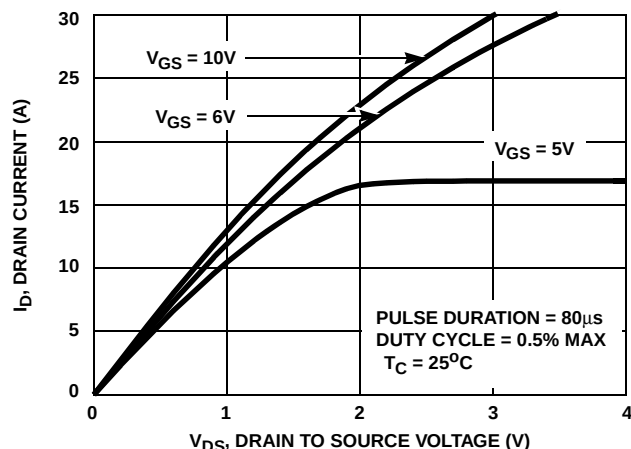


FIGURE 8. SATURATION CHARACTERISTICS

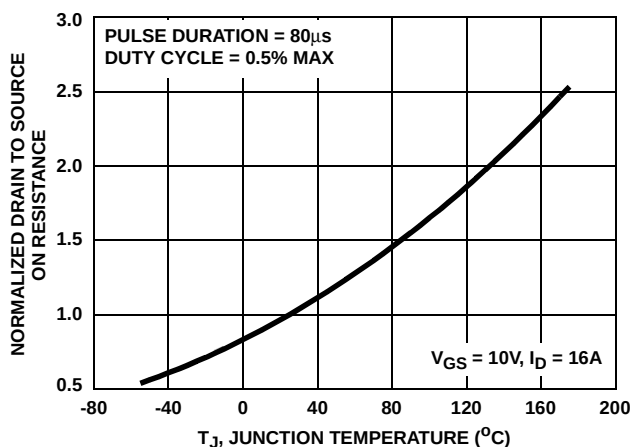


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

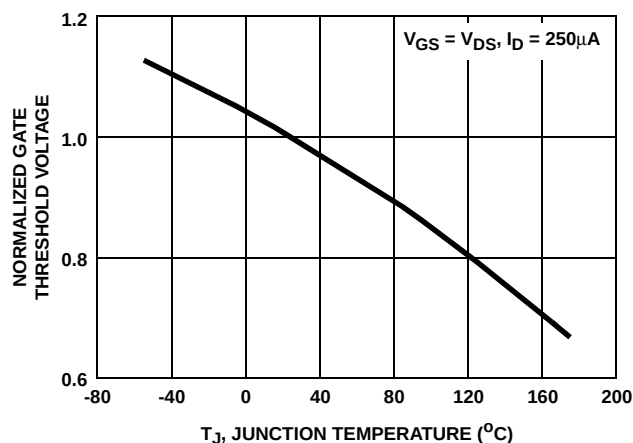


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

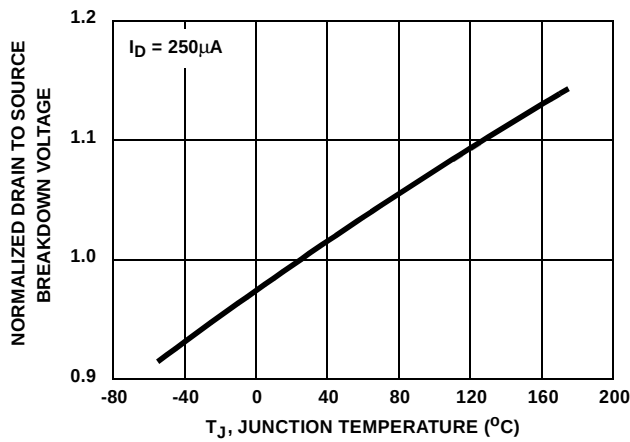


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

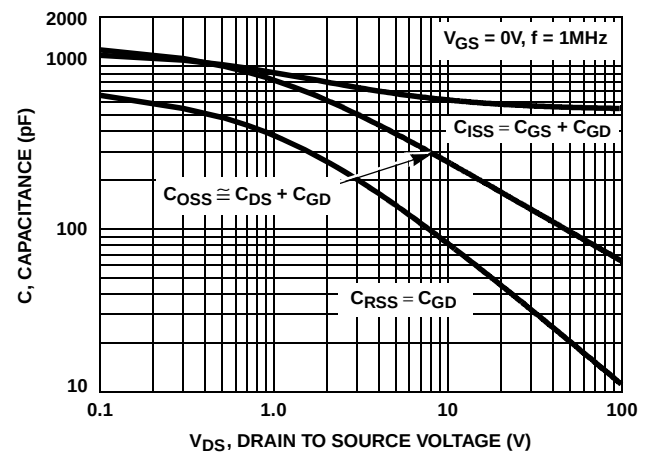
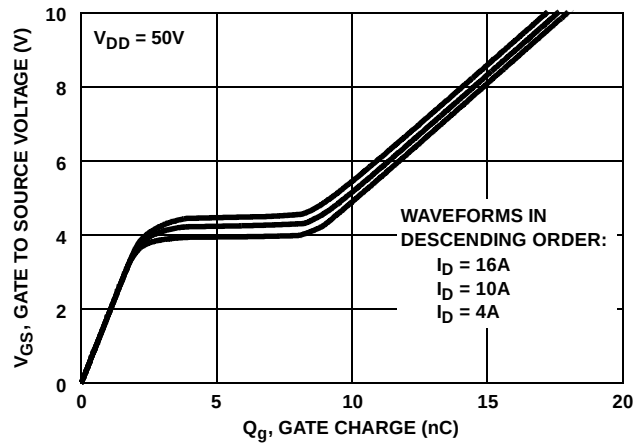


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

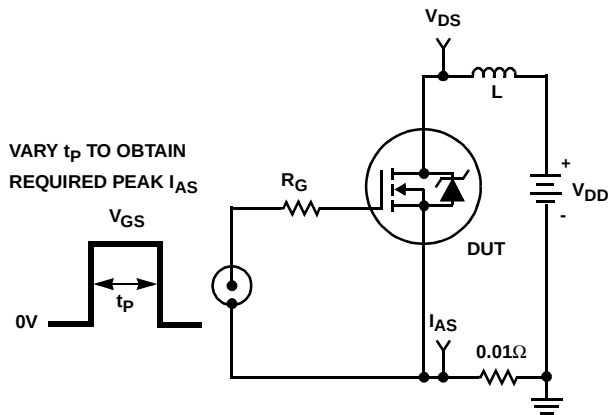


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

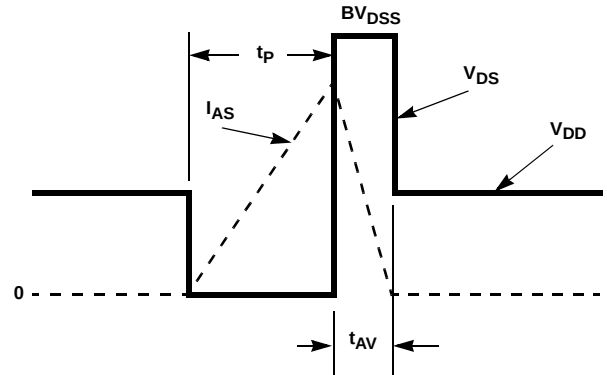


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

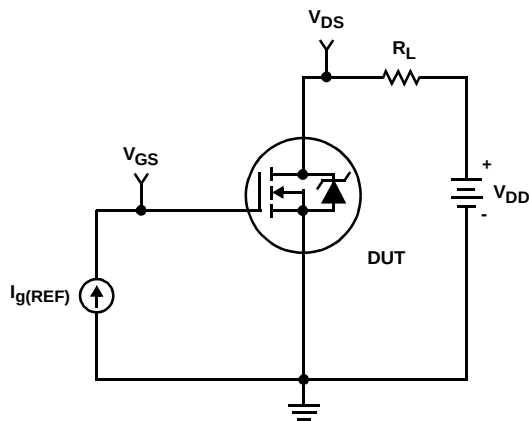


FIGURE 16. GATE CHARGE TEST CIRCUIT

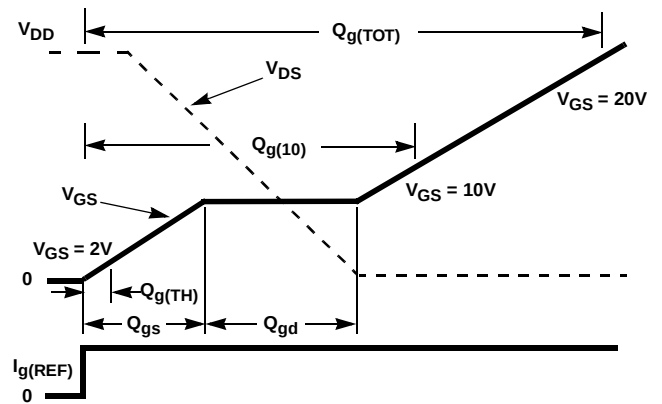


FIGURE 17. GATE CHARGE WAVEFORMS

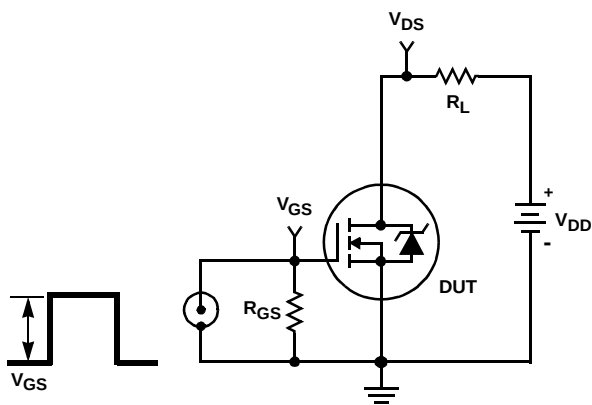


FIGURE 18. SWITCHING TIME TEST CIRCUIT

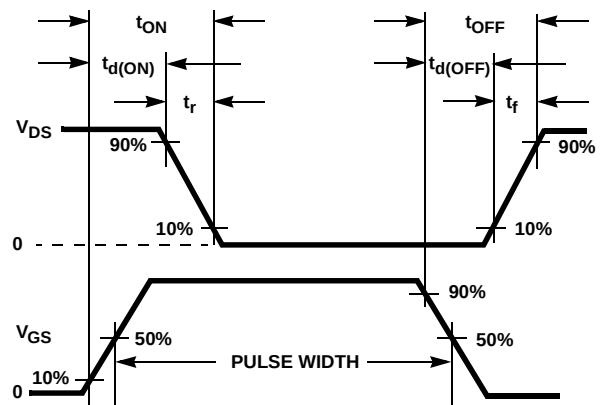


FIGURE 19. SWITCHING TIME WAVEFORM

PSPICE Electrical Model

.SUBCKT HUFA75617d3 2 1 3 ; rev 24May 2000

CA 12 8 9.9e-10
 CB 15 14 1.0e-9
 CIN 6 8 5.4e-10

DBODY 7 5 DBODYMOD
 DBREAK 5 11 DBREAKMOD
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 117.8
 EDS 14 8 5 8 1
 EGS 13 8 6 8 1
 ESG 6 10 6 8 1
 EVTHRES 6 21 19 8 1
 EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1.0e-9
 LGATE 1 9 5.24e-9
 LSOURCE 3 7 4.25e-9

MMED 16 6 8 8 MMEDMOD
 MSTRO 16 6 8 8 MSTROMOD
 MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
 RDRAIN 50 16 RDRAINMOD 3.9e-2
 RGATE 9 20 2.45
 RLDRAIN 2 5 10
 RLGATE 1 9 52.4
 RLSOURCE 3 7 42.5
 RSLC1 5 51 RSLCMOD 1e-6
 RSLC2 5 50 1e3
 RSOURCE 8 7 RSOURCEMOD 3.2e-2
 RVTHRES 22 8 RVTHRESMOD 1
 RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
 S1B 13 12 13 8 S1BMOD
 S2A 6 15 14 13 S2AMOD
 S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

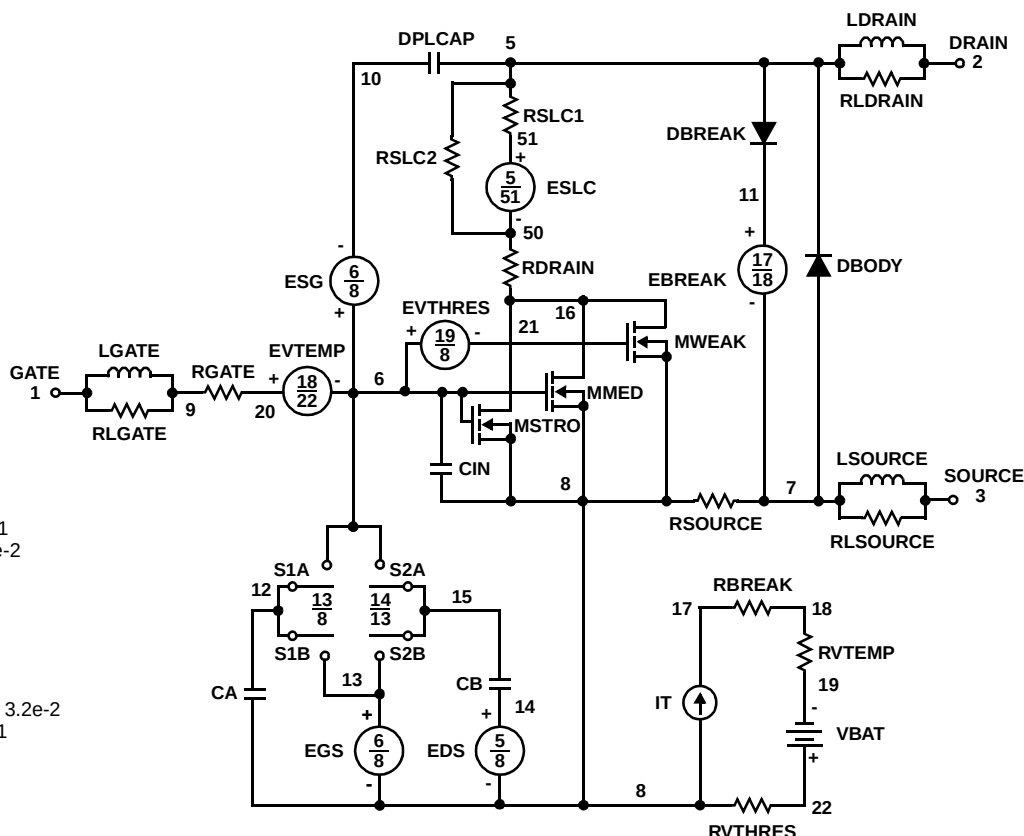
$$\text{ESLC } 51 \ 50 \ \text{VALUE} = \{ (V(5,51)/\text{ABS}(V(5,51))) * (\text{PWR}(V(5,51)/(1e-6*32), 3.5)) \}$$

.MODEL DBODYMOD D (IS = 6.0e-13 RS = 11.0e-3 XTI = 4.5 TRS1 = 1.1e-3 TRS2 = 7.1e-6 CJO = 6.5e-10 TT = 4.1e-8 M = 0.54)
 .MODEL DBREAKMOD D (RS = 5.6e-1 TRS1 = 8.0e-4 TRS2 = 3.0e-6)
 .MODEL DPLCAPMOD D (CJO = 7.0e-1 OIS = 1e-3 OM = 0.89 N = 10)
 .MODEL MMEDMOD NMOS (VTO = 3.10 KP = 3 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 2.45)
 .MODEL MSTROMOD NMOS (VTO = 3.64 KP = 42 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
 .MODEL MWEAKMOD NMOS (VTO = 2.68 KP = 0.02 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 24.5)
 .MODEL RBREAKMOD RES (TC1 = 1.05e-3 TC2 = -5.0e-7)
 .MODEL RDRAINMOD RES (TC1 = 1.20e-2 TC2 = 3.00e-5)
 .MODEL RSLCMOD RES (TC1 = 3.2e-3 TC2 = 1.0e-6)
 .MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-6)
 .MODEL RVTHRESMOD RES (TC1 = -2.2e-3 TC2 = -9.0e-6)
 .MODEL RVTEMPMOD RES (TC1 = -2.4e-3 TC2 = -1.8e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -5.9 VOFF = -3.1)
 .MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.1 VOFF = -5.9)
 .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.6 VOFF = 0.5)
 .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.5 VOFF = -0.6)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



SPICE Thermal Model

REV 24 May 2000

HUFA75617D

CTHERM1 th 6 1.00e-3
 CHERM2 6 5 4.00e-3
 CHERM3 5 4 4.00e-3
 CHERM4 4 3 3.60e-3
 CHERM5 3 2 7.00e-3
 CHERM6 2 tl 5.00e-2

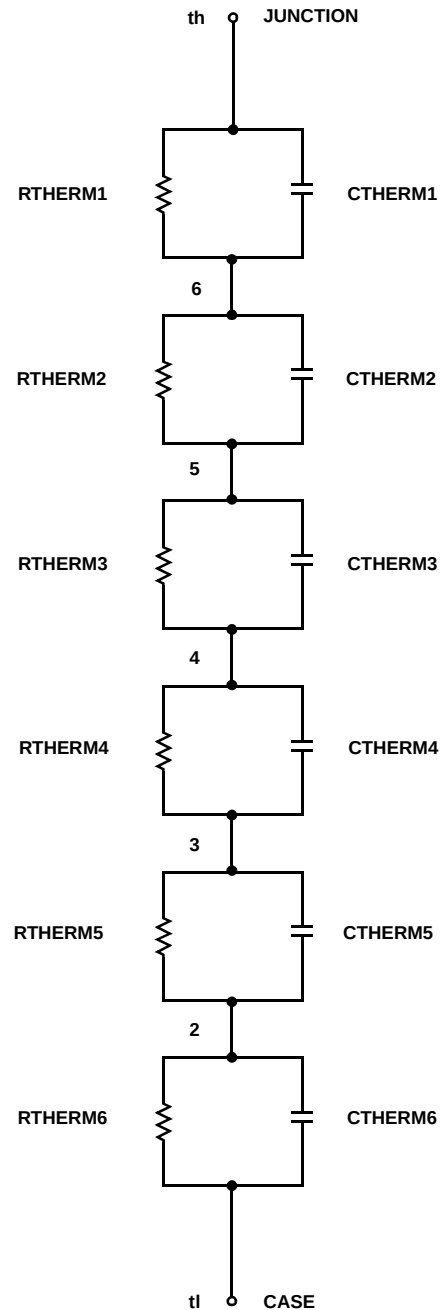
RHERM1 th 6 1.59e-2
 RHERM2 6 5 3.96e-2
 RHERM3 5 4 1.12e-1
 RHERM4 4 3 4.27e-1
 RHERM5 3 2 6.45e-1
 RHERM6 2 tl 7.00e-1

SABER Thermal Model

SABER thermal model HUFA75617D

```
template thermal_model th tl
thermal_c th, tl
{
    ctherm.ctherm1 th 6 = 1.00e-3
    ctherm.ctherm2 6 5 = 4.00e-3
    ctherm.ctherm3 5 4 = 4.00e-3
    ctherm.ctherm4 4 3 = 3.60e-3
    ctherm.ctherm5 3 2 = 7.00e-3
    ctherm.ctherm6 2 tl = 5.00e-2

    rtherm.rtherm1 th 6 = 1.59e-2
    rtherm.rtherm2 6 5 = 3.96e-2
    rtherm.rtherm3 5 4 = 1.12e-1
    rtherm.rtherm4 4 3 = 4.27e-1
    rtherm.rtherm5 3 2 = 6.45e-1
    rtherm.rtherm6 2 tl = 7.00e-1
}
```



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Bottomless TM	FAST ^r TM	OPTOPLANAR TM	STAR*POWER TM	
CoolFET TM	FRFET TM	PACMAN TM	Stealth TM	
CROSSVOLT TM	GlobalOptoisolator TM	POP TM	SuperSOT TM -3	
DenseTrench TM	GTO TM	Power247 TM	SuperSOT TM -6	
DOME TM	HiSeC TM	PowerTrench [®]	SuperSOT TM -8	
EcoSPARK TM	ISOPLANAR TM	QFET TM	SyncFET TM	
E ² CMOS TM	LittleFET TM	QS TM	TinyLogic TM	
EnSigna TM	MicroFET TM	QT Optoelectronics TM	TruTranslation TM	
FACT TM	MicroPak TM	Quiet Series TM	UHC TM	
FACT Quiet Series TM	MICROWIRE TM	SILENT SWITCHER [®]	UltraFET [®]	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.