

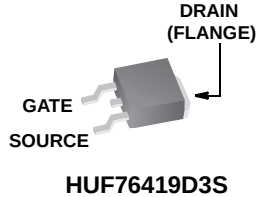
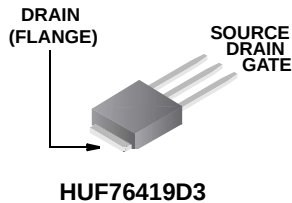
**20A, 60V, 0.043 Ohm, N-Channel, Logic
Level UltraFET® Power MOSFET**



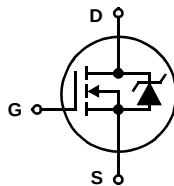
Packaging

JEDEC TO-251AA

JEDEC TO-252AA



Symbol



Features

- Ultra Low On-Resistance
 - $r_{DS(ON)} = 0.037\Omega$, $V_{GS} = 10V$
 - $r_{DS(ON)} = 0.043\Omega$, $V_{GS} = 5V$
- Simulation Models
 - Temperature Compensated PSPICE® and SABER™ Electrical Models
 - Spice and SABER Thermal Impedance Models
 - www.fairchildsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Switching Time vs R_{GS} Curves

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF76419D3	TO-251AA	76419D
HUF76419D3S	TO-252AA	76419D

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the variant in tape and reel, e.g., HUF76419D3ST

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	HUF76419D3, HUF76419D3S	UNITS
Drain to Source Voltage (Note 1)	V_{DSS} 60	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1).	V_{DGR} 60	V
Gate to Source Voltage	V_{GS} ± 16	V
Drain Current		
Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 5V$)	I_D 20	A
Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 10V$) (Figure 2)	I_D 20	A
Continuous ($T_C = 100^\circ\text{C}$, $V_{GS} = 5V$)	I_D 20	A
Continuous ($T_C = 100^\circ\text{C}$, $V_{GS} = 4.5V$) (Figure 2)	I_D 19	A
Pulsed Drain Current	I_{DM} Figure 4	
Pulsed Avalanche Rating	UIS Figures 6, 17, 18	
Power Dissipation	P_D 75	W
Derate Above 25°C	0.5	W/ $^\circ\text{C}$
Operating and Storage Temperature	T_J, T_{STG} -55 to 175	$^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s	T_L 300	$^\circ\text{C}$
Package Body for 10s, See Techbrief TB334	T_{pkg} 260	$^\circ\text{C}$

NOTE:

1. $T_J = 25^\circ\text{C}$ to 150°C .

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Product reliability information can be found at <http://www.fairchildsemi.com/products/discrete/reliability/index.html>

For severe environments, see our Automotive HUFA series.

All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

HUF76419D3, HUF76419D3S

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 12)	60	-	-	V	
		I _D = 250μA, V _{GS} = 0V , T _C = -40 ⁰ C (Figure 12)	55	-	-	V	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 55V, V _{GS} = 0V	-	-	1	μA	
		V _{DS} = 50V, V _{GS} = 0V, T _C = 150 ⁰ C	-	-	250	μA	
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±16V	-	-	±100	nA	
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA (Figure 11)	1	-	3	V	
Drain to Source On Resistance	r _{DS(ON)}	I _D = 20A, V _{GS} = 10V (Figures 9, 10)	-	0.031	0.037	Ω	
		I _D = 20A, V _{GS} = 5V (Figure 9)	-	0.036	0.043	Ω	
		I _D = 19A, V _{GS} = 4.5V (Figure 9)	-	0.038	0.046	Ω	
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	R _{θJC}	TO-251,TO-252	-	-	2.00	⁰ C/W	
Thermal Resistance Junction to Ambient	R _{θJA}		-	-	100	⁰ C/W	
SWITCHING SPECIFICATIONS (V _{GS} = 4.5V)							
Turn-On Time	t _{ON}	V _{DD} = 30V, I _D = 19A V _{GS} = 4.5V, R _{GS} = 13Ω (Figures 15, 21, 22)	-	-	205	ns	
Turn-On Delay Time	t _{d(ON)}		-	12	-	ns	
Rise Time	t _r		-	124	-	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	28	-	ns	
Fall Time	t _f		-	50	-	ns	
Turn-Off Time	t _{OFF}		-	-	115	ns	
SWITCHING SPECIFICATIONS (V _{GS} = 10V)							
Turn-On Time	t _{ON}	V _{DD} = 30V, I _D = 20A V _{GS} = 10V, R _{GS} = 13Ω (Figures 16, 21, 22)	-	-	62	ns	
Turn-On Delay Time	t _{d(ON)}		-	6.5	-	ns	
Rise Time	t _r		-	35	-	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	50	-	ns	
Fall Time	t _f		-	50	-	ns	
Turn-Off Time	t _{OFF}		-	-	150	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 10V	V _{DD} = 30V, I _D = 20A, I _{g(REF)} = 1.0mA (Figures 14, 19, 20)	-	23	27.5	nC
Gate Charge at 5V	Q _{g(5)}	V _{GS} = 0V to 5V		-	12.5	15	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0V to 1V		-	0.9	1.05	nC
Gate to Source Gate Charge	Q _{gs}			-	2.7	-	nC
Gate to Drain “Miller” Charge	Q _{gd}			-	5.9	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz (Figure 13)	-	900	-	pF	
Output Capacitance	C _{OSS}		-	250	-	pF	
Reverse Transfer Capacitance	C _{RSS}		-	45	-	pF	

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 20\text{A}$	-	-	1.25	V
		$I_{SD} = 10\text{A}$	-	-	1.0	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 20\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	74	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 20\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	200	nC

Typical Performance Curves

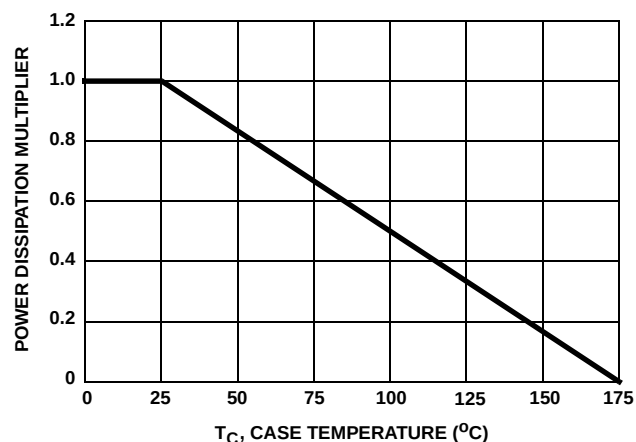


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

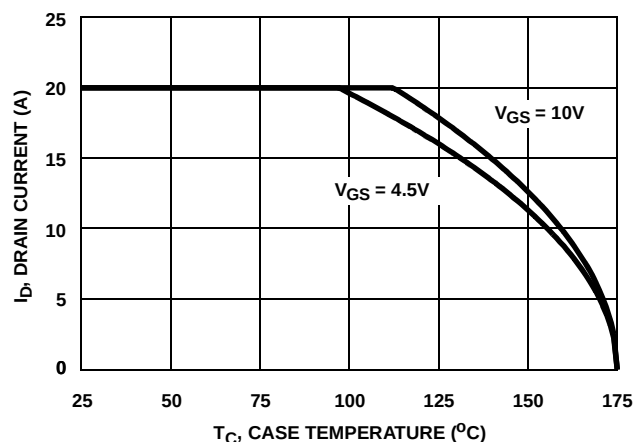


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

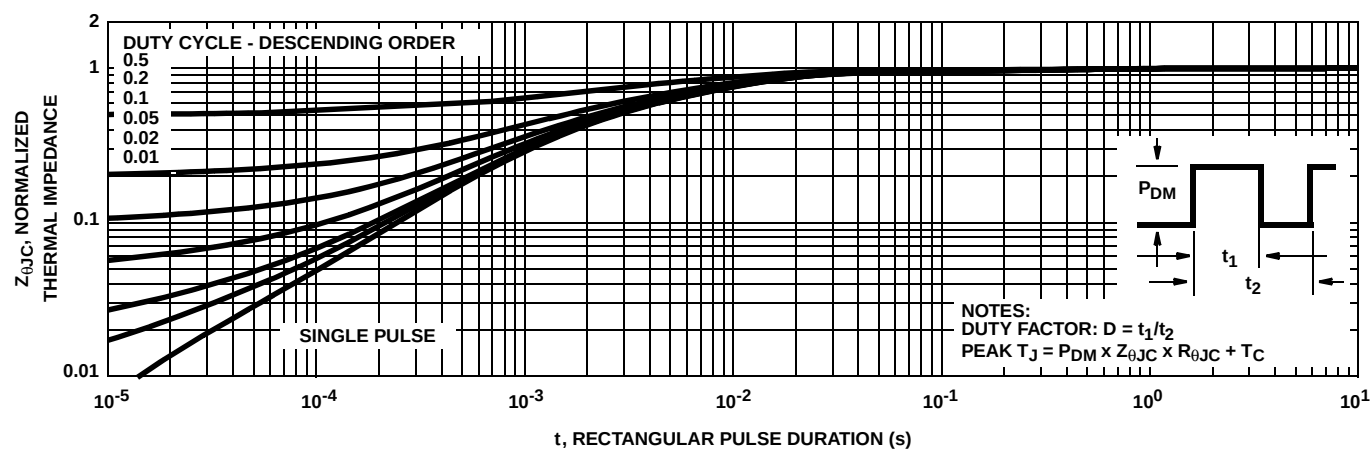


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

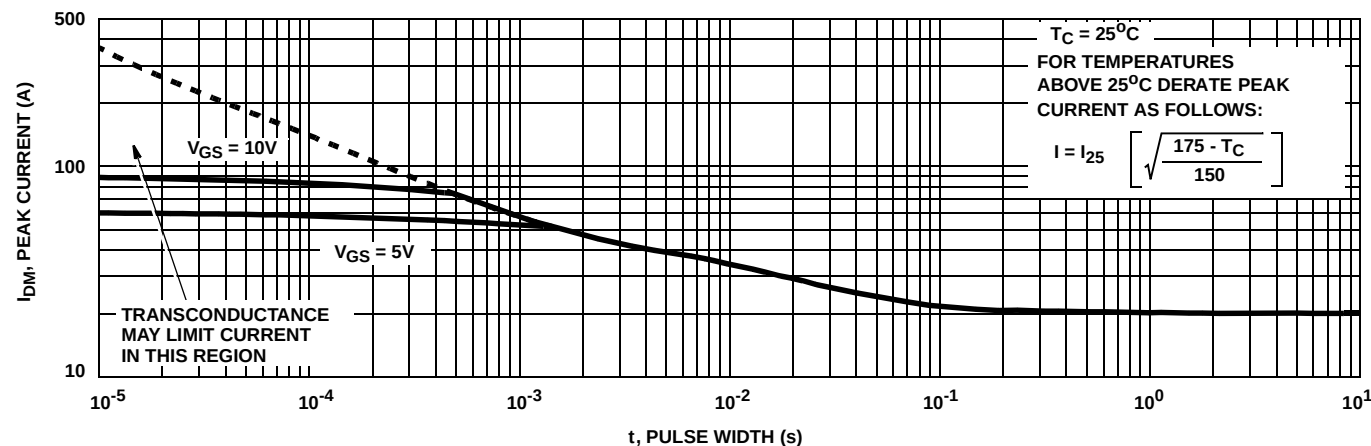


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

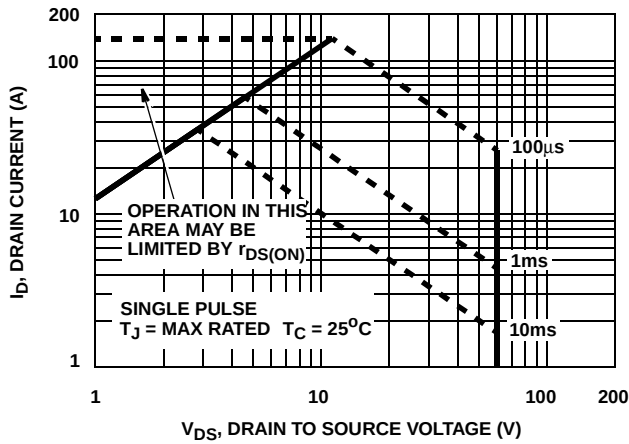
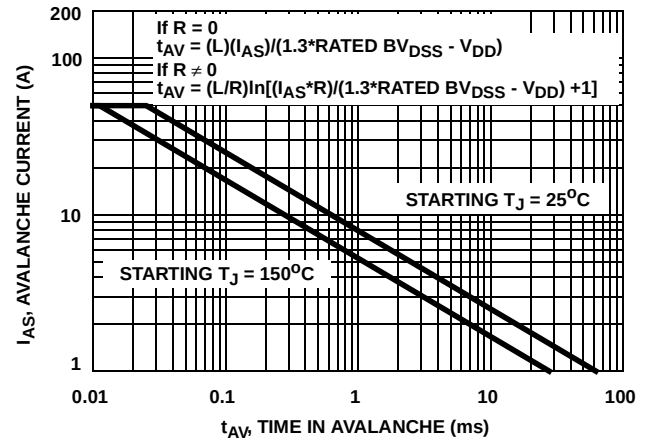


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

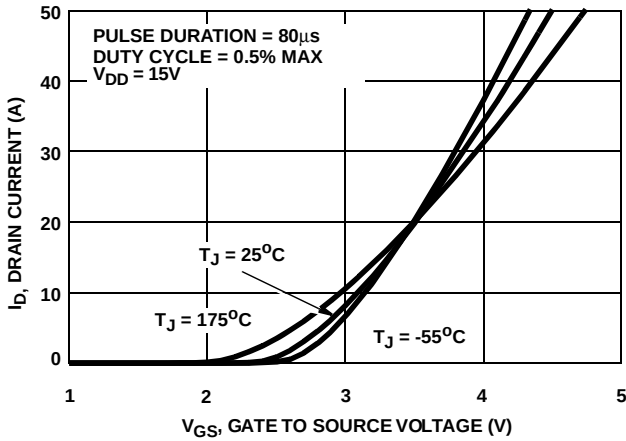


FIGURE 7. TRANSFER CHARACTERISTICS

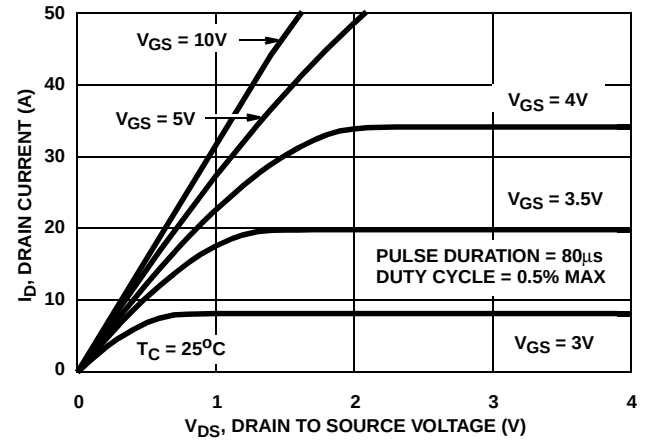


FIGURE 8. SATURATION CHARACTERISTICS

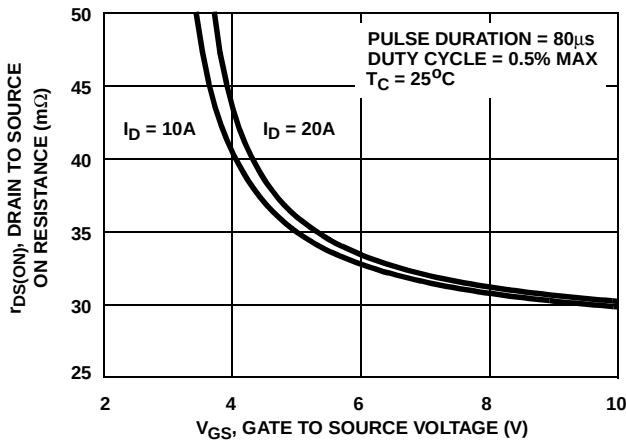


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

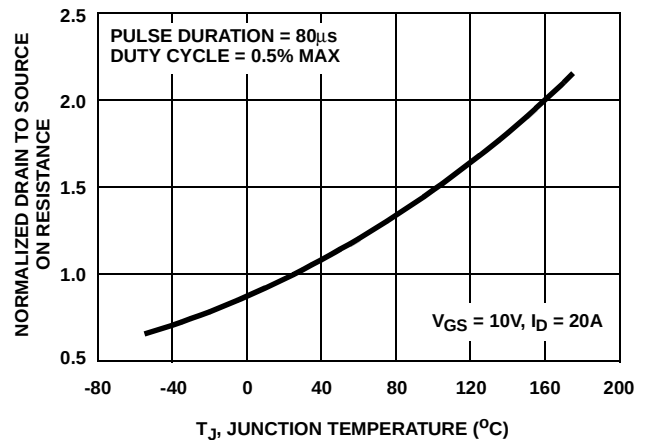


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

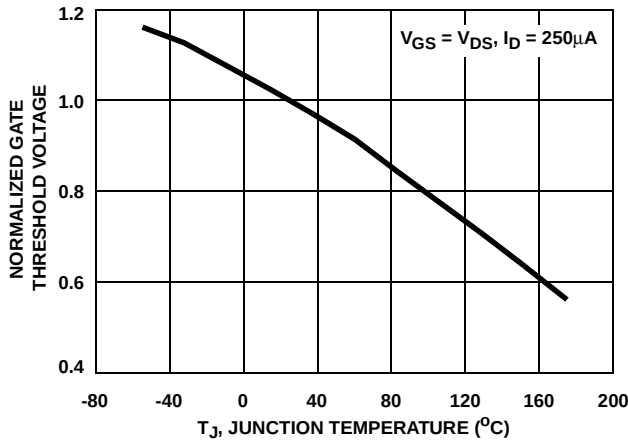


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

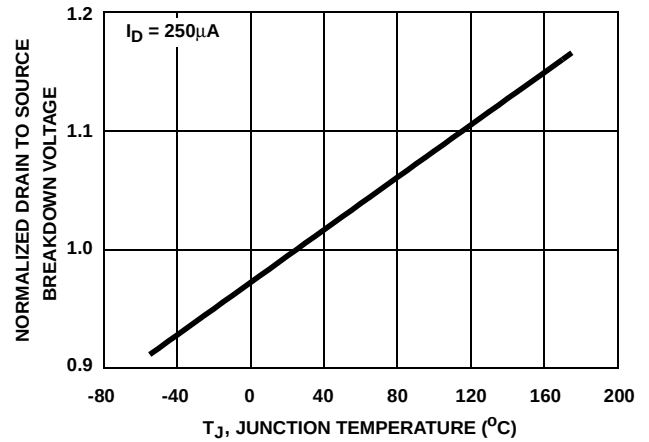


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

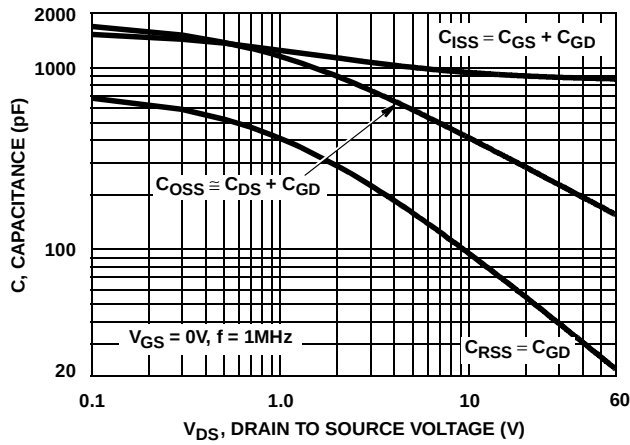
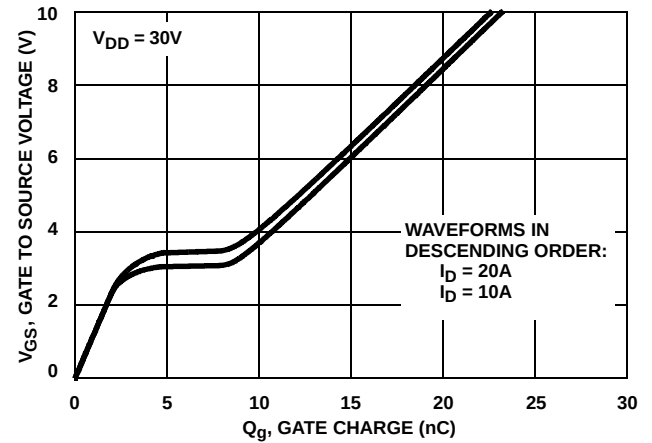


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

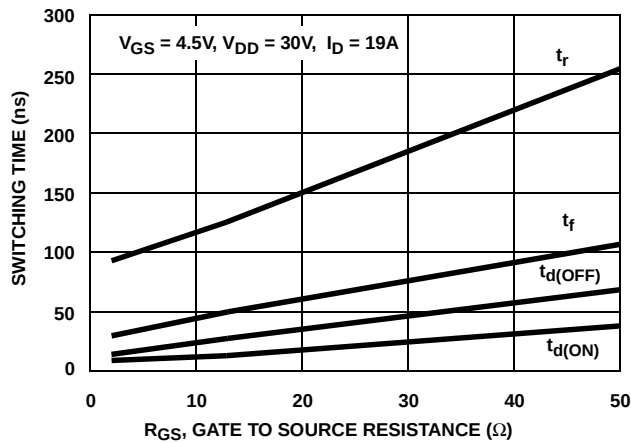


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

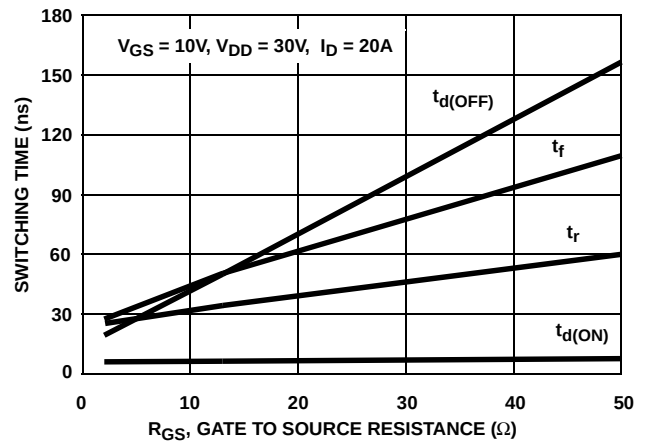


FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

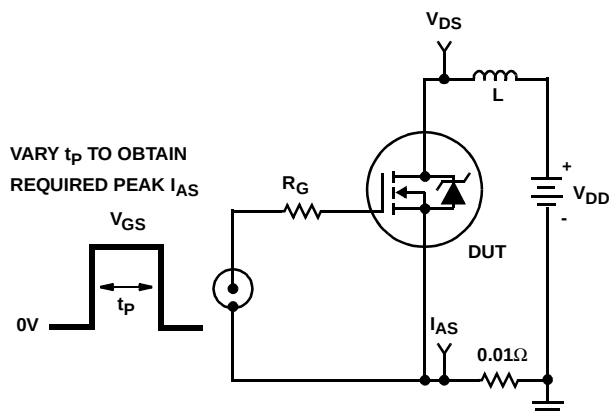


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

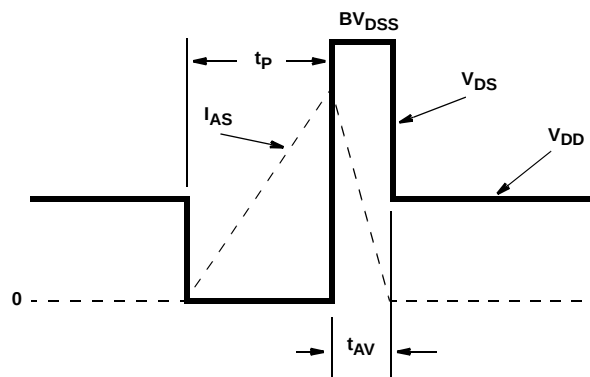


FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

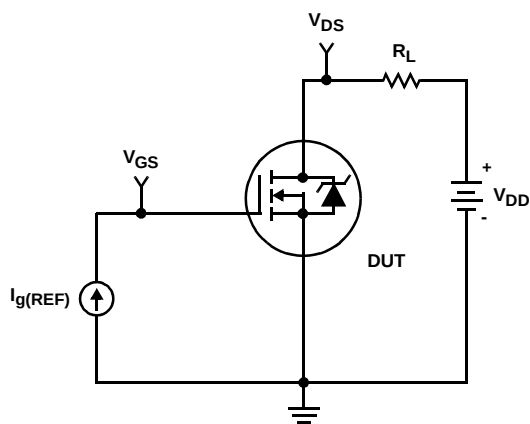


FIGURE 19. GATE CHARGE TEST CIRCUIT

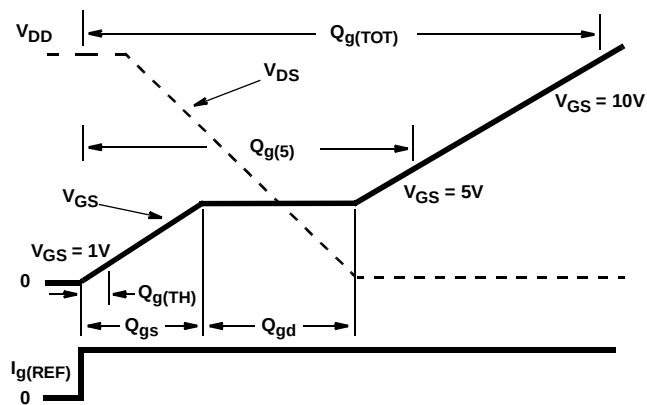


FIGURE 20. GATE CHARGE WAVEFORMS

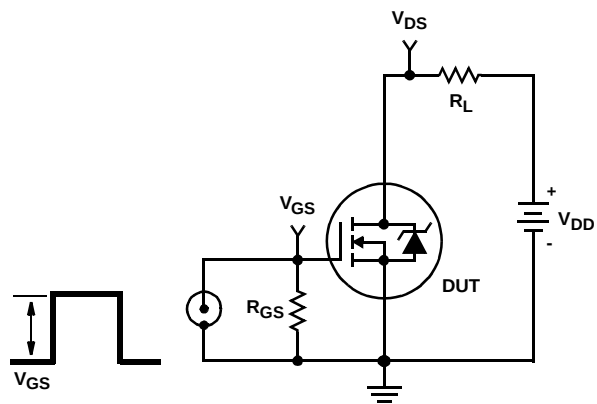


FIGURE 21. SWITCHING TIME TEST CIRCUIT

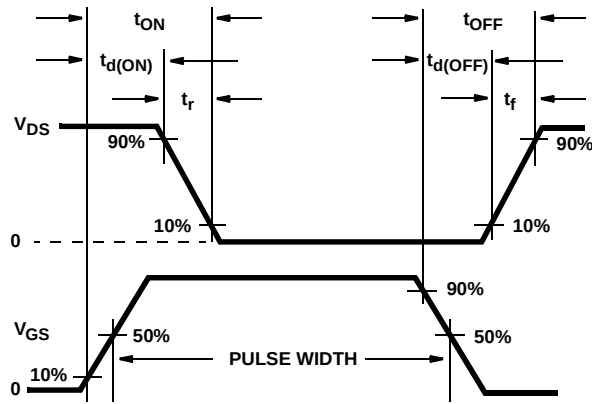


FIGURE 22. SWITCHING TIME WAVEFORM

SPICE Thermal Model

REV 16 July 1999

HUF76419D3T

CTHERM1 th 6 1.35e-3
 CTHERM2 6 5 1.50e-2
 CTHERM3 5 4 5.50e-3
 CTHERM4 4 3 3.00e-3
 CTHERM5 3 2 1.20e-2
 CTHERM6 2 tl 3.00

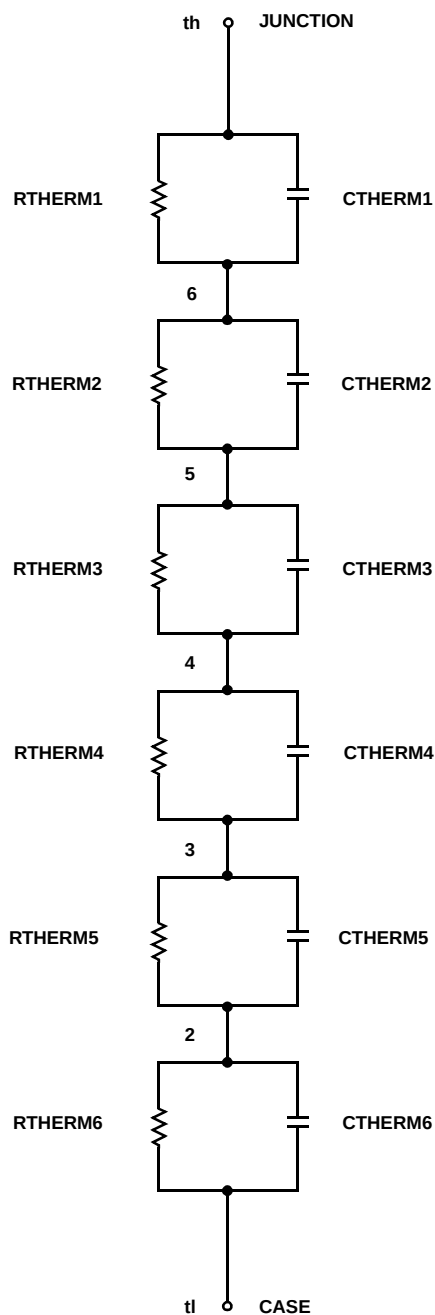
RTHERM1 th 6 1.32e-2
 RTHERM2 6 5 3.30e-2
 RTHERM3 5 4 9.28e-2
 RTHERM4 4 3 5.21e-1
 RTHERM5 3 2 7.86e-1
 RTHERM6 2 tl 1.04e-1

SABER Thermal Model

SABER thermal model HUF76419D3T

```
template thermal_model th tl
thermal_c th, tl
{
    ctherm.ctherm1 th 6 = 1.35e-3
    ctherm.ctherm2 6 5 = 1.50e-2
    ctherm.ctherm3 5 4 = 5.50e-3
    ctherm.ctherm4 4 3 = 3.00e-3
    ctherm.ctherm5 3 2 = 1.20e-2
    ctherm.ctherm6 2 tl = 3.00
```

```
rtherm.rtherm1 th 6 = 1.32e-2
rtherm.rtherm2 6 5 = 3.30e-2
rtherm.rtherm3 5 4 = 9.28e-2
rtherm.rtherm4 4 3 = 5.21e-1
rtherm.rtherm5 3 2 = 7.86e-1
rtherm.rtherm6 2 tl = 1.04e-1
```



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CoolFET™	FRFET™	PACMAN™	Stealth™	
CROSSVOLT™	GlobalOptoisolator™	POP™	SuperSOT™-3	
DenseTrench™	GTO™	Power247™	SuperSOT™-6	
DOME™	HiSeC™	PowerTrench [®]	SuperSOT™-8	
EcoSPARK™	ISOPLANAR™	QFET™	SyncFET™	
E ² CMOS™	LittleFET™	QS™	TinyLogic™	
EnSigna™	MicroFET™	QT Optoelectronics™	TruTranslation™	
FACT™	MicroPak™	Quiet Series™	UHC™	
FACT Quiet Series™	MICROWIRE™	SILENT SWITCHER [®]	UltraFET [®]	

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PRODUCT STATUS DEFINITIONS

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Datasheet Identification	Product Status	Definition
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