## 600V, SMPS Series N-Channel IGBT

The HGTD3N60A4S and the HGTP3N60A4 are MOS gated high voltage switching devices combining the best features of MOSFETs and bipolar transistors. These devices have the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between $25^oC$ and $150^oC$.

This IGBT is ideal for many high voltage switching applications operating at high frequencies where low conduction losses are essential. **This device has been optimized for high frequency switch mode power supplies**.

Formerly Developmental Type TA49327.

## Features

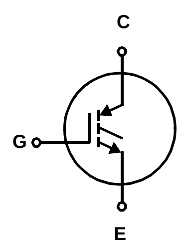
- >100kHz Operation at 390V, 3A
- 200kHz Operation at 390V, 2.5A
- 600V Switching SOA Capability
- Typical Fall Time. . . . . . . . . . . . . . . . . 70ns at $T_J = 125^oC$
- 12mJ $E_{AS}$ Capability
- Low Conduction Loss
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

## Ordering Information

| PART NUMBER | PACKAGE | BRAND |
|---|---|---|
| HGTD3N60A4S | TO-252AA | 3N60A4 |
| HGTP3N60A4 | TO-220AB | 3N60A4 |

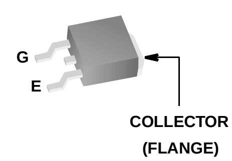
NOTE: When ordering, use the entire part number.

## Symbol

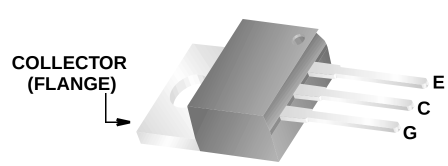



## Packaging

**JEDEC TO-252AA**




**JEDEC TO-220AB**




**FAIRCHILD CORPORATION IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 4,364,073 | 4,417,385 | 4,430,792 | 4,443,931 | 4,466,176 | 4,516,143 | 4,532,534 | 4,587,713 |
| 4,598,461 | 4,605,948 | 4,620,211 | 4,631,564 | 4,639,754 | 4,639,762 | 4,641,162 | 4,644,637 |
| 4,682,195 | 4,684,413 | 4,694,313 | 4,717,679 | 4,743,952 | 4,783,690 | 4,794,432 | 4,801,986 |
| 4,803,533 | 4,809,045 | 4,809,047 | 4,810,665 | 4,823,176 | 4,837,606 | 4,860,080 | 4,883,767 |
| 4,888,627 | 4,890,143 | 4,901,127 | 4,904,609 | 4,933,740 | 4,963,951 | 4,969,027 | |

## Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

| | | ALL TYPES | UNITS |
|---|---|---|---|
| Collector to Emitter Voltage | $BV_{CES}$ | 600 | V |
| Collector Current Continuous | | | |
| At $T_C = 25^oC$ | $I_{C25}$ | 17 | A |
| At $T_C = 110^oC$ | $I_{C110}$ | 8 | A |
| Collector Current Pulsed (Note 1) | $I_{CM}$ | 40 | A |
| Gate to Emitter Voltage Continuous | $V_{GES}$ | ±20 | V |
| Gate to Emitter Voltage Pulsed | $V_{GEM}$ | ±30 | V |
| Switching Safe Operating Area at $T_J = 150^oC$, Figure 2 | SSOA | 15A at 600V | |
| Single Pulse Avalanche Energy at $T_C = 25^oC$ | $E_{AS}$ | 12mJ at 3A | |
| Power Dissipation Total at $T_C = 25^oC$ | $P_D$ | 70 | W |
| Power Dissipation Derating $T_C > 25^oC$ | | 0.56 | $W/^oC$ |
| Operating and Storage Junction Temperature Range | $T_J$, $T_{STG}$ | -55 to 150 | $^oC$ |
| Maximum Lead Temperature for Soldering | | | |
| Leads at 0.063in (1.6mm) from Case for 10s | $T_L$ | 300 | $^oC$ |
| Package Body for 10s, See Tech Brief 334 | $T_{PKG}$ | 260 | $^oC$ |

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. Pulse width limited by maximum junction temperature.

## Electrical Specifications $T_J = 25^oC$, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Collector to Emitter Breakdown Voltage | $BV_{CES}$ | $I_C = 250\mu A$, $V_{GE} = 0V$ | | 600 | - | - | V |
| Emitter to Collector Breakdown Voltage | $BV_{ECS}$ | $I_C = -10mA$, $V_{GE} = 0V$ | | 20 | - | - | V |
| Collector to Emitter Leakage Current | $I_{CES}$ | $V_{CE} = 600V$ | $T_J = 25^oC$ | - | - | 250 | µA |
| | | | $T_J = 125^oC$ | - | - | 2.0 | mA |
| Collector to Emitter Saturation Voltage | $V_{CE(SAT)}$ | $I_C = 3A$, $V_{GE} = 15V$ | $T_J = 25^oC$ | - | 2.0 | 2.7 | V |
| | | | $T_J = 125^oC$ | - | 1.6 | 2.2 | V |
| Gate to Emitter Threshold Voltage | $V_{GE(TH)}$ | $I_C = 250\mu A$, $V_{CE} = 600V$ | | 4.5 | 6.1 | 7.0 | V |
| Gate to Emitter Leakage Current | $I_{GES}$ | $V_{GE} = \pm 20V$ | | - | - | ±250 | nA |
| Switching SOA | SSOA | $T_J = 150^oC$, $R_G = 50\Omega$, $V_{GE} = 15V$ L = 200µH, $V_{CE} = 600V$ | | 15 | - | - | A |
| Pulsed Avalanche Energy | $E_{AS}$ | $I_{CE} = 3A$, L = 2.7mH | | 12 | - | - | mJ |
| Gate to Emitter Plateau Voltage | $V_{GEP}$ | $I_C = 3A$, $V_{CE} = 300V$ | | - | 8.8 | - | V |
| On-State Gate Charge | $Q_{g(ON)}$ | $I_C = 3A$, $V_{CE} = 300V$ | $V_{GE} = 15V$ | - | 21 | 25 | nC |
| | | | $V_{GE} = 20V$ | - | 26 | 32 | nC |
| Current Turn-On Delay Time | $t_{d(ON)I}$ | IGBT and Diode at $T_J = 25^oC$ $I_{CE} = 3A$ $V_{CE} = 390V$ $V_{GE} = 15V$ $R_G = 50\Omega$ L = 1mH Test Circuit - Figure 20 | | - | 6 | - | ns |
| Current Rise Time | $t_{rI}$ | | | - | 11 | - | ns |
| Current Turn-Off Delay Time | $t_{d(OFF)I}$ | | | - | 73 | - | ns |
| Current Fall Time | $t_{fI}$ | | | - | 47 | - | ns |
| Turn-On Energy (Note 3) | $E_{ON1}$ | | | - | 37 | - | µJ |
| Turn-On Energy (Note 3) | $E_{ON2}$ | | | - | 55 | 70 | µJ |
| Turn-Off Energy (Note 2) | $E_{OFF}$ | | | - | 25 | 35 | µJ |

**Electrical Specifications** $T_J = 25^oC$, Unless Otherwise Specified **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Current Turn-On Delay Time | $t_{d(ON)I}$ | IGBT and Diode at $T_J = 125^oC$<br>$I_{CE}$ = 3A<br>$V_{CE}$ = 390V<br>$V_{GE}$ = 15V<br>$R_G = 50\Omega$<br>L = 1mH<br>Test Circuit - Figure 20 | - | 5.5 | 8 | ns |
| Current Rise Time | $t_{rI}$ | | - | 12 | 15 | ns |
| Current Turn-Off Delay Time | $t_{d(OFF)I}$ | | - | 110 | 165 | ns |
| Current Fall Time | $t_{fI}$ | | - | 70 | 100 | ns |
| Turn-On Energy (Note 3) | $E_{ON1}$ | | - | 37 | - | μJ |
| Turn-On Energy (Note 3) | $E_{ON2}$ | | - | 90 | 100 | μJ |
| Turn-Off Energy (Note 2) | $E_{OFF}$ | | - | 50 | 80 | μJ |
| Thermal Resistance Junction To Case | $R_{\theta JC}$ | | - | - | 1.8 | $^oC/W$ |

NOTES:

2. Turn-Off Energy Loss ($E_{OFF}$) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE}$ = 0A). All devices were tested per JEDEC Standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.
3. Values for two Turn-On loss conditions are shown for the convenience of the circuit designer. $E_{ON1}$ is the turn-on loss of the IGBT only. $E_{ON2}$ is the turn-on loss when a typical diode is used in the test circuit and the diode is at the same $T_J$ as the IGBT. The diode type is specified in Figure 20.

## *Typical Performance Curves* Unless Otherwise Specified

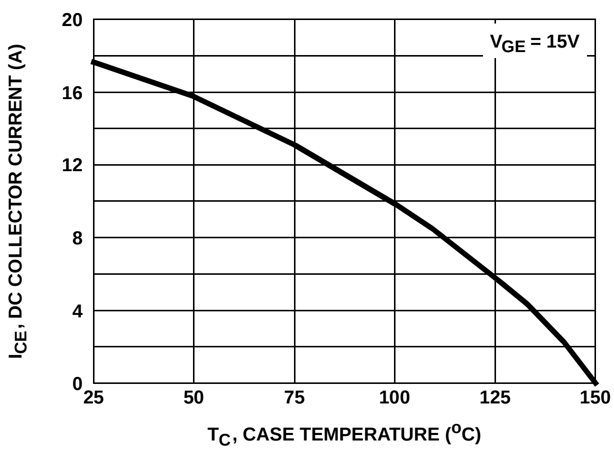



**FIGURE 1. DC COLLECTOR CURRENT vs CASE TEMPERATURE**

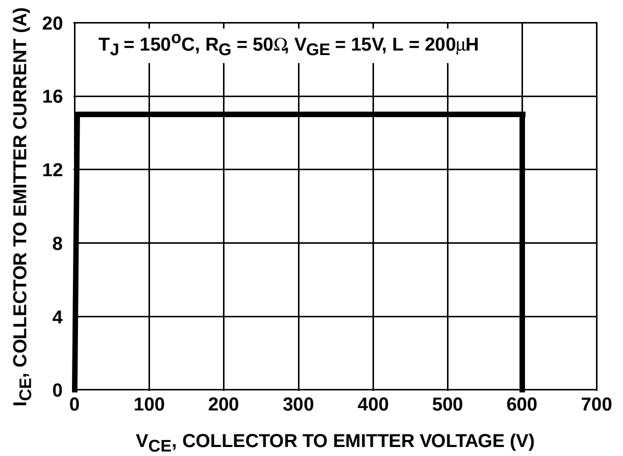



**FIGURE 2. MINIMUM SWITCHING SAFE OPERATING AREA**

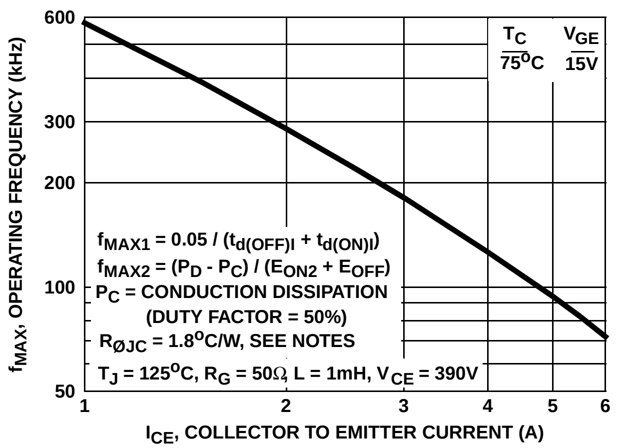



**FIGURE 3. OPERATING FREQUENCY vs COLLECTOR TO EMITTER CURRENT**

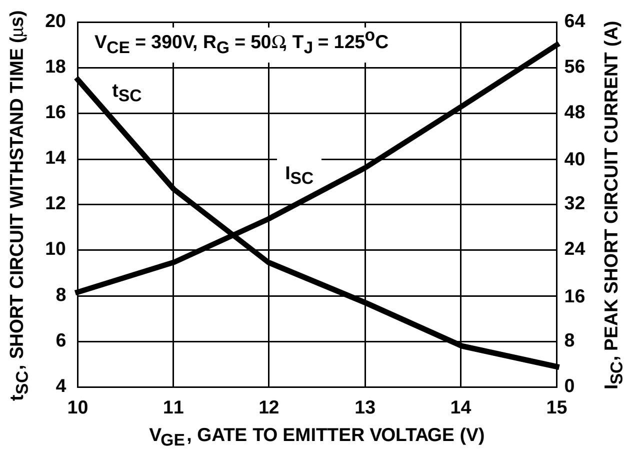



**FIGURE 4. SHORT CIRCUIT WITHSTAND TIME**

## *Typical Performance Curves* Unless Otherwise Specified **(Continued)**

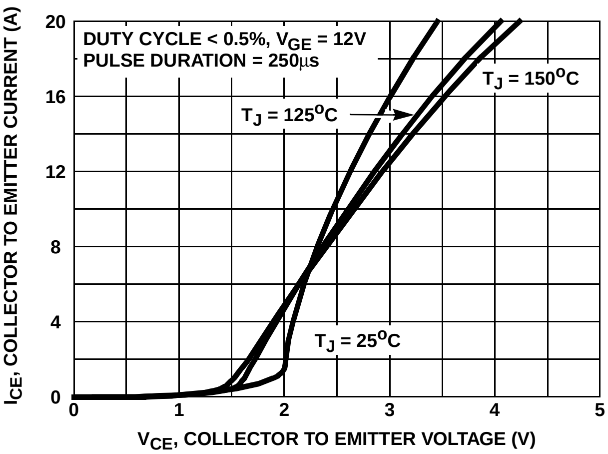



**FIGURE 5. COLLECTOR TO EMITTER ON-STATE VOLTAGE**

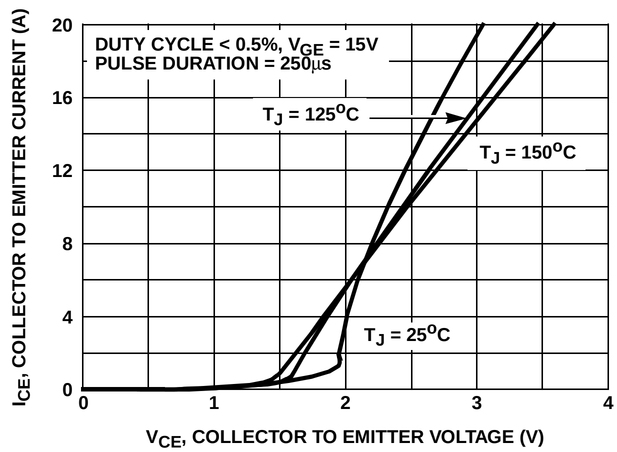



**FIGURE 6. COLLECTOR TO EMITTER ON-STATE VOLTAGE**

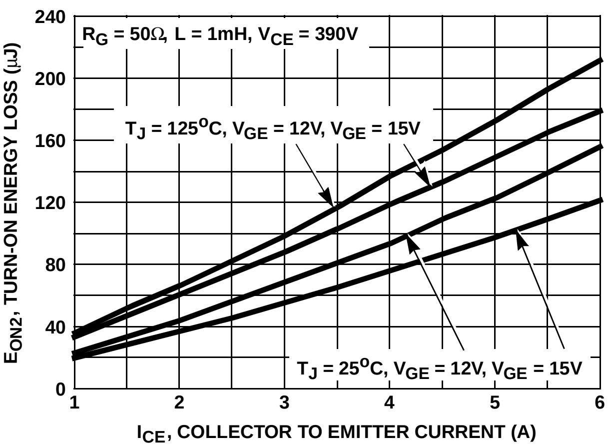



**FIGURE 7. TURN-ON ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT**

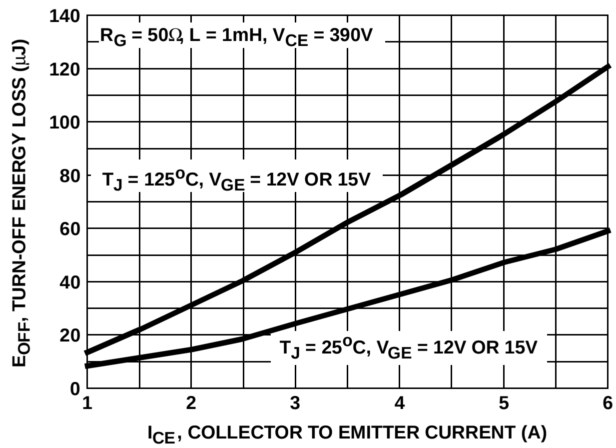



**FIGURE 8. TURN-OFF ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT**

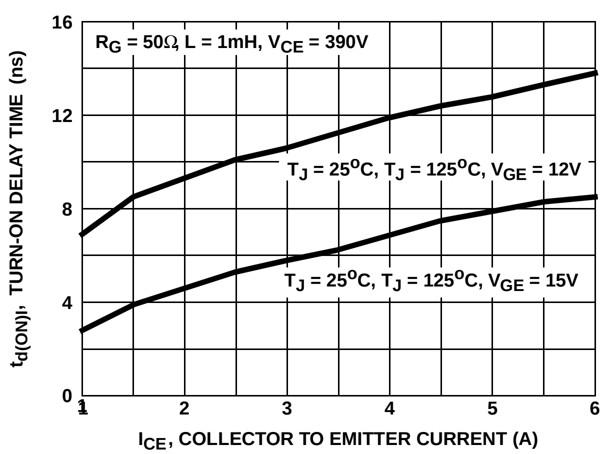



**FIGURE 9. TURN-ON DELAY TIME vs COLLECTOR TO EMITTER CURRENT**

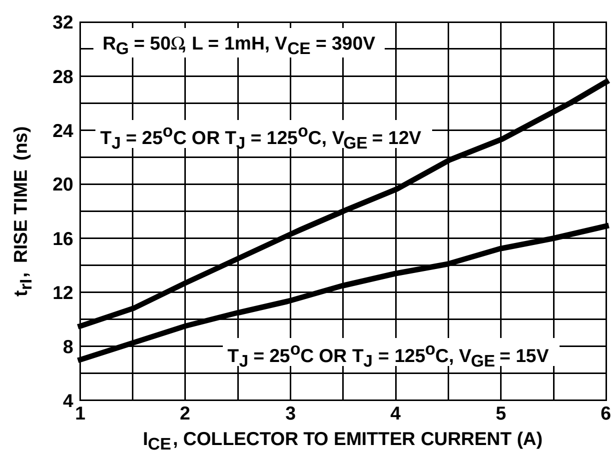



**FIGURE 10. TURN-ON RISE TIME vs COLLECTOR TO EMITTER CURRENT**

## *Typical Performance Curves* Unless Otherwise Specified **(Continued)**

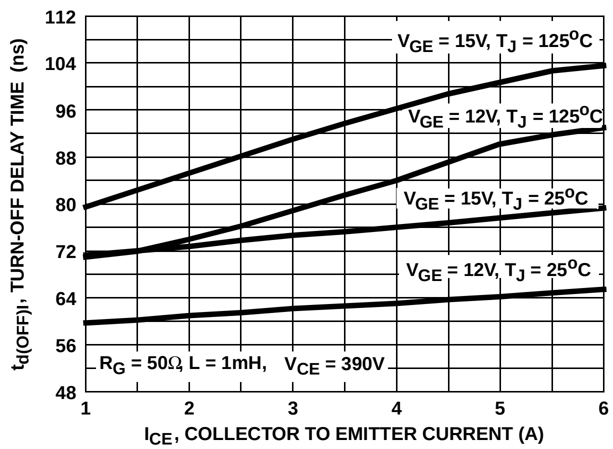



**FIGURE 11. TURN-OFF DELAY TIME vs COLLECTOR TO EMITTER CURRENT**

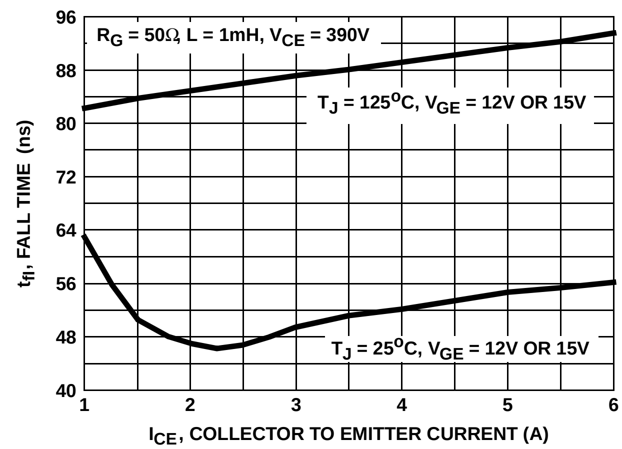



**FIGURE 12. FALL TIME vs COLLECTOR TO EMITTER CURRENT**

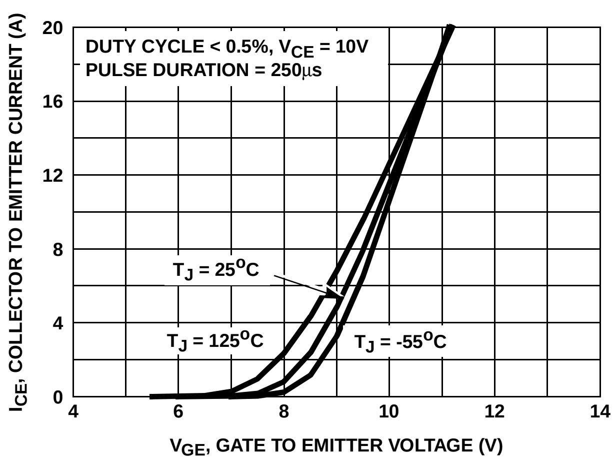



**FIGURE 13. TRANSFER CHARACTERISTIC**

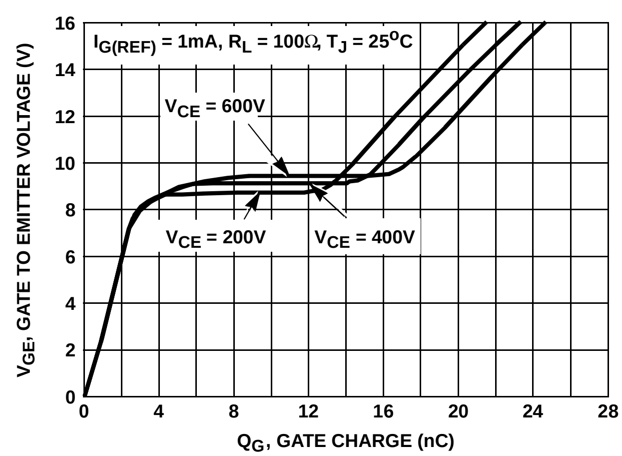



**FIGURE 14. GATE CHARGE WAVEFORMS**

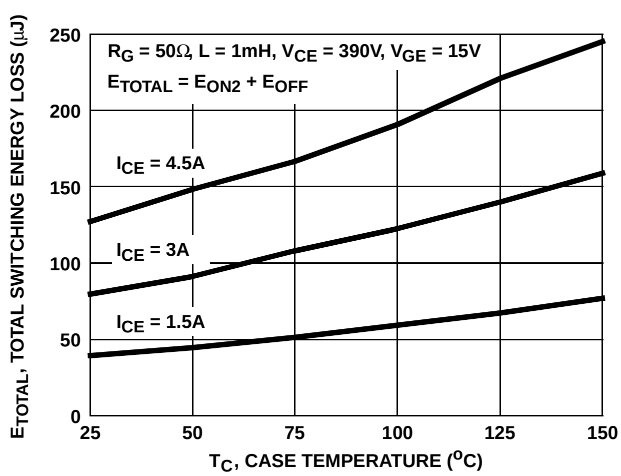



**FIGURE 15. TOTAL SWITCHING LOSS vs CASE TEMPERATURE**

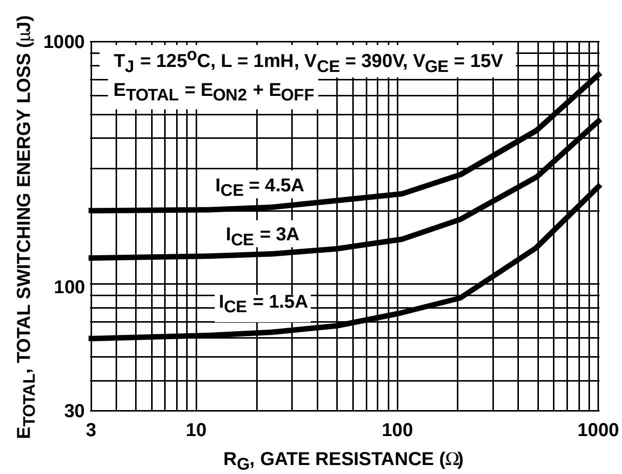



**FIGURE 16. TOTAL SWITCHING LOSS vs GATE RESISTANCE**

## *Typical Performance Curves* Unless Otherwise Specified **(Continued)**

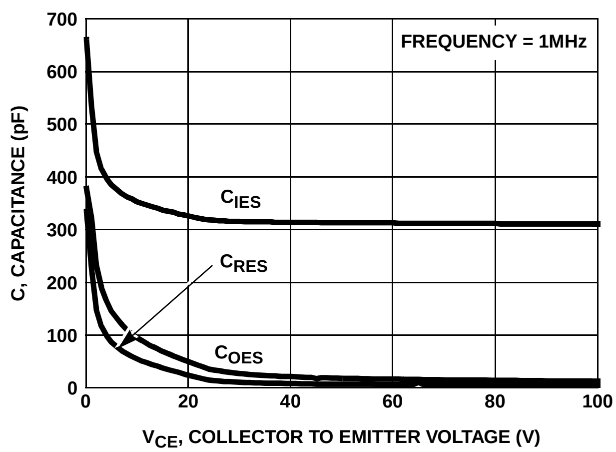



FIGURE 17. CAPACITANCE vs COLLECTOR TO EMITTER VOLTAGE

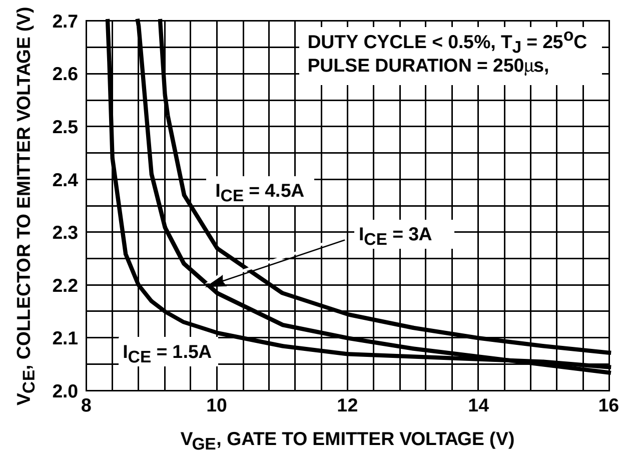



FIGURE 18. COLLECTOR TO EMITTER ON-STATE VOLTAGE vs GATE TO EMITTER VOLTAGE

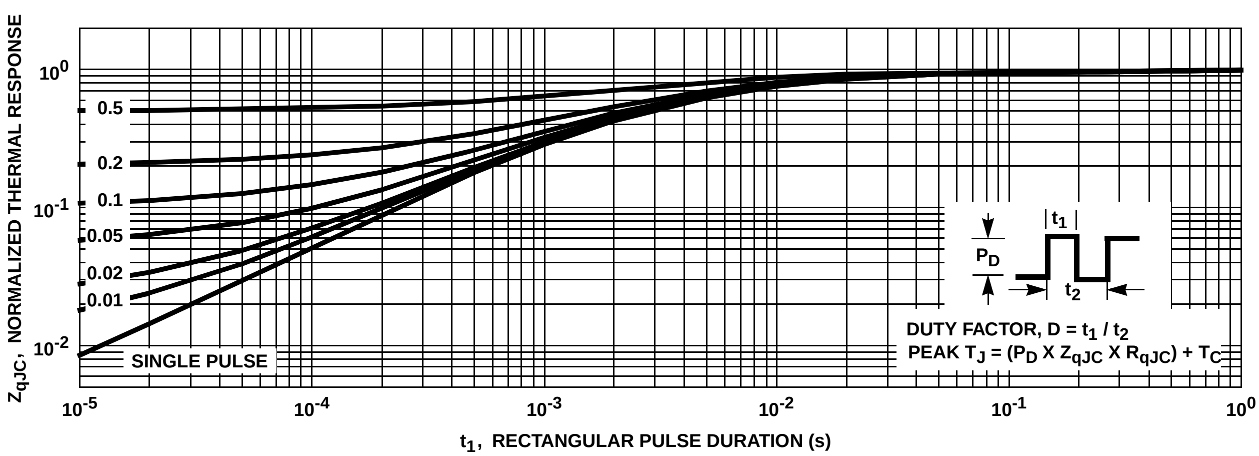



FIGURE 19. IGBT NORMALIZED TRANSIENT THERMAL RESPONSE, JUNCTION TO CASE

## Test Circuit and Waveforms

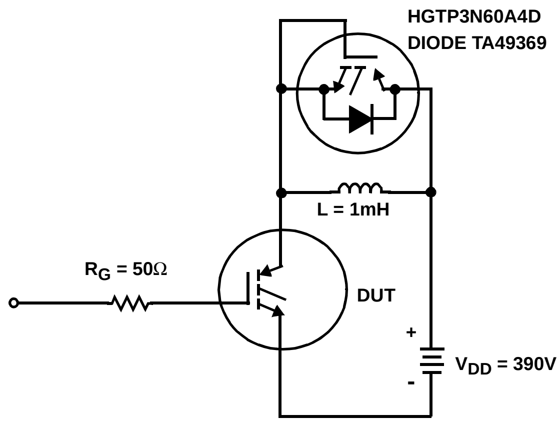



FIGURE 20. INDUCTIVE SWITCHING TEST CIRCUIT

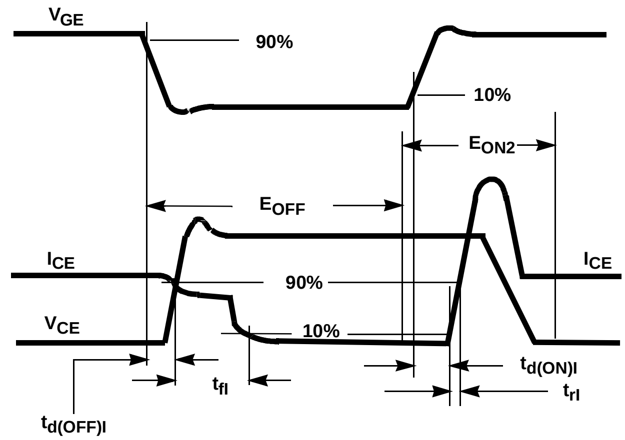



FIGURE 21. SWITCHING TEST WAVEFORMS

## Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as “ECCOSORBD™ LD26” or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of $V_{GEM}$. Exceeding the rated $V_{GE}$ can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic Zener diode from gate to emitter. If gate protection is required an external Zener is recommended.

## Operating Frequency Information

Operating frequency information for a typical device (Figure 3) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current ($I_{CE}$) plots are possible using the information shown for a typical unit in Figures 6, 7, 8, 9 and 11. The operating frequency plot (Figure 3) of a typical device shows $f_{MAX1}$ or $f_{MAX2}$; whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

$f_{MAX1}$ is defined by $f_{MAX1} = 0.05/(t_{d(OFF)I} + t_{d(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{d(OFF)I}$ and $t_{d(ON)I}$ are defined in Figure 21. Device turn-off delay can establish an additional frequency limiting condition for an application other than $T_{JM}$.

$f_{MAX2}$ is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON2})$. The allowable dissipation ($P_D$) is defined by $P_D = (T_{JM} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed $P_D$. A 50% duty factor was used (Figure 3) and the conduction losses ($P_C$) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

$E_{ON2}$ and $E_{OFF}$ are defined in the switching waveforms shown in Figure 21. $E_{ON2}$ is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and $E_{OFF}$ is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-off. All tail losses are included in the calculation for $E_{OFF}$; i.e., the collector current equals zero ($I_{CE} = 0$).

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|---|---|---|---|---|
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| ActiveArray™ | FAST® | MICROCOUPLER™ | PowerTrench® | SuperSOT™-8 |
| Bottomless™ | FASTr™ | MicroFET™ | QFET® | SyncFET™ |
| CoolFET™ | FRFET™ | MicroPak™ | QS™ | TinyLogic® |
| CROSSVOLT™ | GlobalOptoisolator™ | MICROWIRE™ | QT Optoelectronics™ | TINYOPTO™ |
| DOME™ | GTO™ | MSX™ | Quiet Series™ | TruTranslation™ |
| EcoSPARK™ | HiSeC™ | MSXPro™ | RapidConfigure™ | UHC™ |
| $E^2$CMOS™ | $I^2$C™ | OCX™ | RapidConnect™ | UltraFET® |
| EnSigna™ | ImpliedDisconnect™ | OCXPro™ | SILENT SWITCHER® | VCX™ |
| FACT™ | ISOPLANAR™ | OPTOLOGIC® | SMART START™ | |
| Across the board. Around the world.™ | | OPTOPLANAR™ | SPM™ | |
| The Power Franchise™ | | PACMAN™ | Stealth™ | |
| Programmable Active Droop™ | | POP™ | SuperSOT™-3 | |

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

| Datasheet Identification | Product Status | Definition |
|---|---|---|
| Advance Information | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| No Identification Needed | Full Production | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
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