

FQP9N25C / FQPF9N25C

N-Channel QFET® MOSFET

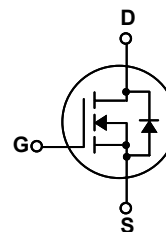
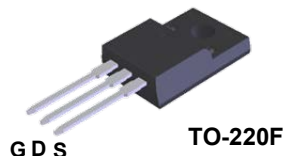
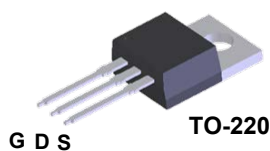
250 V, 8.8 A, 430 mΩ

Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor®'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 8.8 A, 250 V, $R_{DS(on)}=430\text{ m}\Omega(\text{Max.})@V_{GS}=10\text{ V}, I_D=4.4\text{ A}$
- Low Gate Charge (Typ. 26.5 nC)
- Low C_{rss} (Typ. 45.5 pF)
- 100% Avalanche Tested



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQP9N25C	FQPF9N25C	Unit
V_{DSS}	Drain-Source Voltage	250		V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 100^\circ\text{C}$)	8.8	8.8 *	A
		5.6	5.6 *	A
I_{DM}	Drain Current - Pulsed (Note 1)	35.2	35.2 *	A
V_{GSS}	Gate-Source Voltage	± 30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	285		mJ
I_{AR}	Avalanche Current (Note 1)	8.8		A
E_{AR}	Repetitive Avalanche Energy (Note 1)	7.4		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5		V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$) - Derate above 25°C	74	38	W
		0.59	0.3	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ\text{C}$

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	FQP9N25C	FQPF9N25C	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.69	3.29	$^\circ\text{C}/\text{W}$
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	$^\circ\text{C}/\text{W}$

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	250	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	--	0.30	--	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 250\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	μA
		$V_{DS} = 200\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 4.4\text{ A}$	--	0.35	0.43	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 4.4\text{ A}$ (Note 4)	--	7.0	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	545	710	pF
C_{oss}	Output Capacitance		--	115	150	pF
C_{riss}	Reverse Transfer Capacitance		--	45.5	60	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 125\text{ V}, I_D = 8.8\text{ A},$ $R_G = 25\ \Omega$	--	15	40	ns
t_r	Turn-On Rise Time		--	85	180	ns
$t_{d(off)}$	Turn-Off Delay Time		--	90	190	ns
t_f	Turn-Off Fall Time		(Note 4, 5)	--	65	140
Q_g	Total Gate Charge	$V_{DS} = 200\text{ V}, I_D = 8.8\text{ A},$ $V_{GS} = 10\text{ V}$	--	26.5	35	nC
Q_{gs}	Gate-Source Charge		--	3.5	--	nC
Q_{gd}	Gate-Drain Charge		(Note 4, 5)	--	13.5	--

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	8.8	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	35.2	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 8.8\text{ A}$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 8.8\text{ A},$	--	218	--	ns
Q_{rr}	Reverse Recovery Charge	$dI_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	1.58	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 5.9\text{ mH}, I_{AS} = 8.8\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 8.8\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\ \mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

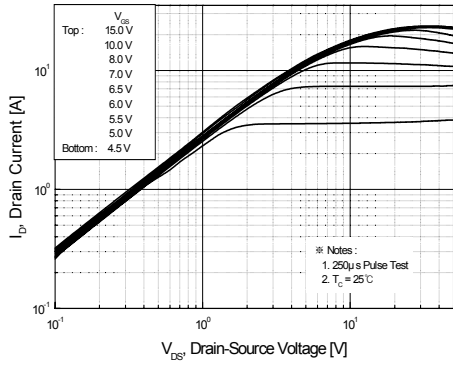


Figure 1. On-Region Characteristics

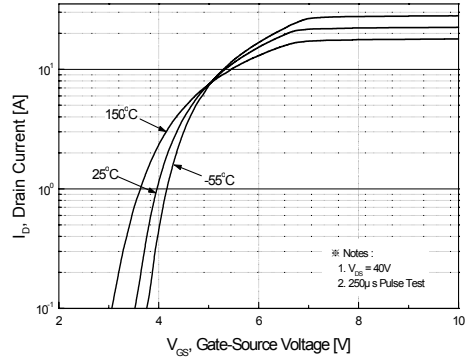


Figure 2. Transfer Characteristics

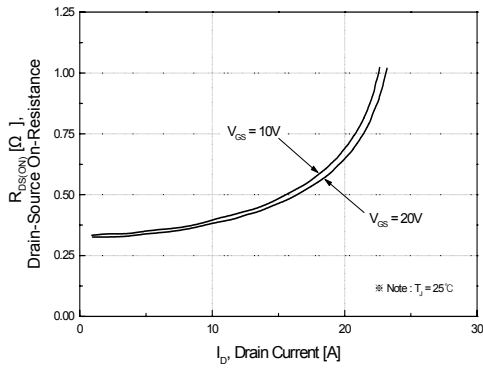


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

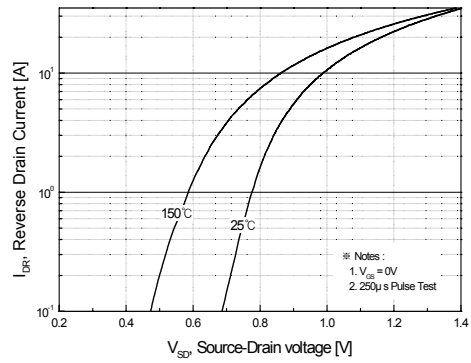


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

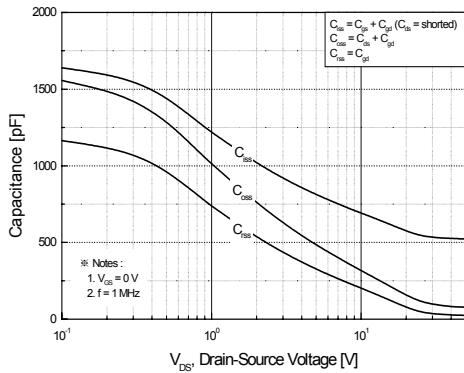


Figure 5. Capacitance Characteristics

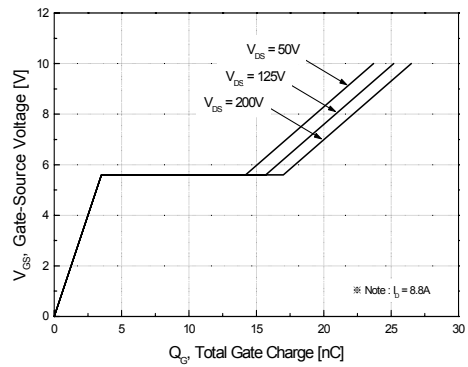


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

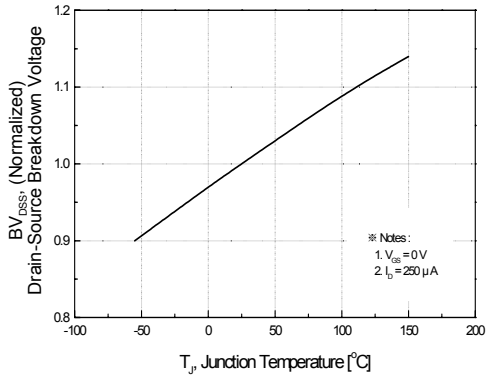


Figure 7. Breakdown Voltage Variation vs Temperature

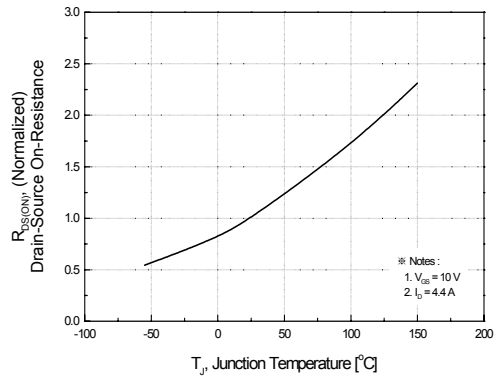


Figure 8. On-Resistance Variation vs Temperature

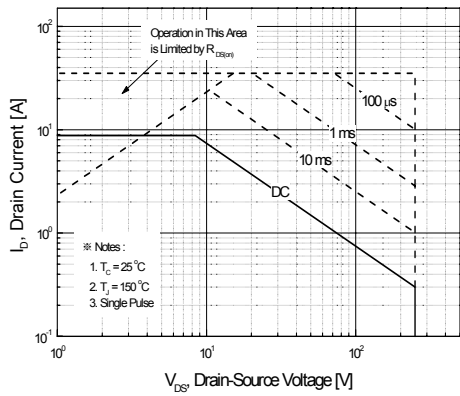


Figure 9-1. Maximum Safe Operating Area for FQP9N25C

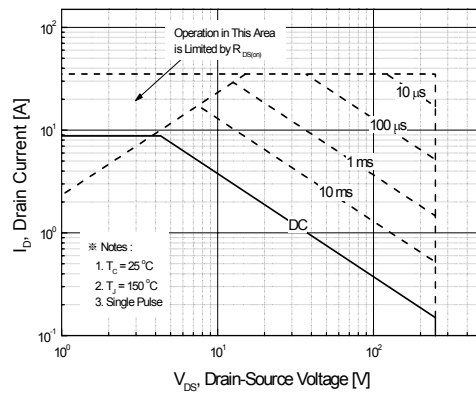


Figure 9-2. Maximum Safe Operating Area for FQPF9N25C

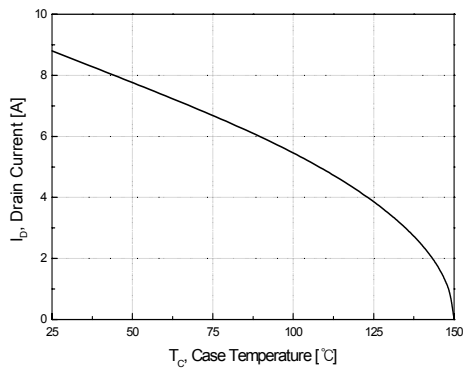


Figure 10. Maximum Drain Current vs Case Temperature

Typical Characteristics (Continued)

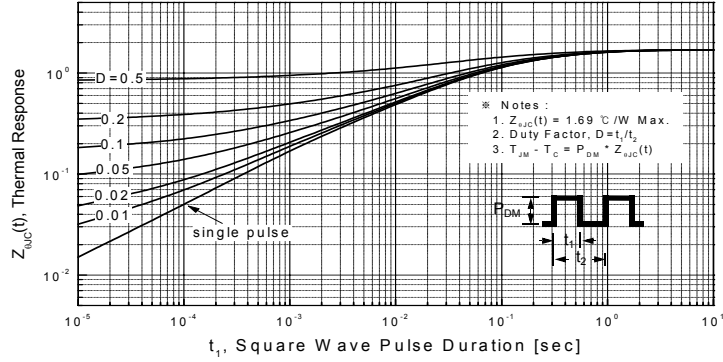


Figure 11-1. Transient Thermal Response Curve for FQP9N25C

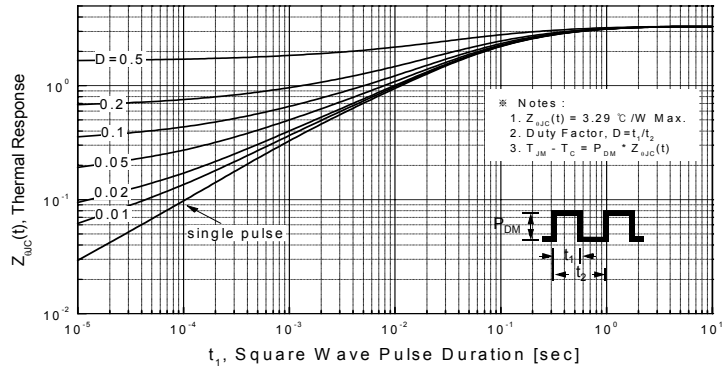
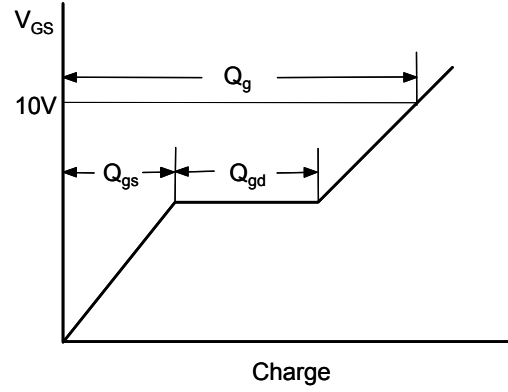
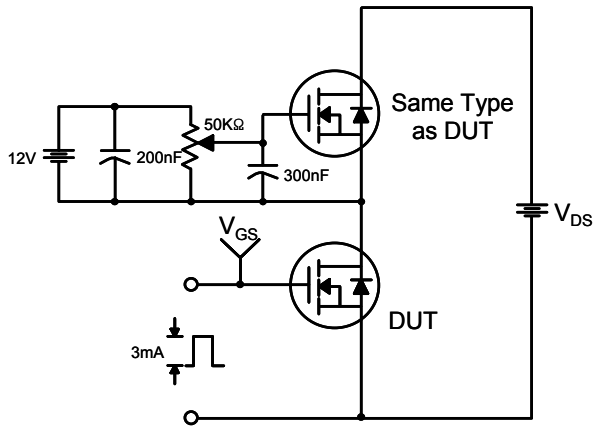
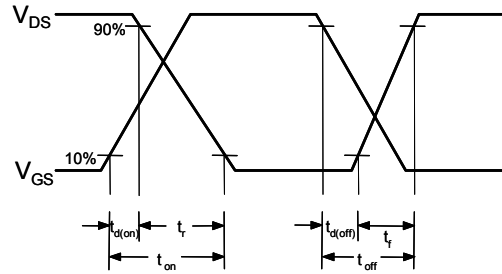
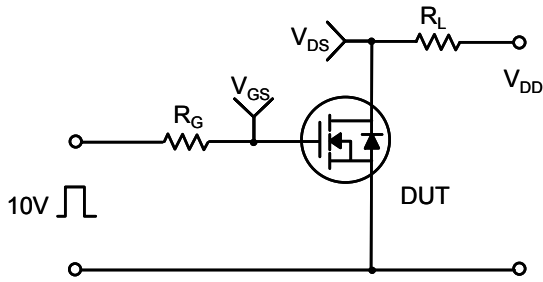


Figure 11-2. Transient Thermal Response Curve for FQPF9N25C

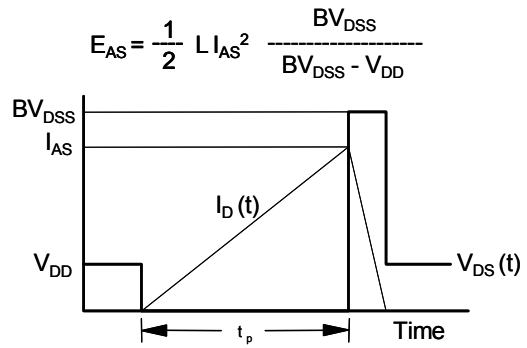
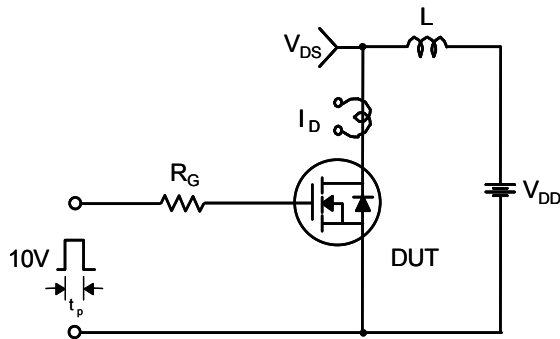
Gate Charge Test Circuit & Waveform



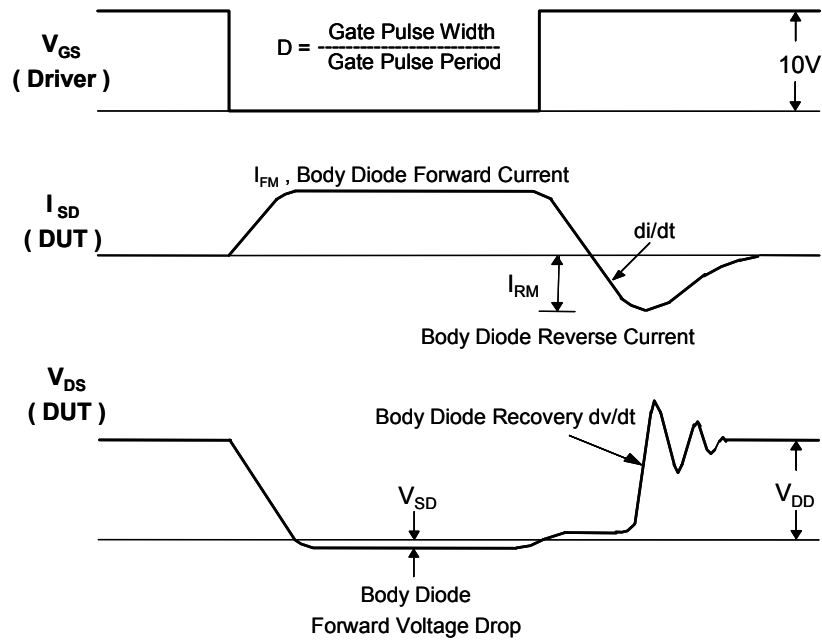
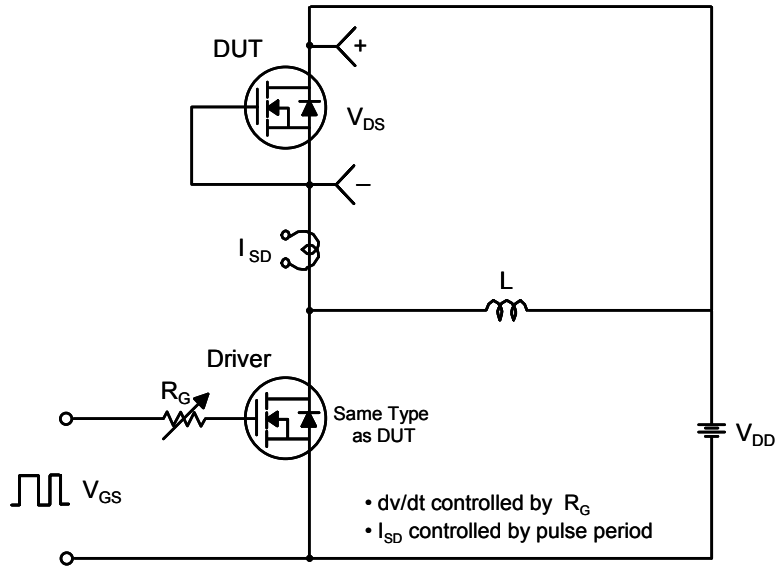
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

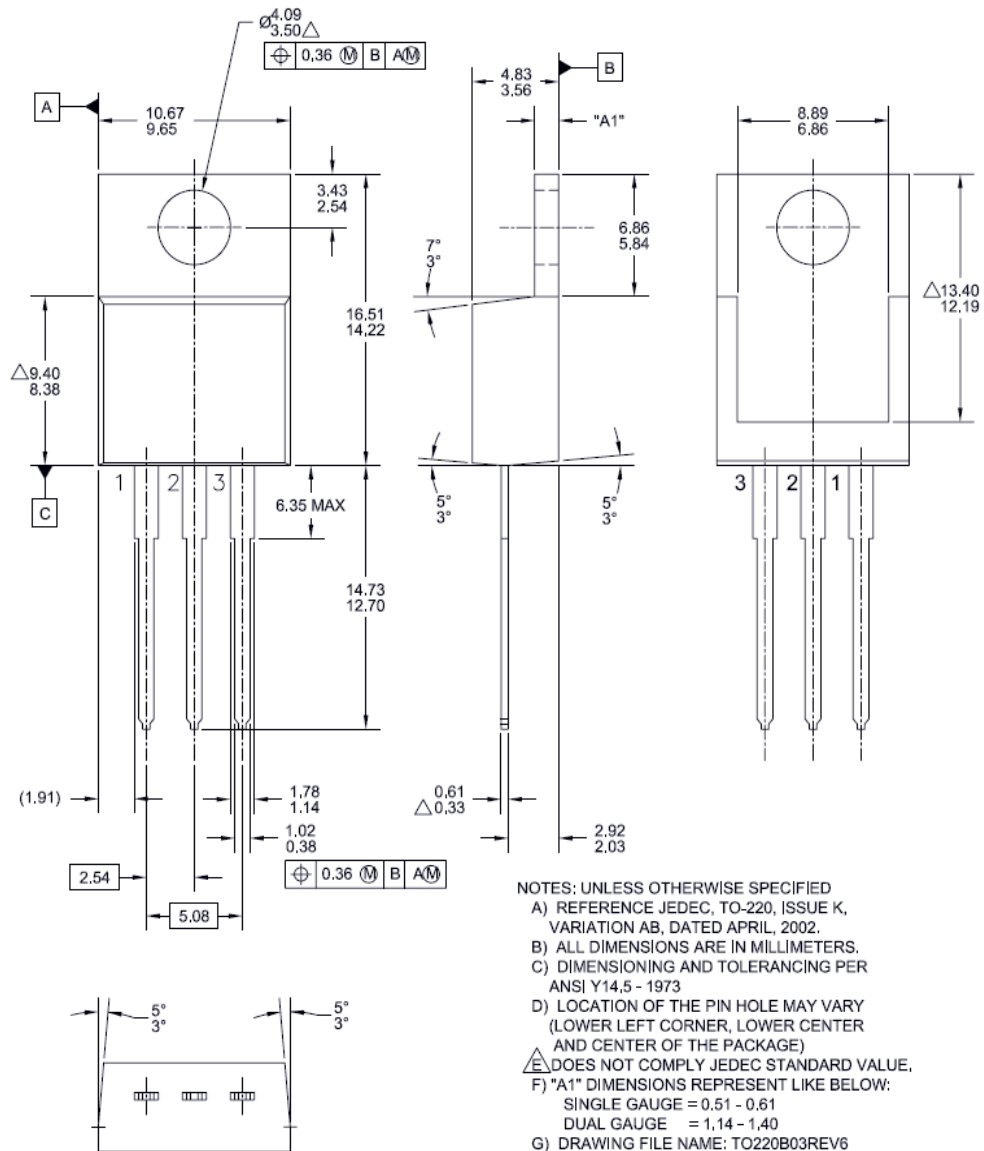


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

TO-220

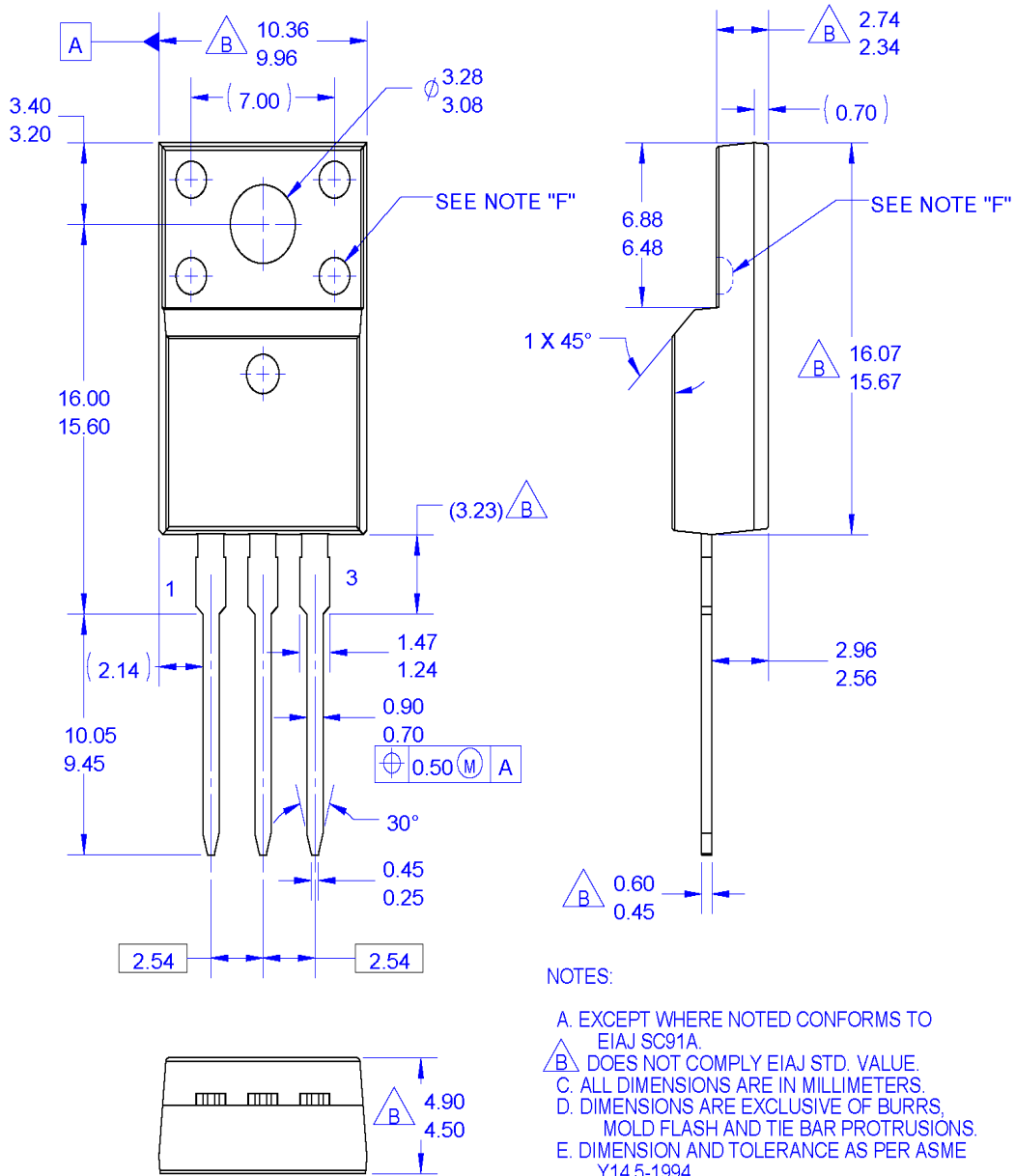


NOTES: UNLESS OTHERWISE SPECIFIED
 A) REFERENCE JEDEC, TO-220, ISSUE K, VARIATION AB, DATED APRIL, 2002.
 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1973
 D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
 E) Δ DOES NOT COMPLY JEDEC STANDARD VALUE.
 F) "A1" DIMENSIONS REPRESENT LIKE BELOW:
 SINGLE GAUGE = 0.51 - 0.61
 DUAL GAUGE = 1.14 - 1.40
 G) DRAWING FILE NAME: TO220B03REV6

Dimensions in Millimeters

Mechanical Dimensions

TO-220F



NOTES:



- A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
- B. DOES NOT COMPLY EIAJ STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- F. OPTION 1 - WITH SUPPORT PIN HOLE.
OPTION 2 - NO SUPPORT PIN HOLE.
- G. DRAWING FILE NAME: TO220M03REV3

Dimensions in Millimeters



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| Build it Now™ | Green Bridge™ | TinyCalc™ |
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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