

# FQD12P10 / FQU12P10

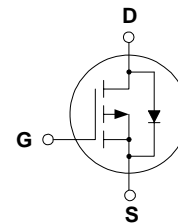
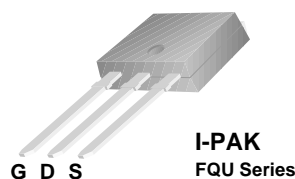
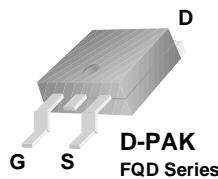
## 100V P-Channel MOSFET

### General Description

These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as audio amplifier, high efficiency switching DC/DC converters, and DC motor control.

### Features

- -9.4A, -100V,  $R_{DS(on)} = 0.29\Omega$  @  $V_{GS} = -10$  V
- Low gate charge ( typical 21 nC)
- Low  $C_{rss}$  ( typical 65 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- RoHS Compliant



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQD12P10 / FQU12P10	Units
$V_{DSS}$	Drain-Source Voltage	-100	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	-9.4	A
		-6.0	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	-37.6	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	370	mJ
$I_{AR}$	Avalanche Current (Note 1)	-9.4	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	5.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-6.0	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ ) *	2.5	W
	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	50	W
		0.4	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	2.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	50	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	$^\circ\text{C}/\text{W}$

\* When mounted on the minimum pad size recommended (PCB Mount)

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-100	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	-0.1	--	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}$	--	--	-1	$\mu\text{A}$
		$V_{DS} = -80\text{ V}, T_C = 125^\circ\text{C}$	--	--	-10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-2.0	--	-4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -4.7\text{ A}$	--	0.24	0.29	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = -40\text{ V}, I_D = -4.7\text{ A}$ (Note 4)	--	6.3	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	620	800	pF
$C_{oss}$	Output Capacitance		--	220	290	pF
$C_{riss}$	Reverse Transfer Capacitance		--	65	85	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -50\text{ V}, I_D = -11.5\text{ A},$ $R_G = 25\ \Omega$  (Note 4, 5)	--	15	40	ns
$t_r$	Turn-On Rise Time		--	160	330	ns
$t_{d(off)}$	Turn-Off Delay Time		--	35	80	ns
$t_f$	Turn-Off Fall Time		--	60	130	ns
$Q_g$	Total Gate Charge	$V_{DS} = -80\text{ V}, I_D = -11.5\text{ A},$ $V_{GS} = -10\text{ V}$  (Note 4, 5)	--	21	27	nC
$Q_{gs}$	Gate-Source Charge		--	4.6	--	nC
$Q_{gd}$	Gate-Drain Charge		--	11.5	--	nC

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	-9.4	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	-37.6	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -9.4\text{ A}$	--	--	-4.0	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = -11.5\text{ A},$ $dI_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	110	--	ns
$Q_{rr}$	Reverse Recovery Charge		--	0.47	--	$\mu\text{C}$

#### Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 6.3\text{ mH}, I_{AS} = -9.4\text{ A}, V_{DD} = -25\text{ V}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq -11.5\text{ A}, dI/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width  $\leq 300\ \mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

## Typical Characteristics

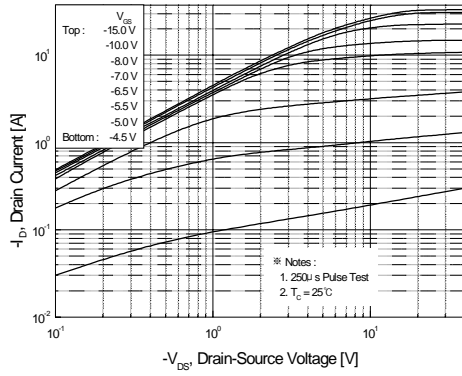


Figure 1. On-Region Characteristics

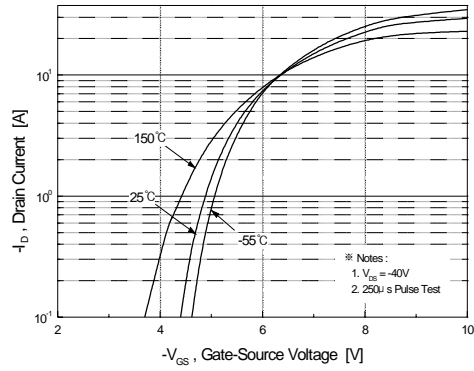


Figure 2. Transfer Characteristics

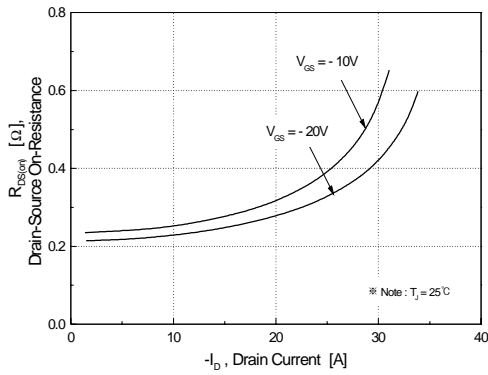


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

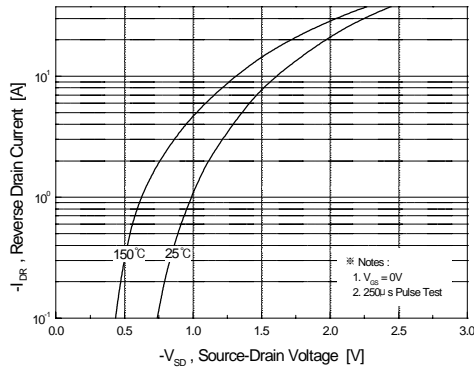


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

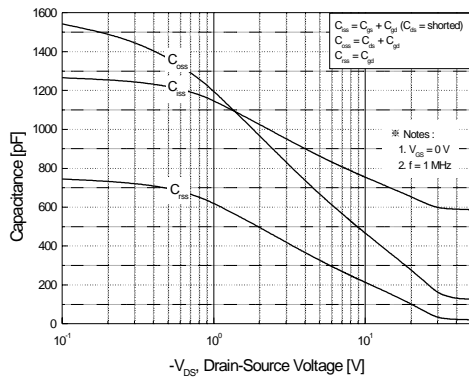


Figure 5. Capacitance Characteristics

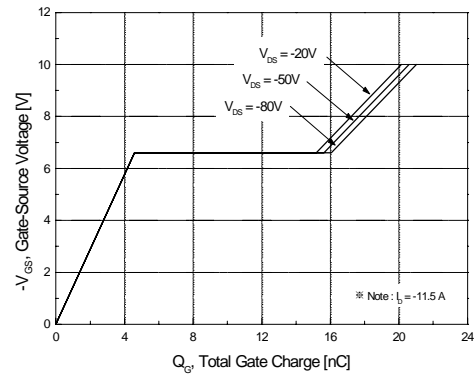
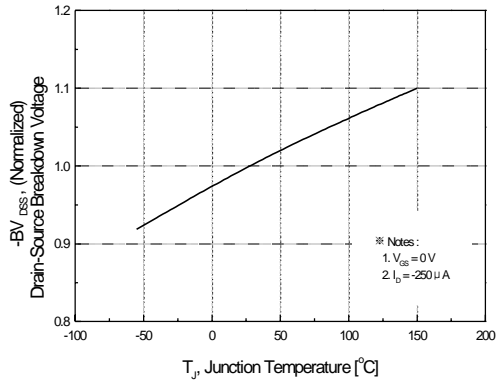
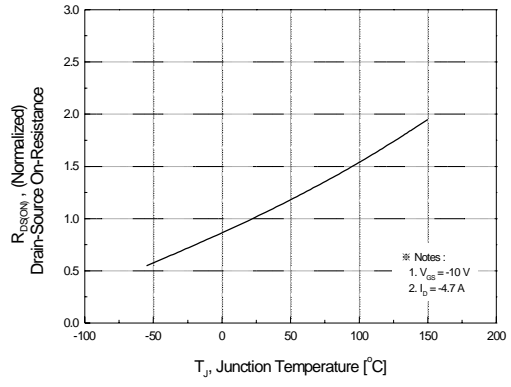


Figure 6. Gate Charge Characteristics

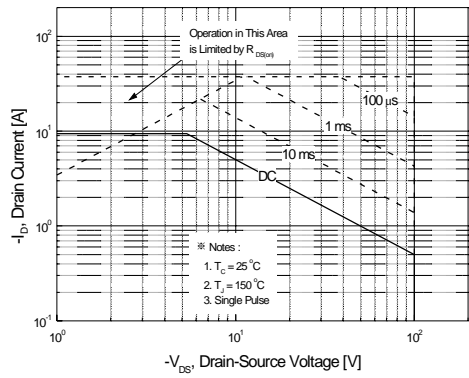
**Typical Characteristics** (Continued)



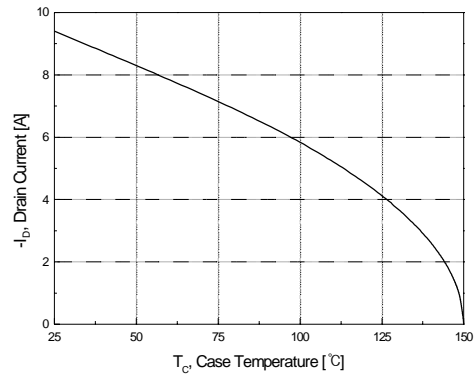
**Figure 7. Breakdown Voltage Variation vs. Temperature**



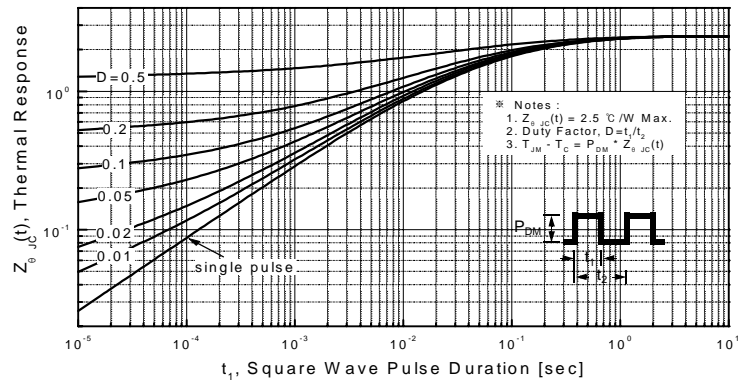
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**

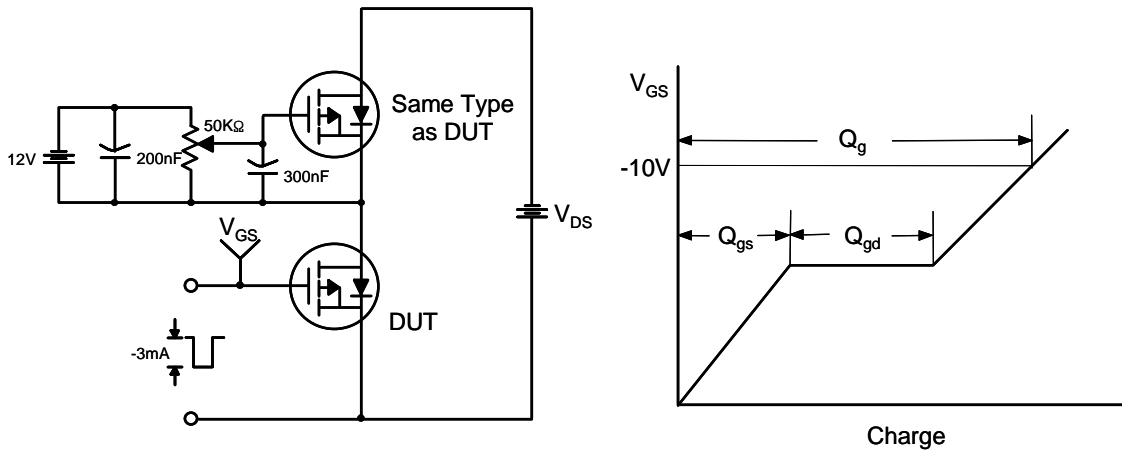


**Figure 10. Maximum Drain Current vs. Case Temperature**

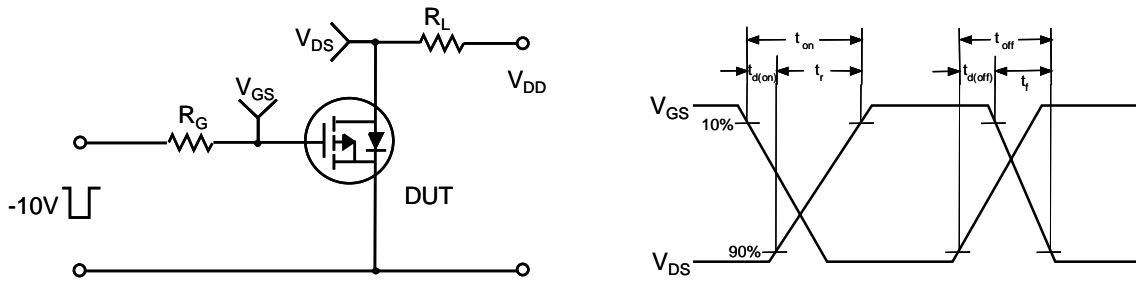


**Figure 11. Transient Thermal Response Curve**

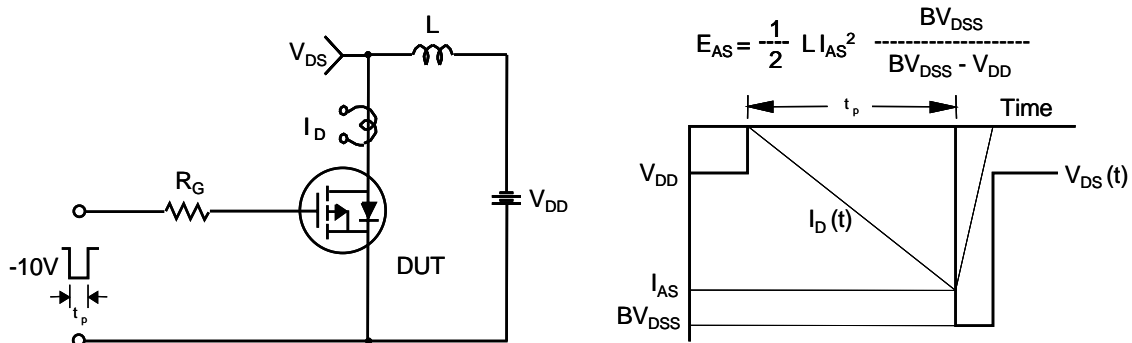
**Gate Charge Test Circuit & Waveform**



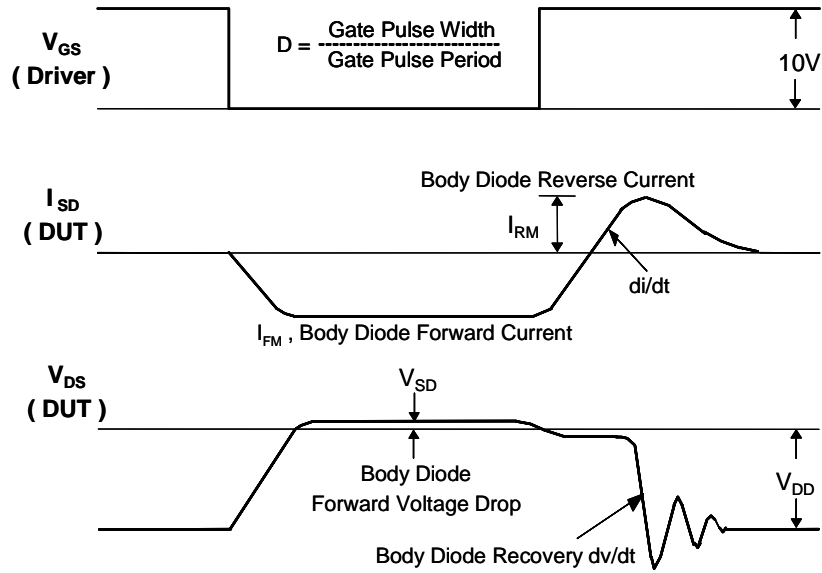
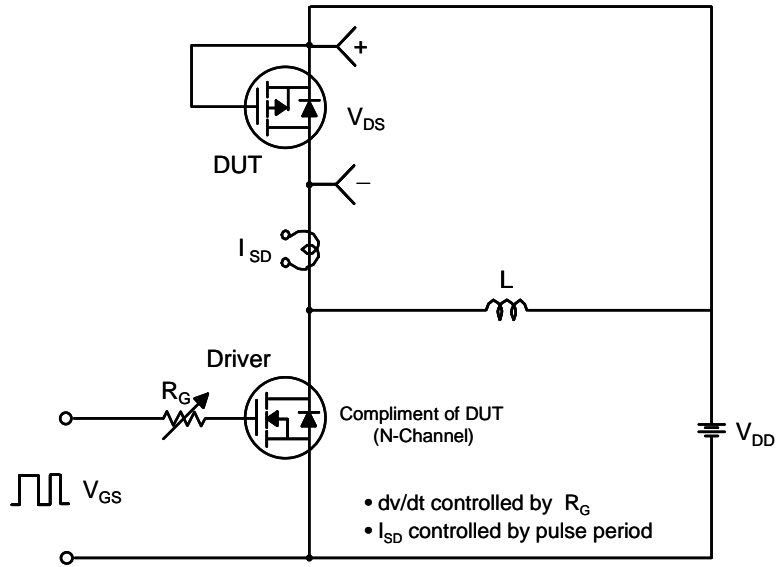
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

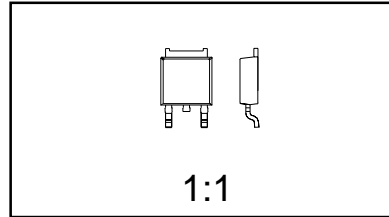
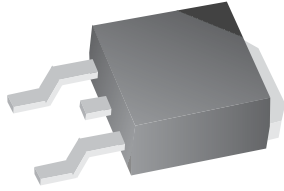


Peak Diode Recovery dv/dt Test Circuit & Waveforms



**Package Dimensions**

**TO-252 (DPAK) (FS PKG Code 36)**

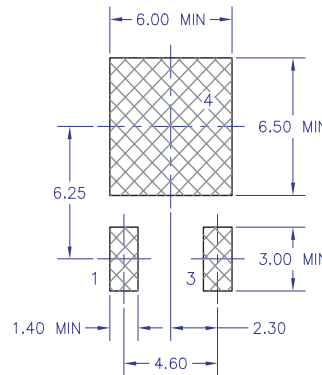
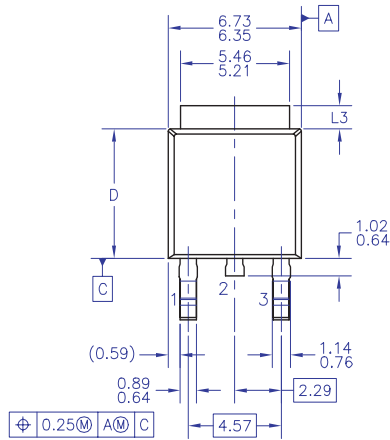


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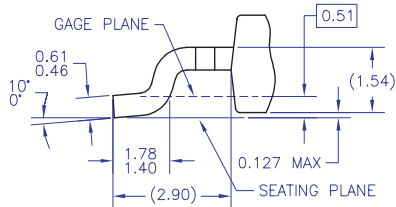
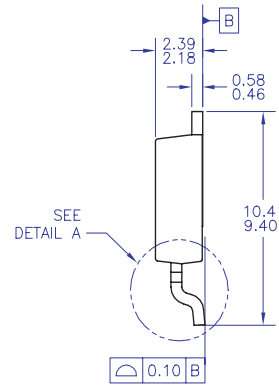
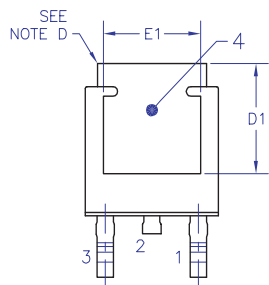
Scale 1:1 on letter size paper

Dimensions shown below are in:  
millimeters

Part Weight per unit (gram): 0.33



LAND PATTERN RECOMMENDATION



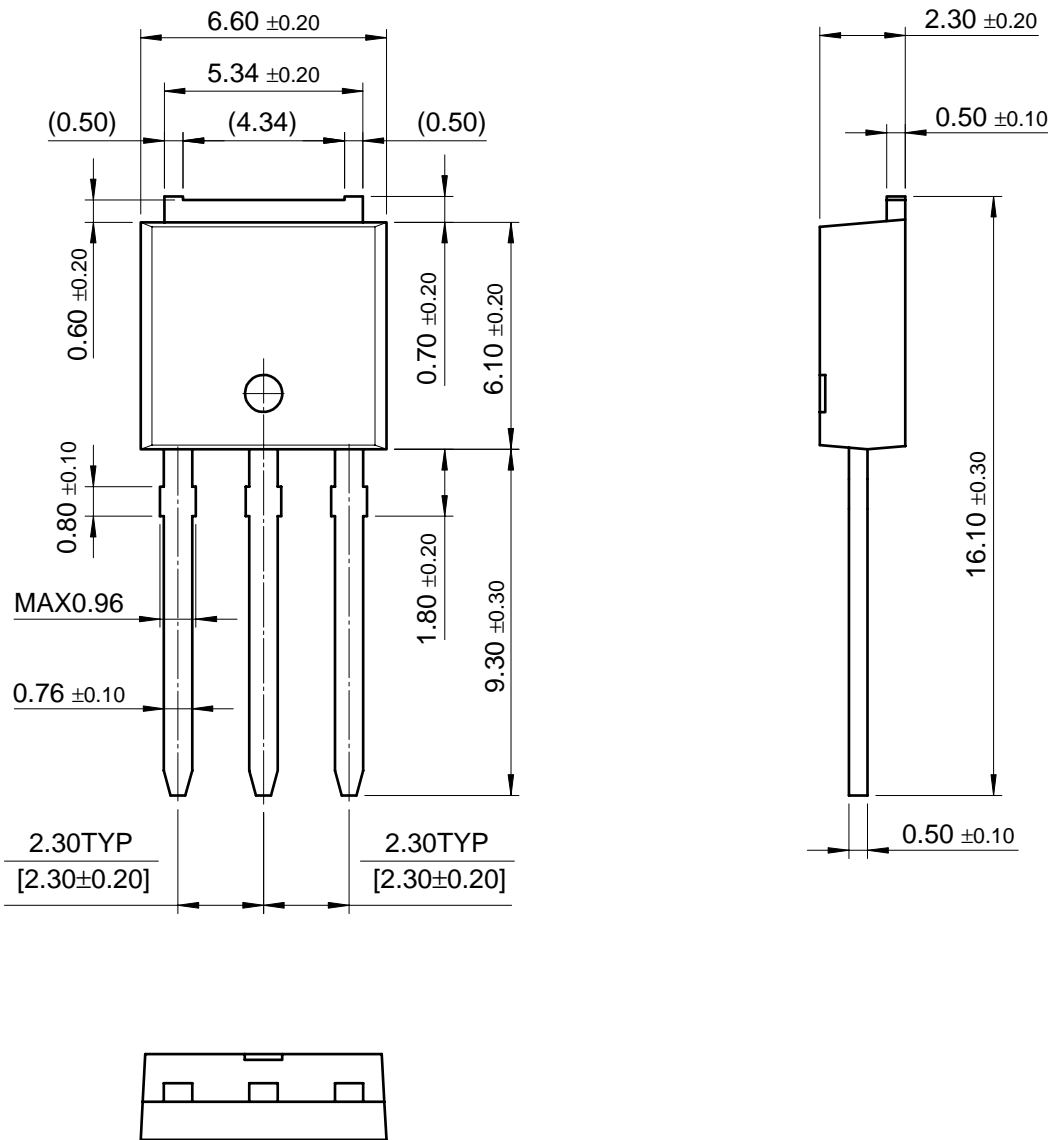
**DETAIL A**  
(ROTATED -90°)  
SCALE: 12X

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
  - B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) DIMENSIONS L3,D,E1&D1 TABLE:

	OPTION AA	OPTION AB
L3	0.89-1.27	1.52-2.03
D	5.97-6.22	5.33-5.59
E1	4.32 MIN	3.81 MIN
D1	5.21 MIN	4.57 MIN

Package Dimensions (Continued)

I-PAK



Dimensions in Millimeters






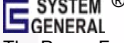
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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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