FAIRCHILD SEMICONDUCTOR®

January 2008

FMS3110 / FMS3115
Triple Video D/A Converters, 3x10-Bit, 150Ms/s

Features

- 10-bit Resolution
- 150 Megapixels per Second
- ± 0.1% Linearity Error
- /SYNC and /BLANK Controls
- 1.0V_{PP} Video into 37.5Ω or 75Ω Load
- Internal Bandgap Voltage Reference
- Double-buffered Data for Low Distortion
- TTL-compatible Inputs
- Low Glitch Energy
- Single +5V Power Supply

Applications

- Video Signal Conversion
  -RGB
  -YC_BC_R
  -Composite, Y, C
- Multimedia Systems
- Image Processing
- True-color Graphics Systems: 1 Billion Colors
- Broadcast Television Equipment
- High-Definition Television (HDTV) Equipment
- Direct Digital Synthesis

Description

FMS3110 / FMS3115 products are low-cost, triple D/A converters tailored for graphics and video applications where speed is critical. Two speed grades are available:

- FMS3110-100Ms/s
- FMS3115-150Ms/s

TTL-level inputs are converted to analog current outputs that can drive 25–37.5Ω loads corresponding to doubly terminated 50–75Ω loads. A sync current following /SYNC input timing is added to the I_{OG} output. /BLANK overrides RGB inputs, setting I_{OG}, I_{OB}, and I_{OR} currents to zero when /BLANK = L. Although appropriate for many applications, the internal 1.235V reference voltage can be overridden by the V_{REF} input.

Few external components are required: a current reference resistor, current output load resistors, and decoupling capacitors.

Package is a 48-lead LQFP. Fabrication technology is CMOS. Performance is guaranteed from 0 to 70°C.

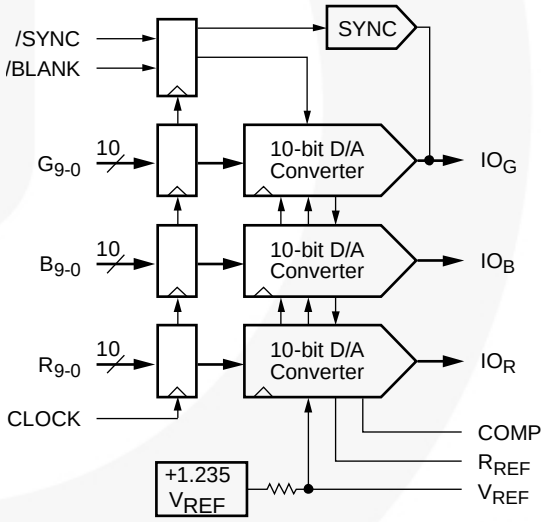

Figure 1. Block Diagram

Ordering Information

Part Numbers	Conversion Rate	Operating Temperature Range	Screening	Package
FMS3110KRC	100Ms/s	0 to 70°C	Commercial	48-Contact Leadless Quad Flat Package
FMS3115KRC	150Ms/s	0 to 70°C	Commercial	48-Contact Leadless Quad Flat Package

All packages are lead free per JEDEC: J-STD-020B standard.

Pin Configuration

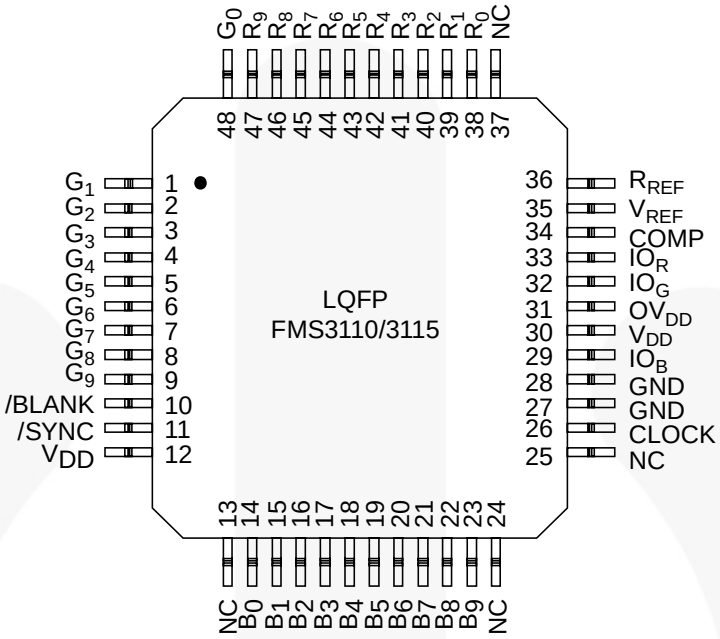

Figure 2. Pin Assignments

Pin Definitions

Name	Pin #	Value	Description
Clock / Pixel I/O			
CLK	26	TTL	**Clock Input**. The clock input is TTL-compatible and all pixel data is registered on the rising edge of CLK. It is recommended that CLK be driven by a dedicated TTL buffer to avoid reflection-induced jitter, overshoot, and undershoot.
R9-0	47-37	TTL	**Red Pixel Data Inputs**. TTL-compatible red data inputs are registered on the rising edge of CLK.
G9-0	48, 9–1	TTL	**Green Pixel Data Inputs**. TTL-compatible green data inputs are registered on the rising edge of CLK.
B9-0	23–14	TTL	**Blue Pixel Data Inputs**. TTL-compatible blue data inputs are registered on the rising edge of CLK.
Controls			
/SYNC	11	TTL	**Sync Pulse Input**. Bringing SYNC LOW turns off a 40 IRE (7.62 mA) current source which forms a sync pulse on the green D/A converter output. /SYNC is registered on the rising edge of CLK with the same pipeline latency as /BLANK and pixel data. /SYNC does not override any other data and should be used only during the blanking interval. Since this is a single-supply D/A and all signals are positive-going, /SYNC is added to the bottom of the green D/A range. Turning /SYNC OFF means turning the current source ON. When a sync pulse is desired, the current source is turned OFF. If the system does not require sync pulses from the green D/A converter, /SYNC should be connected to GND.
/BLANK	10	TTL	**Blanking Input**. When /BLANK is LOW, pixel inputs are ignored and the D/A converter outputs fall to the blanking level. /BLANK is registered on the rising edge of CLK and has the same pipeline latency as /SYNC.
Video Outputs			
IO_R	33	$0.714V_{pp}$	**Red Current Output**. The current source outputs of the D/A converters are capable of driving RS-343A/SMPTE-170M-compatible levels into doubly terminated 75Ω lines.
IO_G	32	$1V_{PP}$	**Green Current Output**. The current source outputs of the D/A converters are capable of driving RS-343A/SMPTE-170M-compatible levels into doubly terminated 75Ω lines. Sync pulses may be added to the green D/A output.
IOB	29	$0.714V_{PP}$	**Blue Current Output**. The current source outputs of the D/A converters are capable of driving RS-343A/SMPTE-170M-compatible levels into doubly terminated 75Ω lines.
Voltage Reference			
V_{REF}	35	+1.235V	**Voltage Reference Output/Input**. An internal voltage source of +1.235V is output on this pin. An external +1.235V reference may be applied here to override the internal reference. Decoupling VREF to GND with a 0.1µF ceramic capacitor is required.
V_{REF}	36	560Ω	**Current-Setting Resistor**. Full-scale output current of each D/A converter is determined by the value of the resistor connected between R_{REF} and GND. Nominal value of R_{REF} is found from: $R_{REF} = 9.1 (V_{REF}/I_{FS})$ where I_{FS} is the full-scale (white) output current (in amps) from the D/A converter (without sync). Sync is $0.4 \bullet I_{FS}$. D/A full-scale (white) current may also be calculated from: $I_{FS} = V_{FS}/R_L$ where V_{FS} is the white voltage level and R_L is the total resistive load (in Ω) on each D/A converter. V_{FS} is the blank to full-scale voltage.
COMP	34	0.1µF	**Compensation Capacitor**. A 0.1µF ceramic capacitor must be connected between COMP and V_{DD} to stabilize internal bias circuitry.
Power and Ground			
V_{DD}	12, 30, 31	+5V	**Power Supply**.
GND	27, 28	0.0V	**Ground**.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. *See Figure 4*.

Symbol	Parameter	Min.	Max.	Unit
Power Supply Voltage				
V_{DD}	Measured to Ground	-0.5	7.0	V
Inputs				
V_{IN_A}	Applied Voltage, Measured to Ground[1]	-0.5	V_{DD}+0.5	V
I_{IN_F}	Forced Current[2, 3]	-10	+10	mA
Outputs				
V_{OUT_A}	Applied Voltage, Measured to Ground[1]	-0.5	V_{DD}+0.5	V
I_{OUT_F}	Forced Current[2, 3]	-60	+60	mA
t_{SC}	Short-Circuit Duration, Single Output in HIGH State to Ground		Infinite	s
Temperature				
T_A	Operating Ambient Temperature	-20	+110	°C
T_J	Junction Temperature		+150	°C
T_L	Lead Soldering, 10 Seconds		+300	°C
T_{VP}	Vapor Phase Soldering, 1 Minute		+220	°C
T_{STG}	Storage Temperature	-65	+150	°C

Notes:
1. Applied voltage must be current limited to specified range.
2. Forcing voltage must be limited to specified range.
3. Current is specified as conventional current flowing into the device.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Nom.	Max.	Unit
V_{DD}	Power Supply Voltage		4.75	5.00	5.25	V
f_S	Conversion Rate	FMS3110			100	Msps
		FMS3115			150	
t_{PWH}	CLK Pulse-width, HIGH	FMS3110	3.1			ns
		FMS3115	2.5			
t_{PWL}	CLK Pulse-width, LOW	FMS3110	3.1			ns
		FMS3115	2.5			
t_W	CLK Pulse-width	FMS3110	10			ns
		FMS3115	6.6			
t_S	Input Data Setup Time		1.7			ns
t_h	Input Data Hold Time		0			ns
V_{REF}	Reference Voltage, External		1.000	1.235	1.500	V
C_C	Compensation Capacitor			0.1		µF
R_{LOAD}	Output Load			37.5		Ω
V_{IH}	Input Voltage, Logic HIGH		2.0		V_{DD}	V
V_{IL}	Input Voltage, Logic LOW		GND		0.8	V
T_A	Ambient Temperature, Still Air		0		70	°C

Electrical Characteristics

Symbol	Parameter	Conditions[6]	Min.	Typ.[4]	Max.	Units
I_{DD}	Power Supply Current[5]	V_{DD}=Max.			125	mA
P_D	Total Power Dissipation[5]	V_{DD}=Max.			655	mW
R_O	Output Resistance			100		kΩ
C_O	Output Capacitance	I_{OUT}=0mA			30	pF
I_{IH}	Input Current HIGH	V_{DD}=Max., V_{IN}=2.4V			-5	µA
I_{IL}	Input Current LOW	V_{DD}=Max., V_{IN}=0.4			+5	µA
I_{REF}	V_{REF} Input Bias Current			0	±100	µA
V_{REF}	Reference Voltage Output			1.235		V
V_{OC}	Output Compliance	Referred to V_{DD}	-0.4	0	+1.5	V
C_{DI}	Digital Input Capacitance			4	10	pF

Notes:
4. Values shown are typical for V_{DD}=+5V and T_A=25°C.
5. Minimum and Maximum values with V_{DD}=Max and T_A=Min.
6. V_{REF}=1.235V, R_{LOAD}=37.5Ω, R_{REF}=540Ω.

Switching Characteristics

Symbol	Parameter	Conditions[8]	Min.	Typ.[7]	Max.	Units
t_D	Clock to Output Delay	V_{DD}=Min.		10	15	ns
t_{SKEW}	Output Skew			1	2	ns
t_R	Output Rise Time	10% to 90% of Full Scale			3	ns
t_F	Output Fall Time	90% to 10% of Full Scale			3	ns

Notes:
7. Values shown are typical for V_{DD}=+5V and T_A=25°C.
8. V_{REF}=1.235V, R_{LOAD}=37.5Ω, R_{REF}=590Ω.

System Performance Characteristics See Figure 3

Symbol	Parameter	Conditions[10]	Min.	Typ.[9]	Max.	Units
ELI	Integral Linearity Error	V_{DD}, V_{REF}=Nominal		±0.10	±0.25	%/FS
ELD	Differential Linearity Error	V_{DD}, V_{REF}=Nominal		±0.10	±0.25	%/FS
EDM	DAC to DAC Matching	V_{DD}, V_{REF}=Nominal		3	10	%
PSRR	Power Supply Rejection Ratio				0.05	%/%

Notes:
9. Values shown are typical for V_{DD}=+5V and T_A=25°C.
10. V_{REF}=1.235V, R_{LOAD}=37.5Ω, R_{REF}=590Ω.

Timing Information

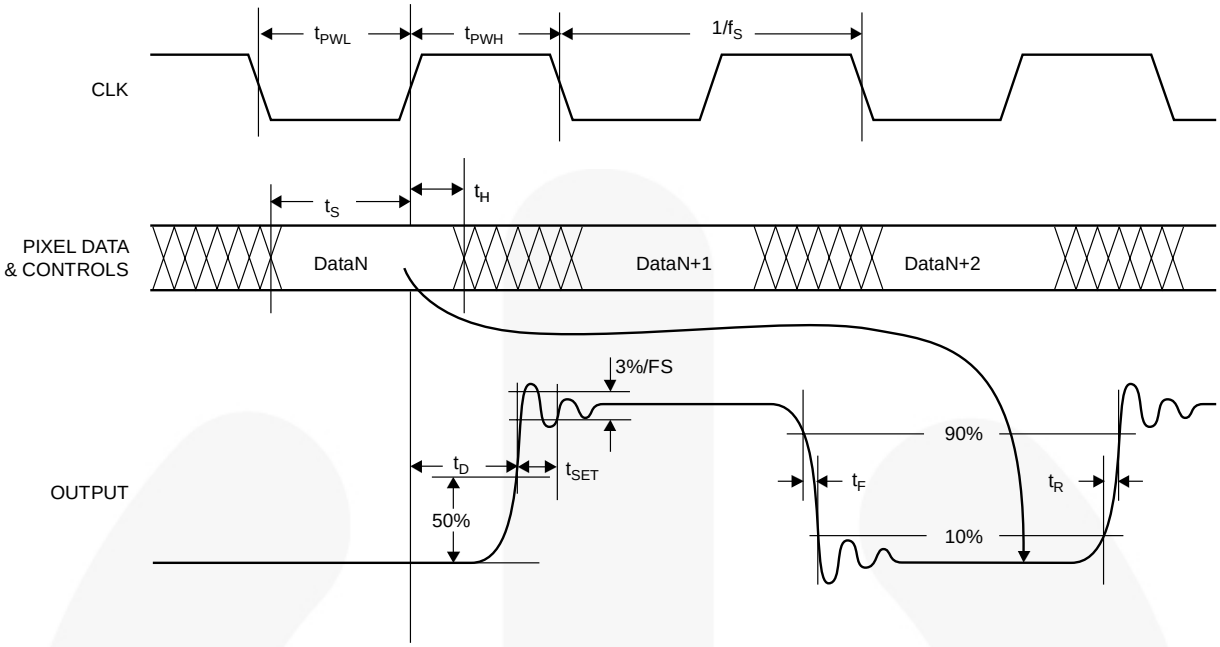

Figure 3. Timing Diagram

Equivalent Circuits

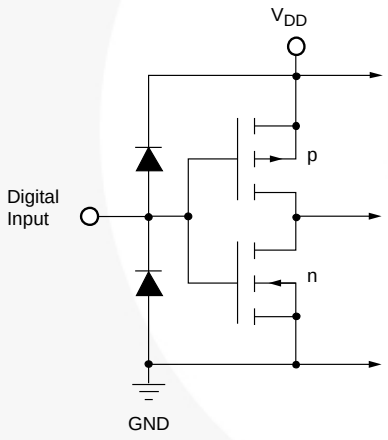

Figure 4. Equivalent Digital Input Circuit

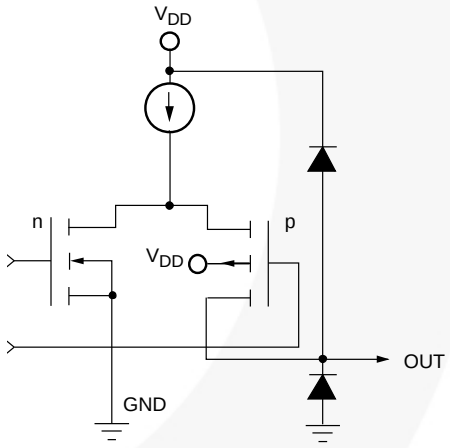

Figure 5. Equivalent Analog Output Circuit

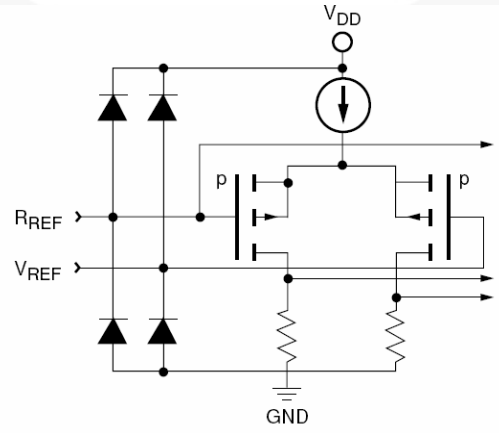

Figure 6. Equivalent Analog Input Circuit

Functional Description

Within the FMS3110/3115 are three identical 10-bit D/A converters, each with a current source output. External loads are required to convert the current to voltage outputs. Data inputs RGB7-0 are overridden by the /BLANK input. /SYNC = H activates sync current from I_{OS} for sync-on-green video signals.

Digital Inputs

All digital inputs are TTL-compatible. Data is registered on the rising edge of the CLK signal. Following one stage of pipeline delay, the analog output changes t_{DO} after the rising edge of CLK.

/SYNC and /BLANK

/SYNC and /BLANK inputs control the output level (Figure 7 and Table 1) of the D/A converters during CRT retrace intervals. /BLANK forces the D/A outputs to the blanking level, while /SYNC = L turns off a current source connected to the green D/A converter. /SYNC = H adds a 40 IRE sync pulse to the green output; /SYNC = L sets the green output to 0.0V during the sync tip. /SYNC and /BLANK are registered on the rising edge of CLK.

/BLANK gates the D/A inputs and sets the pedestal voltage. If /BLANK = HIGH, D/A inputs are added to a pedestal, which offsets the current output. If /BLANK = LOW, data inputs and the pedestal are disabled.

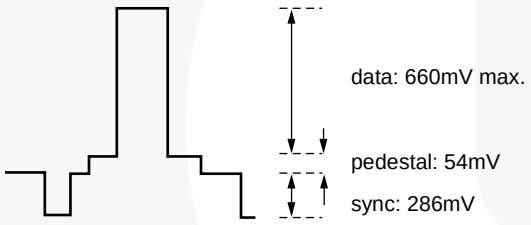

Figure 7. Nominal Output Levels

D/A Outputs

Each D/A output is a current source. To obtain a voltage output, a resistor must be to ground. Output voltage depends upon this external resistor, the reference voltage, and the value of the gain-setting resistor connected between R_{REF} and GND.

Normally, a 75Ω source termination resistor is connected between the D/A current output pin and GND near the D/A converter. A 75Ω line can be connected with another 75Ω termination resistor at the far end of the cable. This “double termination” presents the D/A converter a net resistive load of 37.5Ω.

The FMS3110/3115 may also be operated with a single 75Ω terminating resistor. To lower the output voltage swing to the desired range, the nominal value of the resistor on R_{REF} should be doubled.

Voltage Reference

All three D/A converters are supplied with a common voltage reference. Internal bandgap voltage reference voltage is +1.235V with a 3KΩ source resistance. An external voltage reference may be connected to the V_{REF} pin, overriding the internal voltage reference.

A 0.1µF capacitor must be connected between the COMP pin and V_{DD} to stabilize internal bias circuitry and ensure low-noise operation.

Power and Ground

Required power is a single +5.0V supply. To minimize power-supply induced noise, analog +5V should be connected to V_{DD} pins with 0.1 and 0.01µF decoupling capacitors placed adjacent to each V_{DD} pin or pin pair.

The high slew-rate of digital data makes capacitive coupling to the outputs of any D/A converter a potential problem. Since the digital signals contain high-frequency components of the CLK signal, as well as the video output signal, the resulting data feed-through often looks like harmonic distortion or reduced signal-to-noise performance. All ground pins should be connected to a common solid ground plane for best performance.

Table 1. Output Voltage vs. Input Code, /SYNC and /BLANK (V_{REF}=1.235V, R_{REF}=590Ω, R_L=37.5Ω)

RGB_{9-0}(MSB…LSB)	Blue and Red D/As			Green D/A		
	/SYNC	/BLANK	V_{OUT}	/SYNC	/BLANK	V_{OUT}
11 1111 1111	X	1	0.7140	1	1	1.0000
11 1111 1111	X	1	0.7140	0	1	0.7140
11 1111 1110	X	1	0.7134	1	1	0.9994
11 1111 1101	X	1	0.7127	1	1	0.9987
:	:	:	:	:	:	:
10 0000 0000	X	1	0.3843	1	1	0.6703
01 1111 1111	X	1	0.3837	1	1	0.6697
:	:	:	:	:	:	:
00 0000 0010	X	1	0.0553	1	1	0.3413
00 0000 0001	X	1	0.0546	1	1	0.3406
00 0000 0000	X	1	0.0540	1	1	0.3400
XX XXXX XXXX	X	0	0.0000	1	0	0.2860
XX XXXX XXXX	X	0	0.0000	0	0	0.0000

Application Information

Figure 8 illustrates a typical FMS3110/3115 interface circuit. In this example, an optional 1.2V bandgap reference is connected to the V_{REF} output, overriding the internal voltage reference source.

Grounding

It is important that the FMS3110/3115 power supply be well-regulated and free of high-frequency noise. Careful power supply decoupling ensures the highest quality video signals at the output of the circuit. The FMS3110/3115 has separate analog and digital circuits. To keep digital system noise from the D/A converter, it is recommended that power supply voltages (V_{DD}) come from the system analog power source and all ground connections (GND) be made to the analog ground plane. Power supply pins should be individually decoupled at the pin.

Printed Circuit Board Layout

Designing with high-performance mixed-signal circuits demands printed circuits with ground planes. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor D/A conversion. Consider the following suggestions when designing the layout:

1. Keep the critical analog traces (V_{REF}, I_{REF}, COMP, I_{OS}, I_{OR}, I_{OG}) as short as possible and as far as possible from all digital signals. The FMS3110/3115 should be located near the board edge, close to the analog output connectors.
2. The power plane for the FMS3110/3115 should be separate from that which supplies the digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the power supply for the FMS3110/3115 is the same as that of the system's digital circuitry, power to the FMS3110/3115 should be decoupled with 0.1µF and 0.01µF capacitors and isolated with a ferrite bead.
3. The ground plane should be solid, not cross-hatched. Connections to the ground plane should have very short leads.
4. If the digital power supply has a dedicated power plane layer, it should not be placed under the FMS3110/3115, the voltage reference, or the analog outputs. Capacitive coupling of digital power supply noise from this layer to the FMS3110/3115 and its related analog circuitry can have an adverse effect on performance.
5. CLK should be handled carefully. Jitter and noise on this clock degrade performance. Terminate the clock line carefully to eliminate overshoot and ringing.

Related Products

- FMS38XX Triple 8-bit 150Msp D/A Converters
- FMS9884A 3x8-bit 140Ms/s A/D Converter

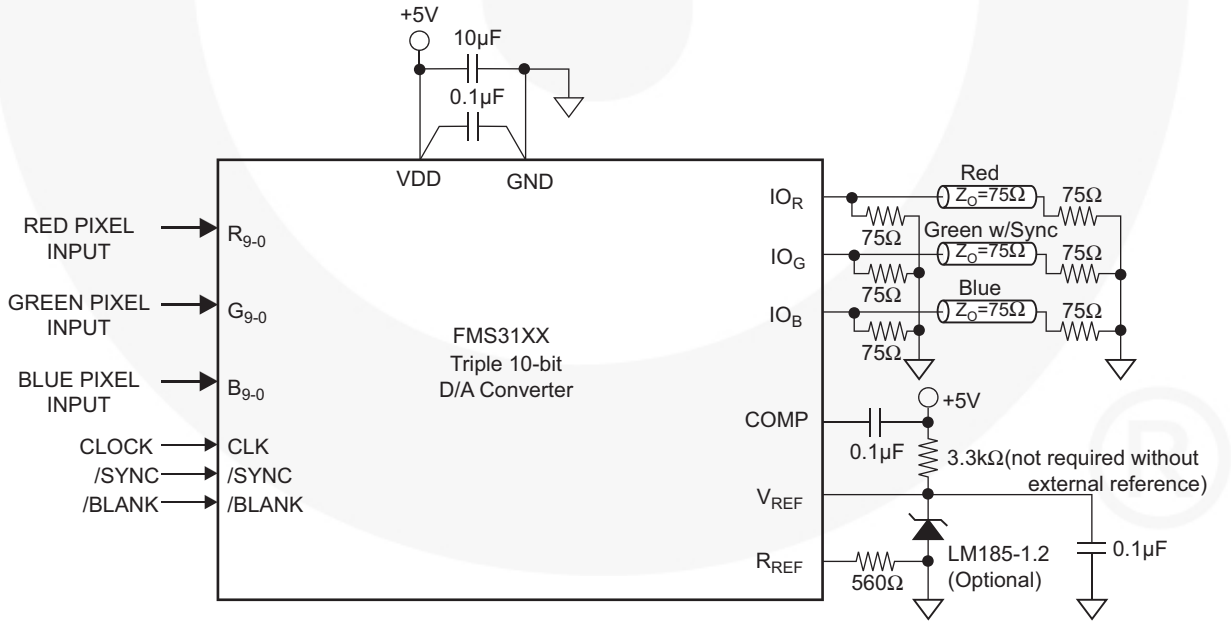

Figure 8. Typical Interface Circuit

Physical Dimensions

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.055	.063	1.40	1.60	
A1	.001	.005	.05	.15	
A2	.053	.057	1.35	1.45	
B	.006	.010	.17	.27	7
D/E	.346	.362	8.8	9.2	8
D1/E1	.268	.284	6.8	7.2	2
e	.019 BSC		.50 BSC		
L	.017	.029	.45	.75	6
N	48		48		4
ND	12		12		5
α	0	7	0	7	
ccc	.004		0.08		

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Dimensions "D1" and "E1" do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Pin 1 identifier is optional.
4. Dimension ND: Number of terminals.
5. Dimension ND: Number of terminals per package edge.
6. "L" is the length of terminal for soldering to a substrate.
7. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum B dimension by more than 0.08mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm for 0.4mm and 0.5mm pitch packages.
8. To be determined at seating place ÑCÑ

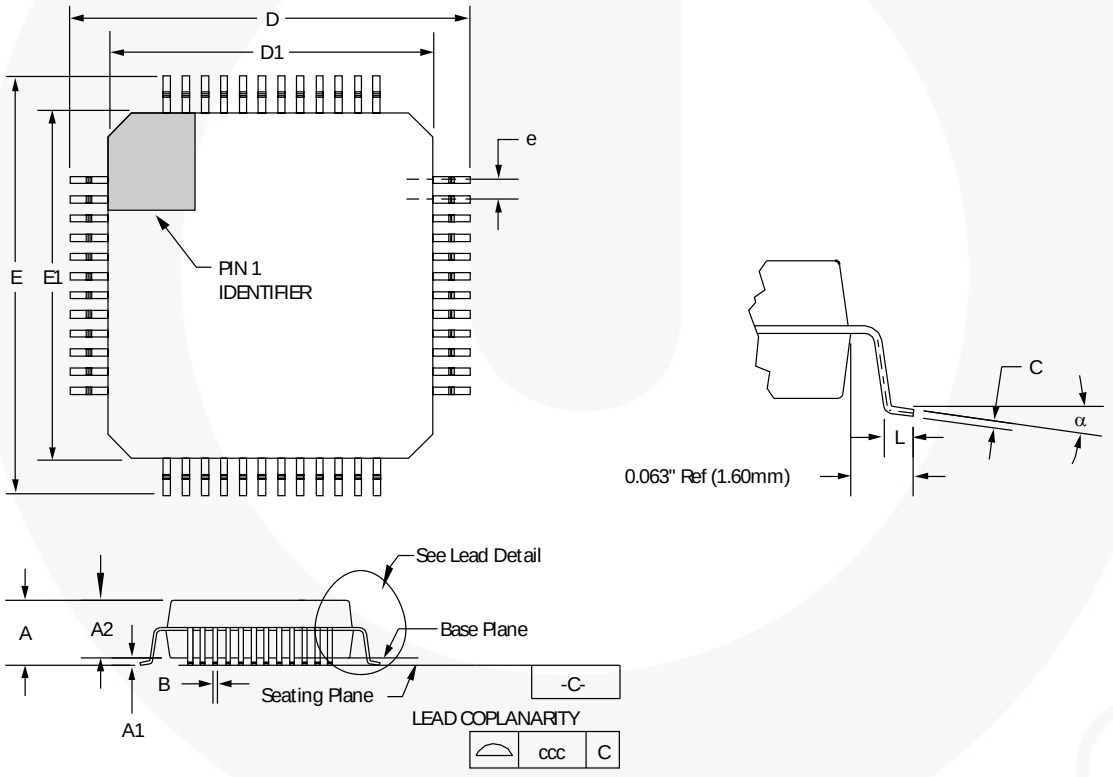

Figure 9. 48-Contact Leadless Quad Flat Package (LMQFP)

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