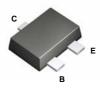




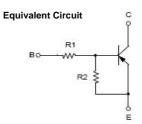
# FJY4004R PNP Epitaxial Silicon Transistor

## **Features**

- · Switching circuit, Inverter, Interface circuit, Driver Circuit
- Built in bias Resistor (R<sub>1</sub>=47K $\Omega$ , R<sub>2</sub>=47K $\Omega$ )
- Complement to FJY3004R







# Absolute Maximum Ratings \* Ta = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V <sub>CBO</sub>	Collector-Base Voltage	-50	V
V <sub>CEO</sub>	Collector-Emitter Voltage	-50	V
V <sub>EBO</sub>	Emitter-Base Voltage	-10	V
I <sub>C</sub>	Collector Current	-100	mA
T <sub>STG</sub>	Storage Temperature Range	-55~150	°C
T <sub>J</sub>	Junction Temperature	150	°C
P <sub>C</sub>	Collector Power Dissipation, by $R_{\theta JA}$	200	mW

С

**S54** 

# Thermal Characteristics\* Ta=25°C unless otherwise noted

Symbol	Parameter	Max	Units	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	600	°C/W	

<sup>\*</sup> Minimum land pad size.

# Electrical Characteristics\* T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	Test Condition	MIN	Тур	MAX	Units
V <sub>(BR)</sub> CBO	Collector-Emitter Breakdown Voltage	Ic = -10 uA, IE = 0	-50			V
V <sub>(BR)</sub> CEO	Collector-Base Breakdown Voltage	Ic = -100 uA, I <sub>B</sub> = 0	-50			V
Ісво	Collector-Cutoff Current	Vcb = -40 V, IE = 0			-0.1	uA
hfe	DC Current Gain	Vce = -5 V, Ic = -5mA	68			
VcE(sat)	Collector-Emitter Saturation Voltage	Ic = -10 mA, I <sub>B</sub> = -0.5 mA			-0.3	V
f⊤	Current Gain - Bandwidth Product	Vce = -10V, Ic = -5 mA		200		MHz
Ccb	Output Capacitance	Vcb = -10 V, IE = 0, f = 1.0 MHz		5.5		pF
Vı(off)	Input Off Voltage	Vc= -5 V, Ic = -100uA	-0.5			V
V <sub>I</sub> (on)	Input On Voltage	Vce = -0.3V, Ic = -2mA			-3.0	V
R <sub>1</sub>	Input Resistor		32	47	62	ΚΩ
R <sub>1</sub> /R <sub>2</sub>	Resistor Ratio		0.9	1.0	1.1	

<sup>\*</sup> Pulse Test: PW≤300μs, Duty Cycle≤2%

<sup>\*</sup> These ratings are limiting values above which the serviceability of any semiconductor device may by impaired.

# **Typical Performance Characteristics**

Figure 1. DC current Gain

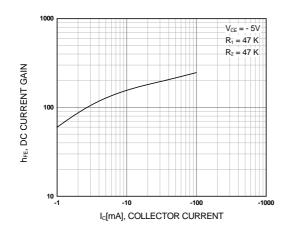


Figure 3. Input off Voltage

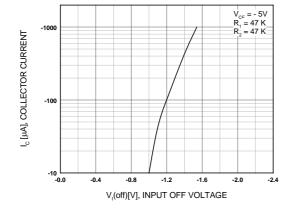


Figure 2. Input On Voltage

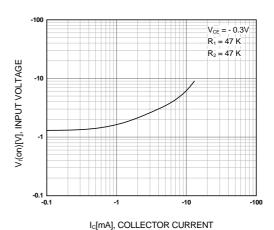
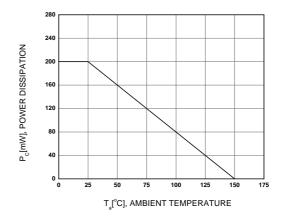
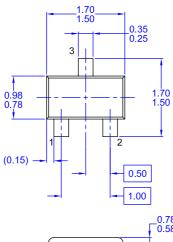


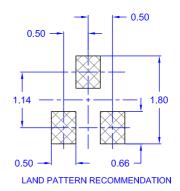
Figure 4. Power Derating

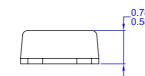


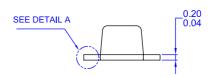
# **Package Dimensions**

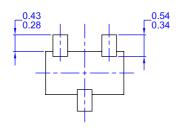
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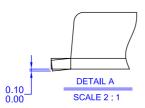












- NOTES: UNLESS OTHERWISE SPECIFIED A) THIS PACKAGE CONFORMS TO EIAJ SC89 PACKAGING STANDARD. B) ALL DIMENSIONS ARE IN MILLIMETERS.
  C) DIMENSIONS ARE EXCLUSIVE OF BURRS,
  MOLD FLASH, AND TIE BAR EXTRUSIONS.

Dimensions in Millimeters



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