

FJN3307R

Switching Application (Bias Resistor Built In) - Switching circuit, Inverter, Interface circuit, Driver Circuit

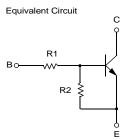
- Built in bias Resistor (R₁=22K Ω , R₂=47K Ω)
- Complement to FJN4307R



NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings Ta=25°C unless otherwise noted

| Symbol | Parameter | Value | Units | |
|------------------|-----------------------------|-----------|-------|--|
| V _{CBO} | Collector-Base Voltage | 50 | V | |
| V _{CEO} | Collector-Emitter Voltage | 50 | V | |
| V _{EBO} | Emitter-Base Voltage | 10 | V | |
| I _C | Collector Current | 100 | mA | |
| P _C | Collector Power Dissipation | 300 | mW | |
| T _J | Junction Temperature | 150 | °C | |
| T _{STG} | Storage Temperature | -55 ~ 150 | °C | |



Electrical Characteristics T_a=25°C unless otherwise noted

| Symbol | Parameter | Test Condition | Min. | Тур. | Max. | Units |
|--------------------------------|--------------------------------------|---|------|------|------|-------|
| BV _{CBO} | Collector-Base Breakdown Voltage | $I_{C}=10\mu A, I_{E}=0$ | 50 | | | V |
| BV _{CEO} | Collector-Emitter Breakdown Voltage | I _C =100μA, I _B =0 | 50 | | | V |
| I _{CBO} | Collector Cut-off Current | V_{CB} =40V, I_{E} =0 | | | 0.1 | μΑ |
| h _{FE} | DC Current Gain | V_{CE} =5V, I_{C} =5mA | 68 | | | |
| V _{CE} (sat) | Collector-Emitter Saturation Voltage | I _C =10mA, I _B =0.5mA | | | 0.3 | V |
| C _{ob} | Output Capacitance | V _{CB} =10V, I _E =0 f=1MHz | | 3.7 | | pF |
| f _T | Current Gain Bandwidth Product | V _{CE} =10V, I _C =5mA | | 250 | | MHz |
| V _I (off) | Input Off Voltage | $V_{CE}=5V, I_{C}=100\mu A$ | 0.4 | | | V |
| V _I (on) | Input On Voltage | V_{CE} =0.3V, I_{C} =2mA | | | 2.5 | V |
| R ₁ | Input Resistor | | 15 | 22 | 29 | ΚΩ |
| R ₁ /R ₂ | Resistor Ratio | | 0.42 | 0.47 | 0.52 | |

Typical Characteristics

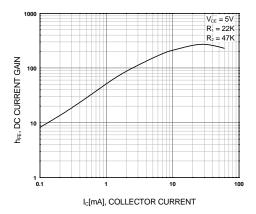


Figure 1. DC current Gain

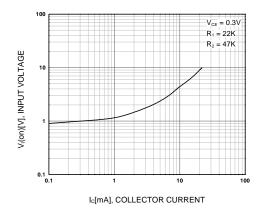


Figure 2. Input On Voltage

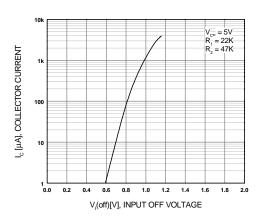


Figure 3. Input Off Voltage

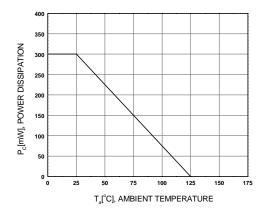
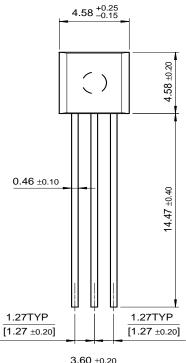
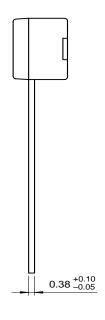
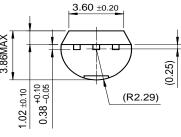


Figure 4. Power Derating

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