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January 2013

## **FJAFS1720**

# **ESBC<sup>™</sup> Rated NPN Power Transistor**

### **ESBC Features (FDS8817 MOSFET)**

V <sub>CS(ON)</sub>	I <sub>C</sub>	Equiv. R <sub>CS(ON)</sub>
0.304 V	10 A	$0.0304~\Omega^{~(1)}$

- · Low Equivalent On Resistance
- · Very Fast Switch: 150 kHz
- Squared RBSOA: Up to 1700 V
- Avalanche Rated
- · Low Driving Capacitance, No Miller Capacitance
- · Low Switching Losses
- Reliable HV Switch: No False Triggering due to High dv/dt Transients

### **Applications**

- High-Voltage and High-Speed Power Switches
- · Emitter-Switched Bipolar/MOSFET Cascode (ESBC<sup>™</sup>)
- · Smart Meters, Smart Breakers, SMPS, **HV Industrial Power Supplies**
- · Motor Drivers and Ignition Drivers

#### **Description**

The FJAFS1720 is a low-cost, high-performance power switch designed to provide the best performance when used in an ESBC<sup>™</sup> configuration in applications such as: power supplies, motor drivers, smart grid, or ignition switches. The power switch is designed to operate up to 1700 volts and up to 12 amps, while providing exceptionally low on-resistance and very low switching losses.

The ESBC<sup>™</sup> switch is designed to be driven using off-theshelf power supply controllers or drivers. The ESBCT MOSFET is a low-voltage, low-cost, surface-mount device that combines low-input capacitance and fast switching, The ESBC<sup>™</sup> configuration further minimizes the required driving power because it does not have Miller capacitance.

The FJAFS1720 provides exceptional reliability and a large operating range due to its square reverse-bias-safeoperating-area (RBSOA) and rugged design. The device is avalanche rated and has no parasitic transistors, so is not prone to static dv/dt failures.

The power switch is manufactured using a dedicated high-voltage bipolar process and is packaged in a highvoltage TO-3PF package.



Figure 1. Pin Configuration

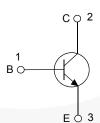


Figure 2. Internal Schematic Diagram

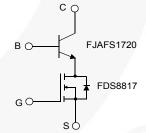


Figure 3. ESBC Configuration<sup>(2)</sup>

### **Ordering Information**

Part Number	Marking	Package	Packing Method
FJAFS1720TU	J1720	TO-3PF	TUBE

#### Notes:

- 1. Figure of Merit.
- 2. Other Fairchild MOSFETs can be used in this ESBC application.

### **Absolute Maximum Ratings**(3)

Values are at  $T_A = 25^{\circ}C$  unless otherwise noted.

Symbol	Parameter	Value	Units
V <sub>CBO</sub>	Collector-Base Voltage	1700	V
V <sub>CEO</sub>	Collector-Emitter Voltage	800	V
V <sub>EBO</sub>	Emitter-Base Voltage	6	V
I <sub>C</sub>	Collector Current (DC)	12	Α
P <sub>C</sub>	Collector Dissipation (T <sub>C</sub> = 25°C)	60	W
T <sub>J</sub>	Operating and Junction Temperature Range	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature Range	-55 to +150	°C

#### Note:

3. Pulse Test is Pulse Width  $\leq$  5 ms, Duty Cycle  $\leq$  10%.

#### **Thermal Characteristics**

Values are at  $T_A = 25$ °C unless otherwise noted.

Symbol	Parameter	Max.	Units
$R_{\theta iC}$	Thermal Resistance, Junction to Case	2.08	°C/W

#### Electrical Characteristics(4)

Values are at  $T_A = 25$ °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
I <sub>CES</sub>	Collector Cut-off Current	V <sub>CB</sub> = 1400 V, R <sub>BE</sub> = 0	1		100	μΑ
I <sub>CBO</sub>	Collector Cut-off Current	$V_{CB} = 800 \text{ V}, I_{E} = 0$			10	μΑ
I <sub>EBO</sub>	Emitter Cut-off Current	$V_{EB} = 4 \text{ V}, I_{C} = 0$			100	μΑ
BV <sub>CBO</sub>	Collector-Base Breakdown Voltage	$I_C = 500  \mu A, I_E = 0$	1700			V
BV <sub>CEO</sub>	Collector-Emitter Breakdown Voltage	$I_C = 5 \text{ mA}, I_B = 0$	800			V
BV <sub>EBO</sub>	Base-Emitter Breakdown Voltage	$I_E = 500  \mu A, I_C = 0$	6			٧
h <sub>FE1</sub>	DC Current Gain	V <sub>CE</sub> = 5 V, I <sub>C</sub> = 1 A	8.0			
h <sub>FE2</sub>	DC Current Gain	V <sub>CE</sub> = 5 V, I <sub>C</sub> = 11 A	5.5		8.5	
		$I_C = 10 \text{ A}, I_B = 3.33 \text{ A}, h_{FE} = 3$		0.25		V
V <sub>CE</sub> (sat)	Collector-Emitter Saturation Voltage	I <sub>C</sub> = 5 A, I <sub>B</sub> = 1.0 A, h <sub>FE</sub> = 5		0.20		V
		I <sub>C</sub> = 1 A, I <sub>B</sub> = 0.1 A, h <sub>FE</sub> = 10		0.20		V
V <sub>BE</sub> (sat)	Base-Emitter Saturation Voltage	I <sub>C</sub> = 10 A, I <sub>B</sub> = 3.33 A, h <sub>FE</sub> = 3		0.86	<i>y</i>	V

#### Note:

4. Pulse Test: Pulse Width 5 ms, Duty Cycle 10%.

### ESBC Configured Electrical Characteristics<sup>(5)</sup>

Values are at  $T_A = 25^{\circ}C$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
f <sub>T</sub>	Current Gain Bandwidth Product	$I_C = 0.1 \text{ A,V}_{CE} = 10 \text{ V}$		15		MHz
It <sub>f</sub>	Inductive Current Fall Time	$V_{GS} = 10 \text{ V}, R_{G} = 47 \Omega,$		60		ns
t <sub>s</sub>	Inductive Storage Time	V <sub>Clamp</sub> = 500 V,		1000		ns
Vt <sub>f</sub>	Inductive Voltage Fall Time	$I_C = 2 A$ , $I_B = 0.2 A$ , $h_{FE} = 10$		85		ns
Vt <sub>r</sub>	Inductive Voltage Rise Time	$L_C = 1 \text{ mH},$		125		ns
t <sub>c</sub>	Inductive Crossover Time	SRF = 350 kHz		165		ns
It <sub>f</sub>	Inductive Current Fall Time	$V_{GS} = 10 \text{ V}, R_{G} = 47 \Omega,$		24		ns
t <sub>s</sub>	Inductive Storage Time	V <sub>Clamp</sub> = 500 V,		1500		ns
Vt <sub>f</sub>	Inductive Voltage Fall Time	I <sub>C</sub> = 5 A, I <sub>B</sub> = 1 A, h <sub>FE</sub> = 5		85		ns
Vt <sub>r</sub>	Inductive Voltage Rise Time	L <sub>C</sub> = 1 mH,		65		ns
t <sub>c</sub>	Inductive Crossover Time	SRF = 350 kHz		110		ns
V <sub>CSW</sub>	Maximum Collector Source Voltage at Turn-off without Snubber	h <sub>FE</sub> = 5, I <sub>C</sub> = 6 A	1700			V
I <sub>GS(OS)</sub>	Gate-Source Leakage Cur- rent	$V_{GS} = \pm 20 \text{ V}$		1.0		nA
		$V_{GS}$ = 10 V, $I_{C}$ = 10 A, $I_{B}$ = 3.3 A, $h_{FE}$ = 3		0.3040		V
	Collector-Source On Voltage	$V_{GS} = 10 \text{ V}, I_C = 6 \text{ A}, I_B = 2 \text{ A}, h_{FE} = 3$		0.2124		V
V <sub>CS(ON)</sub>		$V_{GS} = 10 \text{ V}, I_C = 3 \text{ A}, I_B = 1 \text{ A}, h_{FE} = 3$		0.1362		V
		$V_{GS} = 10 \text{ V}, I_C = 3 \text{ A}, I_B = 0.6 \text{ A}, h_{FE} = 5$		0.1662		V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>BS</sub> = V <sub>GS,</sub> I <sub>B</sub> = 250 μA		1.9		V
C <sub>iss</sub>	Input Capacitance (V <sub>GS</sub> = V <sub>CB</sub> = 0)	V <sub>CS</sub> = 25 V, f = 1 MHz		1805		pF
Q <sub>GS(tot)</sub>	Gate-Source Charge V <sub>CB</sub> =0	$V_{GS}$ = 10 V, $I_{C}$ = 6 A, $V_{CS}$ = 25 V		6		nC
()	Static Drain-Source	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A		5.4		mΩ
		14 4014 L 45 A T 405 00		7.5		
r <sub>DS(ON)</sub>	On Resistance	$V_{GS}$ = 10 V, $I_{D}$ = 15 A, $T_{A}$ = 125 °C		7.5		mΩ

#### Note:

5. Used typical FDS8817 MOSFET specifications in table. Table could vary if other Fairchild MOSFETs are used.

### **Typical Performance Characteristics**

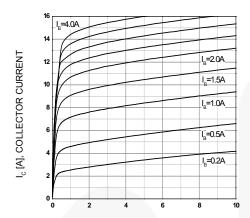


Figure 4. Static Characteristics

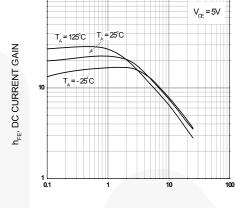


Figure 5. DC Current Gain

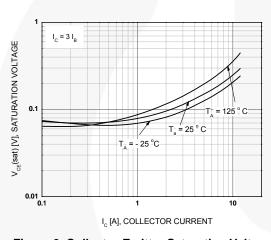


Figure 6. Collector-Emitter Saturation Voltage  $h_{\text{FE}}$ =3

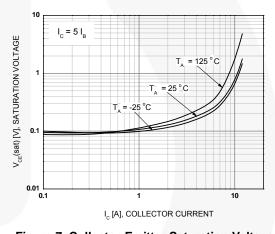


Figure 7. Collector-Emitter Saturation Voltage  $h_{\text{FE}}$ =5

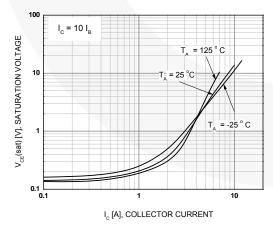


Figure 8. Collector-Emitter Saturation Voltage  $h_{\text{FE}}$ =10

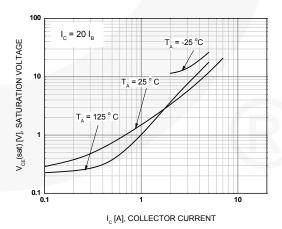


Figure 9. Collector-Emitter Saturation Voltage  $h_{\text{FE}}$ =20

### **Typical Performance Characteristics** (Continued)

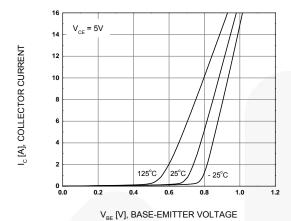


Figure 10. Base-Emitter On Voltage

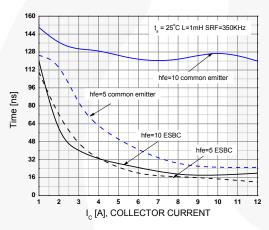


Figure 12. Inductive Load Collector Current Fall-time (t<sub>f</sub>)

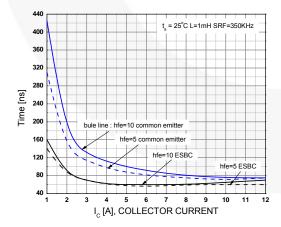


Figure 14. Inductive Load Collector Voltage Fall-time  $(t_f)$ 

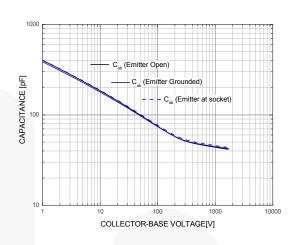


Figure 11. Capacitance

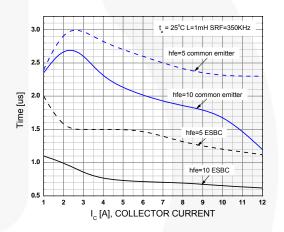


Figure 13. Inductive Load Collector Current Storage time  $(t_{stg})$ 

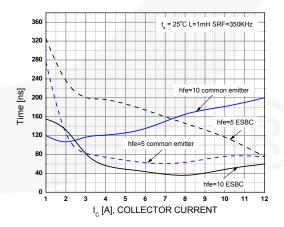


Figure 15. Inductive Load Collector Voltage Rise-time (t<sub>r</sub>)

### **Typical Performance Characteristics** (Continued)

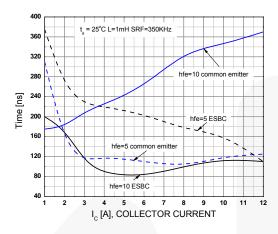


Figure 16. Inductive Load Collector Current / Voltage Crossover (t<sub>c</sub>)

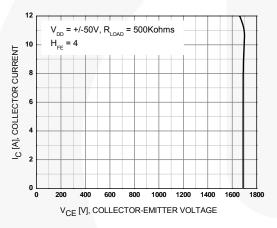


Figure 18. ESBC RBSOA

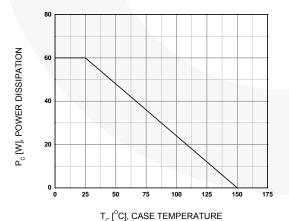


Figure 20. Power Derating

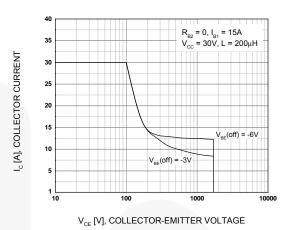


Figure 17. Reverse Bias Safe Operating Area

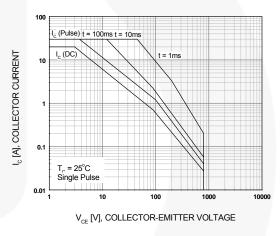


Figure 19. Forward Bias Safe Operating Area

### **Test Circuits**

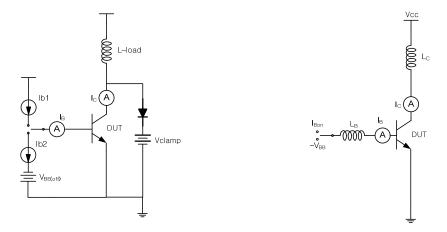


Figure 21. Test Circuit For Inductive Load and Reverse Bias Safe Operating

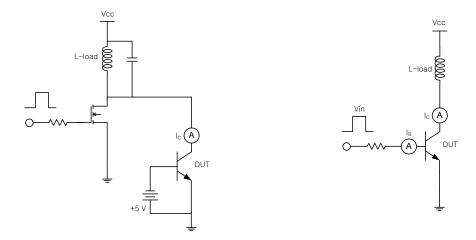


Figure 22. Energy Rating Test Circuit

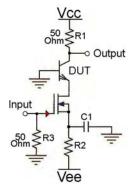


Figure 23. f<sub>T</sub> Measurement

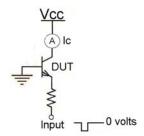


Figure 24. FBSOA

### Test Circuits (Continued)

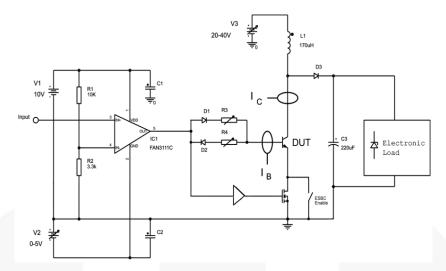


Figure 25. Simplified Saturated Switch Driver Circuit

#### **Functional Test Waveforms**

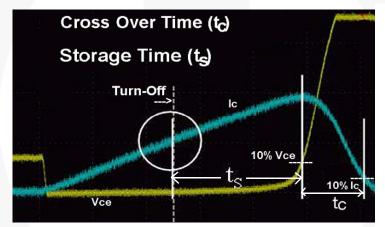


Figure 26. Crossover Time Measurement

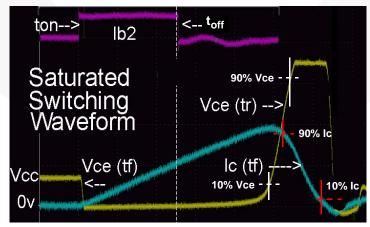


Figure 27. Saturated Switching Waveform

### Functional Test Waveforms (Continued)

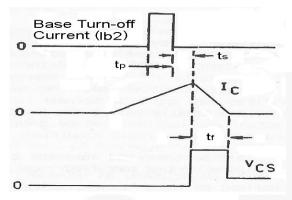


Figure 28. Storage Time - Common Emitter Base turn off (lb2) to I<sub>C</sub> Fall-Time

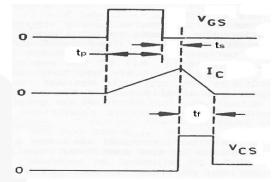
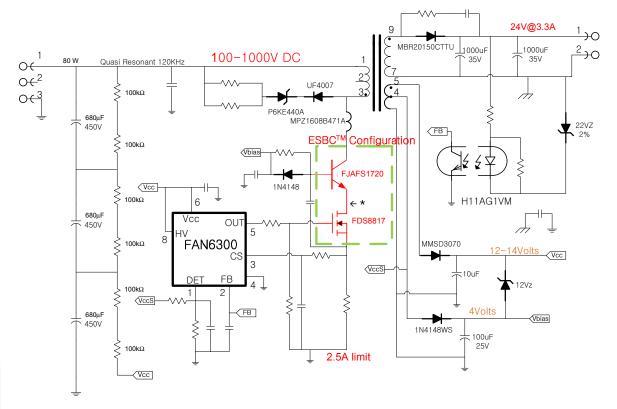


Figure 29. Storage Time - ESBC FET Gate (off) to I<sub>C</sub> Fall-Time

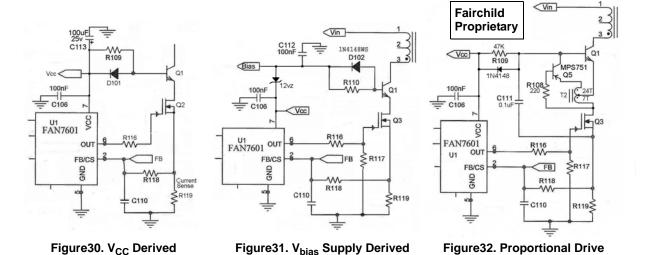
### **Very Wide Input Voltage Range Supply**

- 80 W; Secondary-Side Regulation: 3 Capacitor Input; Quasi Resonant



\* Make short as possible

### **Driving ESBC Switches**



### **Physical Dimensions**

### TO-3PF

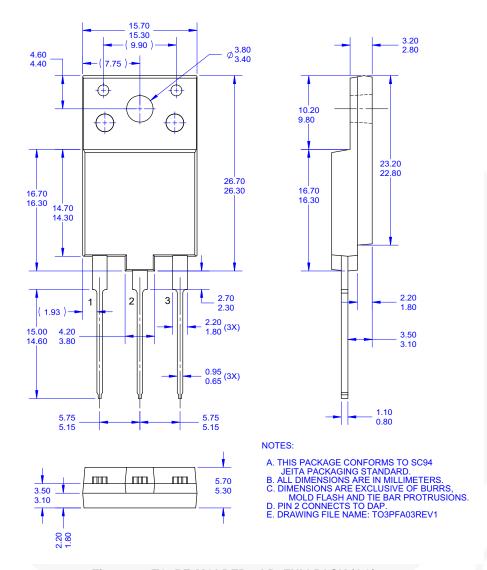


Figure 33. TO3PF, MOLDED, 3LD, FULLPACK (AG)

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