

FIN1019

3.3V LVDS High Speed Differential Driver/Receiver

General Description

This driver and receiver pair are designed for high speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. The driver translates LVTTTL signals to LVDS levels with a typical differential output swing of 350mV and the receiver translates LVDS signals, with a typical differential input threshold of 100mV, into LVTTTL levels. LVDS technology provides low EMI at ultra low power dissipation even at high frequencies. This device is ideal for high speed clock or data transfer.

Features

- Greater than 400Mbps data rate
- 3.3V power supply operation
- 0.5ns maximum differential pulse skew
- 2.5ns maximum propagation delay
- Low power dissipation
- Power-Off protection
- 100mV receiver input sensitivity
- Fail safe protection open-circuit, shorted and terminated conditions
- Meets or exceeds the TIA/EIA-644 LVDS standard
- Flow-through pinout simplifies PCB layout
- 14-Lead SOIC and TSSOP packages save space

Ordering Code:

Order Number	Package Number	Package Description
FIN1019M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
FIN1019MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

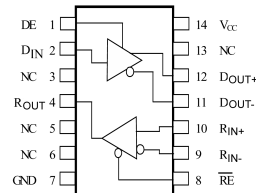
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Function Table

Inputs			Outputs	
R _{IN+}	R _{IN-}	\overline{RE}	R _{OUT}	
L	H	L	L	
H	L	L	H	
X	X	H	Z	
Fail Safe Condition			L	H
D _{IN}		DE	D _{OUT+}	D _{OUT-}
L		H	L	H
H		H	H	L
X		L	Z	Z
Open-Circuit or Z		H	L	H

H = HIGH Logic Level L = LOW Logic Level X = Don't Care
Z = High Impedance Fail Safe = Open, Shorted, Terminated

Connection Diagram



Pin Descriptions

Pin Name	Description
D _{IN}	LVTTTL Data Input
D _{OUT+}	Non-inverting LVDS Output
D _{OUT-}	Inverting LVDS Output
DE	Driver Enable (LVTTTL, Active HIGH)
R _{IN+}	Non-Inverting LVDS Input
R _{IN-}	Inverting LVDS Input
R _{OUT}	LVTTTL Receiver Output
\overline{RE}	Receiver Enable (LVTTTL, Active LOW)
V _{CC}	Power Supply
GND	Ground
NC	No Connect

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	-0.5V to +4.6V
LVTTTL DC Input Voltage (D_{IN} , DE , \overline{RE})	-0.5V to +6V
LVDS DC Input Voltage (R_{IN+} , R_{IN-})	-0.5V to 4.7V
LVTTTL DC Output Voltage (R_{OUT})	-0.5V to +6V
LVDS DC Output Voltage (D_{OUT+} , D_{OUT-})	-0.5V to 4.7V
LVDS Driver Short Circuit Current (I_{OSD})	Continuous
LVTTTL DC Output Current (I_O)	16 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C
Max Junction Temperature (T_J)	150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C
ESD (Human Body Model)	≥ 6500V
ESD (Machine Model)	≥ 300V

Recommended Operating Conditions

Supply Voltage (V_{CC})	3.0V to 3.6V
Input Voltage (V_{IN})	0 to V_{CC}
Magnitude of Differential Voltage ($ V_{ID} $)	100 mV to V_{CC}
Common-Mode Input Voltage (V_{IC})	0.05V to 2.35V
Operating Temperature (T_A)	-40°C to +85°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specification.

DC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ (Note 2)	Max	Units
LVDS Differential Driver Characteristics						
V_{OD}	Output Differential Voltage	$R_L = 100\Omega$, See Figure 1	250	350	450	mV
ΔV_{OD}	V_{OD} Magnitude Change from Differential LOW-to-HIGH				25	mV
V_{OS}	Offset Voltage		1.125	1.25	1.375	V
ΔV_{OS}	Offset Magnitude Change from Differential LOW-to-HIGH				25	mV
I_{OZD}	Disabled Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $DE = 0V$			±20	μA
I_{OFF}	Power Off Output Current	$V_{CC} = 0V$, $V_{OUT} = 0V$ or 3.6V			±20	μA
I_{OS}	Short Circuit Output Current	$V_{OUT} = 0V$, $DE = V_{CC}$			-8	mA
		$V_{OD} = 0V$, $DE = V_{CC}$			±8	
LVTTTL Driver Characteristics						
V_{OH}	Output HIGH Voltage	$I_{OH} = -100\mu A$, $\overline{RE} = 0V$, See Figure 6 and Table 1	$V_{CC} - 0.2$			V
		$I_{OH} = -8mA$, $\overline{RE} = 0V$, $V_{ID} = 400mV$, $V_{ID} = 400mV$, $V_{IC} = 1.2V$, see Figure 6	2.4			
V_{OL}	Output LOW Voltage	$I_{OL} = 100\mu A$, $\overline{RE} = 0V$, $V_{ID} = -400mV$, See Figure 6 and Table 1			0.2	V
		$I_{OL} = -8mA$, $\overline{RE} = 0V$, $V_{ID} = -400mV$, $V_{ID} = -400mV$, $V_{IC} = 1.2V$, see Figure 6			0.5	
I_{OZ}	Disabled Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{RE} = V_{CC}$			±20	μA
LVDS Receiver Characteristics						
V_{TH}	Differential Input Threshold HIGH	See Figure 6 and Table 1			100	mV
V_{TL}	Differential Input Threshold LOW	See Figure 6 and Table 1	-100			mV
I_{IN}	Input Current	$V_{IN} = 0V$ or V_{CC}			±20	μA
$I_{I(OFF)}$	Power-OFF Input Current	$V_{CC} = 0V$, $V_{IN} = 0V$ or 3.6V			±20	μA
LVTTTL Driver and Control Signals Characteristics						
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage		GND		0.8	V
I_{IN}	Input Current	$V_{IN} = 0V$ or V_{CC}			±20	μA
$I_{I(OFF)}$	Power-OFF Input Current	$V_{CC} = 0V$, $V_{IN} = 0V$ or 3.6V			±20	μA
V_{IK}	Input Clamp Voltage	$I_{IK} = -18mA$	-1.5			V

DC Electrical Characteristics (Continued)						
Device Characteristics						
I _{CC}	Power Supply Current	Driver Enabled, Driver Load: R _L = 100 Ω Receiver Disabled, No Receiver Load			12.5	mA
		Driver Enabled, Driver Load: R _L = 100 Ω, Receiver Enabled, (R _{IN+} = 1V and R _{IN-} = 1.4V) or (R _{IN+} = 1.4V and R _{OUT-} = 1V)			12.5	mA
		Driver Disabled, Receiver Enabled, (R _{IN+} = 1V and R _{IN-} = 1.4V) or (R _{IN+} = 1.4V and R _{IN-} = 1V)			7.0	mA
		Driver Disabled, Receiver Disabled			7.0	mA
C _{IN}	Input Capacitance	Any LVTTTL or LVDS Input		4		pF
C _{OUT}	Output Capacitance	Any LVTTTL or LVDS Output		6		pF
Note 2: All typical values are at T _A = 25°C and with V _{CC} = 3.3V.						
AC Electrical Characteristics						
Over supply voltage and operating temperature ranges, unless otherwise specified						
Symbol	Parameter	Test Conditions	Min	Typ (Note 3)	Max	Units
Driver Timing Characteristics						
t _{PLHD}	Differential Propagation Delay LOW-to-HIGH	R _L = 100 Ω, C _L = 10 pF, See Figure 2 and Figure 3	0.5		1.5	ns
t _{PHLD}	Differential Propagation Delay HIGH-to-LOW		0.5		1.5	ns
t _{TLHD}	Differential Output Rise Time (20% to 80%)		0.4		1.0	ns
t _{THLD}	Differential Output Fall Time (80% to 20%)		0.4		1.0	ns
t _{SK(P)}	Pulse Skew t _{PLH} - t _{PHL}				0.5	ns
t _{SK(PP)}	Part-to-Part Skew (Note 4)	R _L = 100Ω, C _L = 10 pF, See Figure 4 and Figure 5			1.0	ns
t _{ZHD}	Differential Output Enable Time from Z to HIGH				5.0	ns
t _{ZLD}	Differential Output Enable Time from Z to LOW				5.0	ns
t _{HZD}	Differential Output Disable Time from HIGH to Z				5.0	ns
t _{LZD}	Differential Output Disable Time from LOW to Z				5.0	ns
Receiver Timing Characteristics						
t _{PLH}	Propagation Delay LOW-to-HIGH	V _{ID} = 400 mV, C _L = 10 pF, See Figure 6 and Figure 7	0.9		2.5	ns
t _{PHL}	Propagation Delay HIGH-to-LOW		0.9		2.5	ns
t _{TLH}	Output Rise time (20% to 80%)		0.5			ns
t _{THL}	Output Fall time (80% to 20%)		0.5			ns
t _{SK(P)}	Pulse Skew t _{PLH} - t _{PHL}				0.5	ns
t _{SK(PP)}	Part-to-Part Skew (Note 4)	R _L = 500 Ω, C _L = 10 pF, See Figure 8			1.0	ns
t _{ZH}	LVTTTL Output Enable Time from Z to HIGH				5.0	ns
t _{ZL}	LVTTTL Output Enable Time from Z to LOW				5.0	ns
t _{HZ}	LVTTTL Output Disable Time from HIGH to Z				5.0	ns
t _{LZ}	LVTTTL Output Disable Time from LOW to Z				5.0	ns
Note 3: All typical values are at T _A = 25°C and with V _{CC} = 5V.						
Note 4: t _{SK(PP)} is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.						

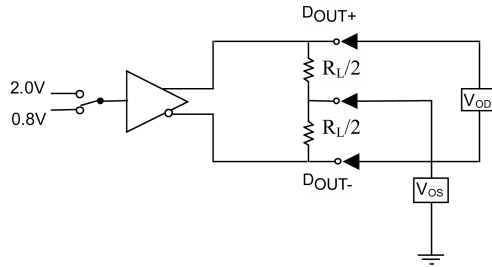
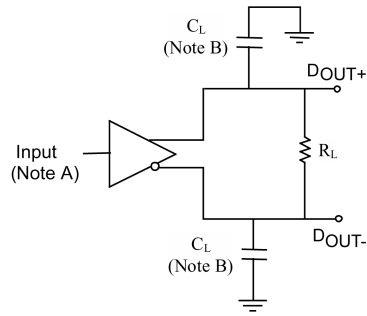


FIGURE 1. Differential Driver DC Test Circuit



Note A: Input pulses have frequency = 10 MHz, t_R or $t_F = 2$ ns

Note B: C_L includes all probe and fixture capacitances

FIGURE 2. Differential Driver Propagation Delay and Transition Time Test Circuit

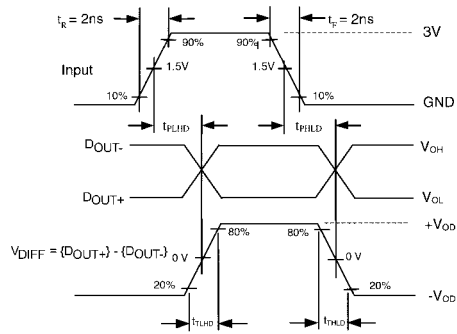
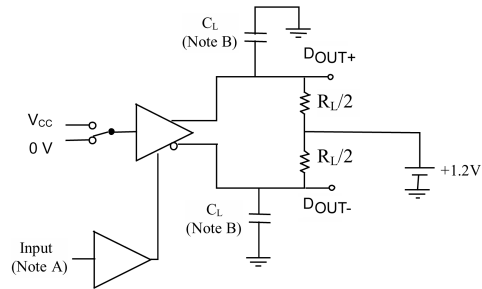


FIGURE 3. AC Waveforms for Differential Driver



Note B: Input pulses have the frequency = 10 MHz, t_R or $t_F = 2$ ns

Note A: C_L includes all probe and fixture capacitances

FIGURE 4. Differential Driver Enable and Disable Test Circuit

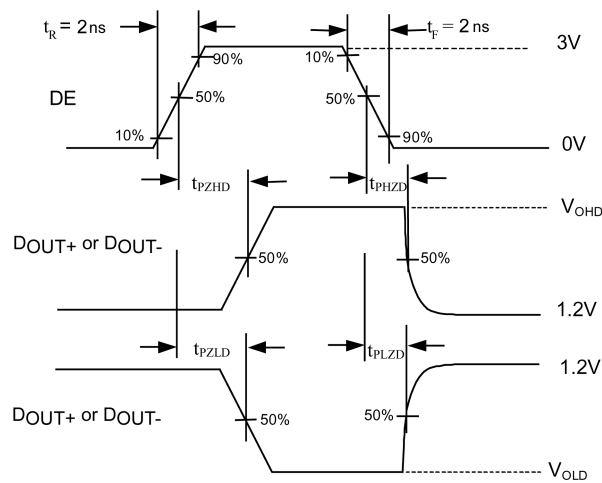
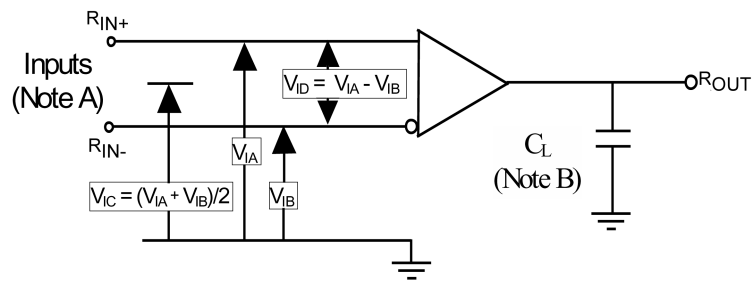


FIGURE 5. Enable and Disable AC Waveforms



Note A: Input pulses have frequency = 10 MHz, t_R or t_F = 1 ns

Note B: C_L includes all probe and fixture capacitance

FIGURE 6. Differential Receiver Voltage Definitions and Propagation Delay and Transition Time Test Circuit

TABLE 1. Receiver Minimum and Maximum Input Threshold Test Voltages

Applied Voltages (V)		Resulting Differential Input Voltage (mV)	Resulting Common Mode Input Voltage (V)	
V_{IA}	V_{IB}		V_{ID}	V_{IC}
1.25	1.15	100	1.2	
1.15	1.25	-100	1.2	
2.4	2.3	100	2.35	
2.3	2.4	-100	2.35	
0.1	0	100	0.05	
0	0.1	-100	0.05	
1.5	0.9	600	1.2	
0.9	1.5	-600	1.2	
2.4	1.8	600	2.1	
1.8	2.4	-600	2.1	
0.6	0	600	0.3	
0	0.6	-600	0.3	

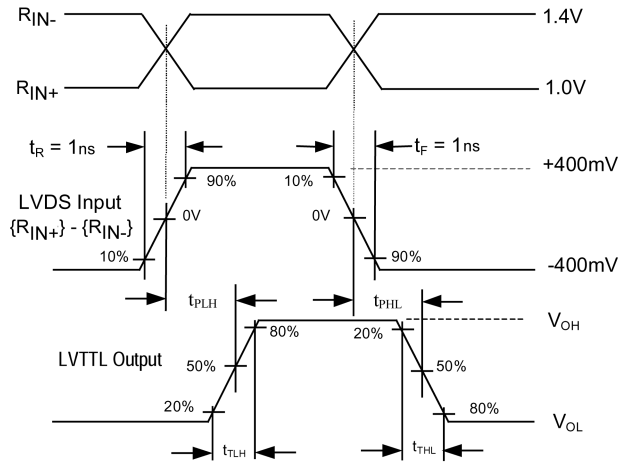
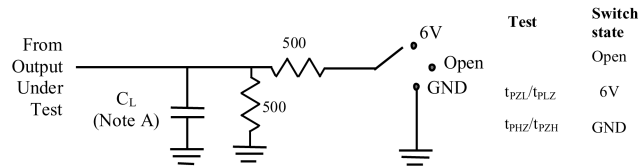


FIGURE 7. LVDS Input to LVTTTL Output AC Waveforms

Test Circuit for LVTTTL Outputs



Voltage Waveforms Enable and Disable Times

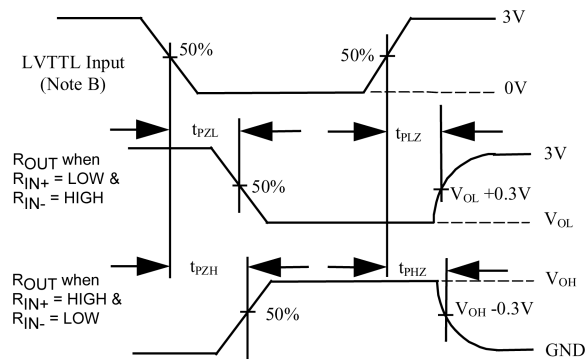


FIGURE 8. LVTTTL Outputs Test Circuit and AC Waveforms

DC / AC Typical Performance Curves

Drivers

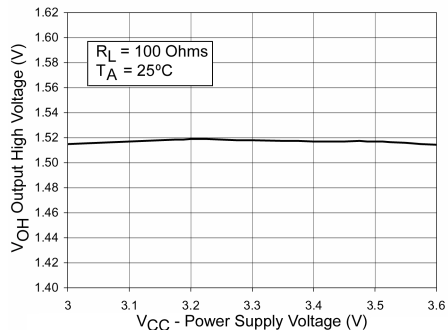


FIGURE 9. Output High Voltage vs. Power Supply Voltage

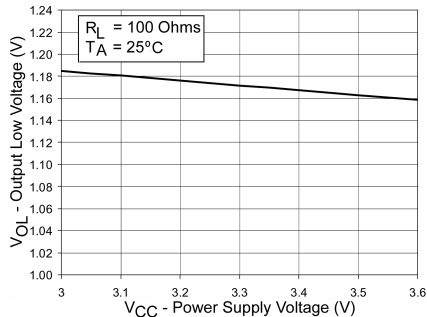


FIGURE 10. Output Low Voltage vs. Power Supply Voltage

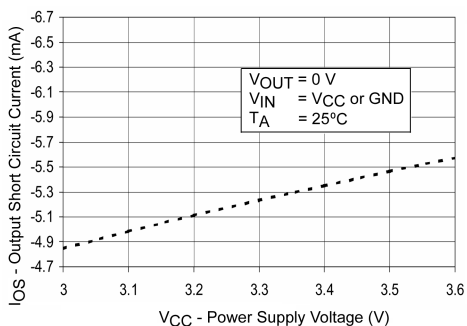


FIGURE 11. Output Short Circuit Current vs. Power Supply Voltage

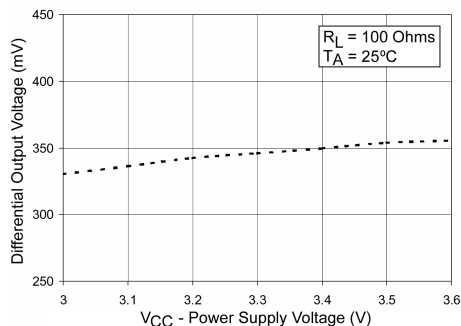


FIGURE 12. Differential Output Voltage vs. Power Supply Voltage

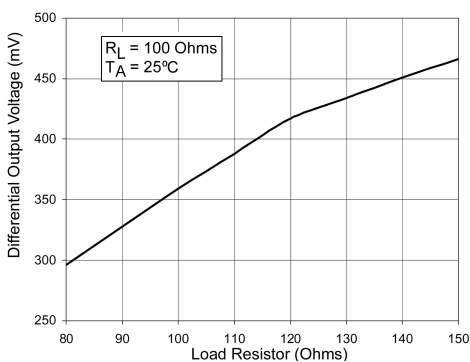


FIGURE 13. Differential Output Voltage vs. Load Resistor

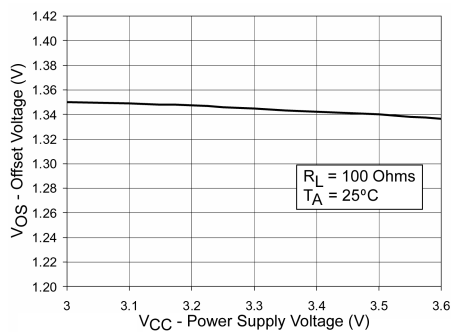


FIGURE 14. Offset Voltage vs. Power Supply Voltage

DC / AC Typical Performance Curves (Continued)

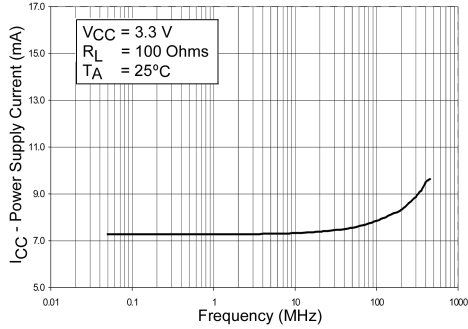


FIGURE 15. Power Supply Current vs. Frequency

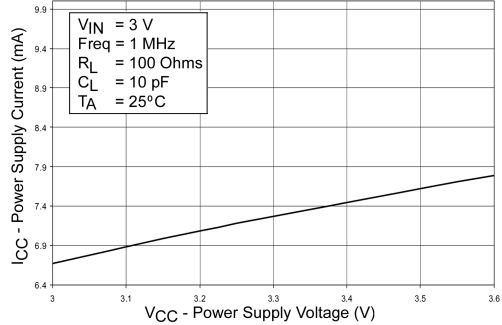


FIGURE 16. Power Supply Current vs. Power Supply Voltage

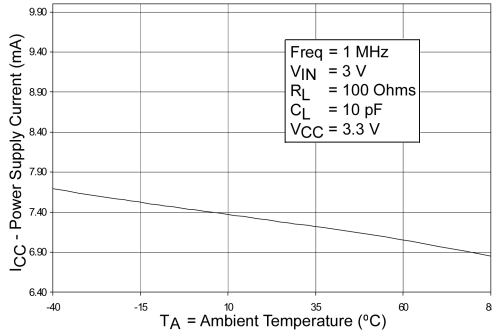


FIGURE 17. Power Supply Current vs. Ambient Temperature

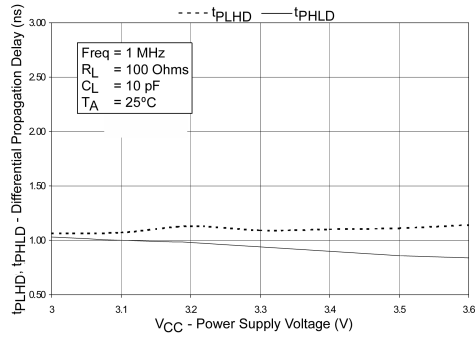


FIGURE 18. Differential Propagation Delay vs. Power Supply

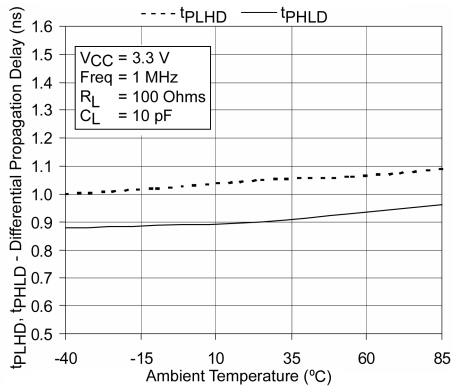


FIGURE 19. Differential Propagation Delay vs. Ambient Temperature

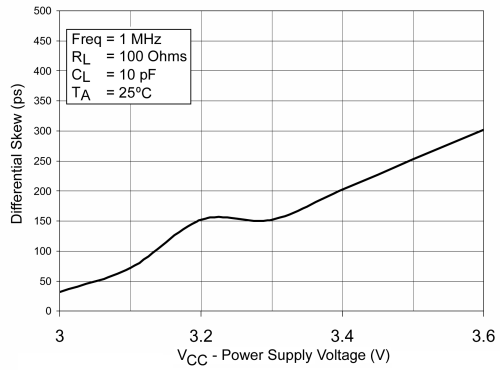


FIGURE 20. Differential Skew ($t_{PLH} - t_{PHL}$) vs. Power Supply Voltage

DC / AC Typical Performance Curves (Continued)

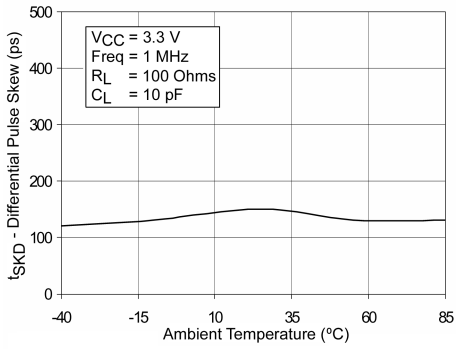


FIGURE 21. Differential Pulse Skew ($t_{pLH} - t_{pHL}$) vs. Ambient Temperature

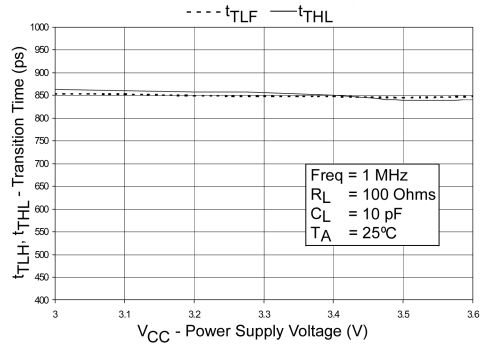


FIGURE 22. Transition Time vs. Power Supply Voltage

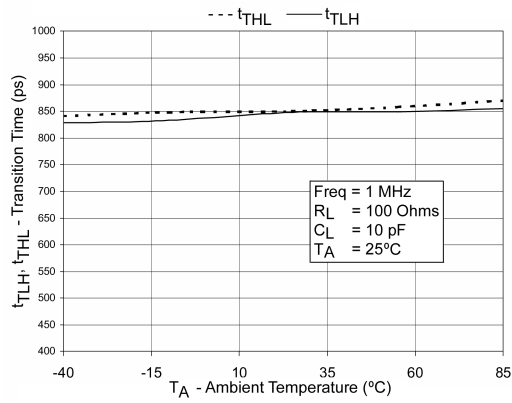


FIGURE 23. Transition Times vs. Ambient Temperature

DC / AC Typical Performance Curves

Receiver

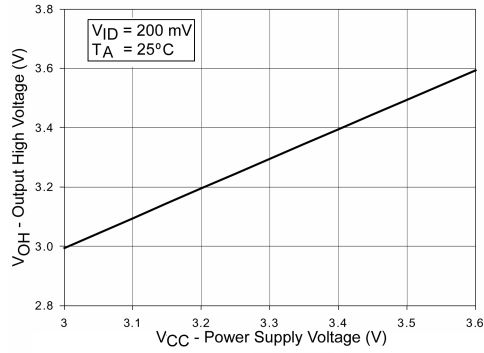


FIGURE 24. Output High Voltage vs. Power Supply Voltage

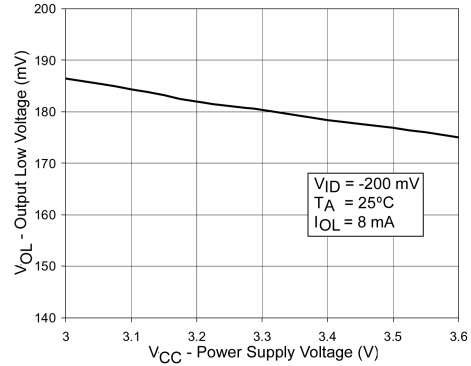


FIGURE 25. Output Low Voltage vs. Power Supply Voltage

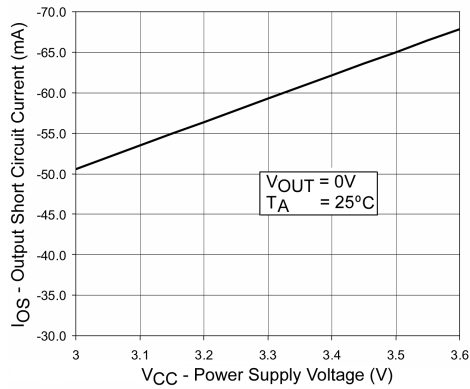


FIGURE 26. Output Short Circuit Current vs. Power Supply Voltage

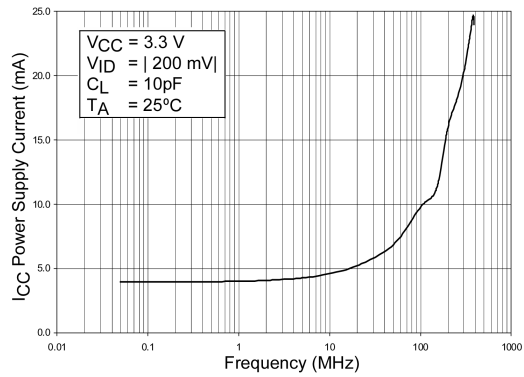


FIGURE 27. Power Supply Current vs. Frequency

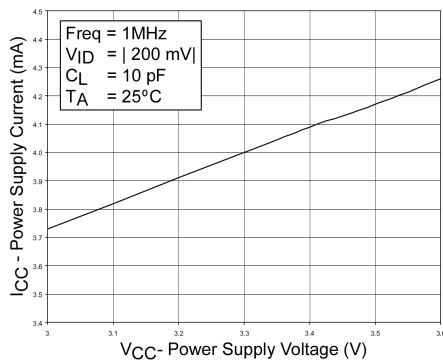


FIGURE 28. Power Supply Current vs. Power Supply Voltage

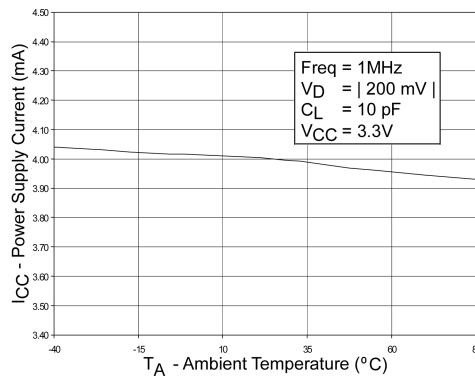


FIGURE 29. Power Supply Current vs. Ambient Temperature

DC / AC Typical Performance Curves (Continued)

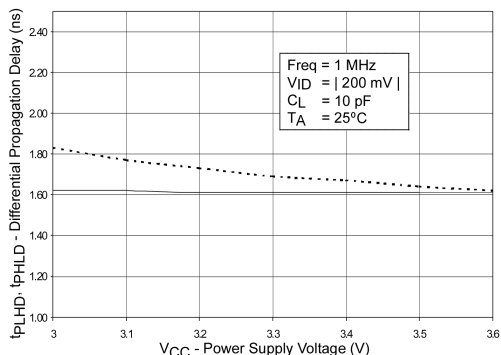


FIGURE 30. Differential Propagation Delay vs. Power Supply Voltage

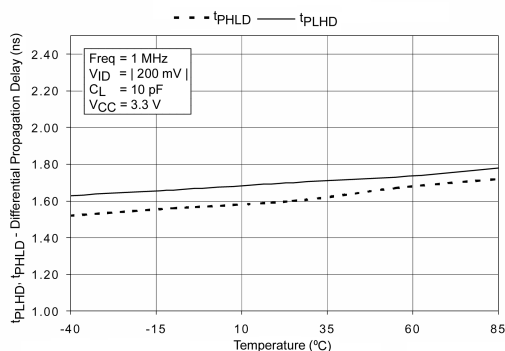


FIGURE 31. Differential Propagation Delay vs. Ambient Temperature

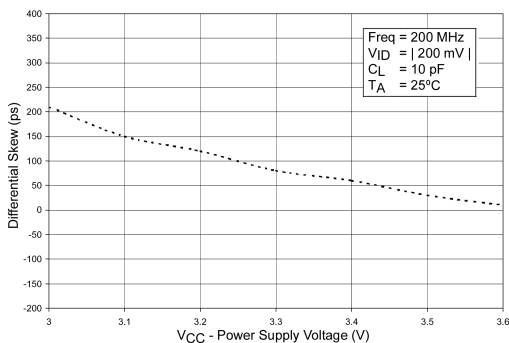


FIGURE 32. Differential Skew ($t_{PHL} - t_{PLH}$) vs. Power Supply Voltage

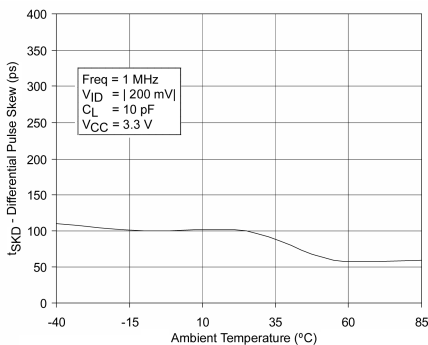


FIGURE 33. Differential Skew ($t_{PLH} - t_{PHL}$) vs. Ambient Temperature

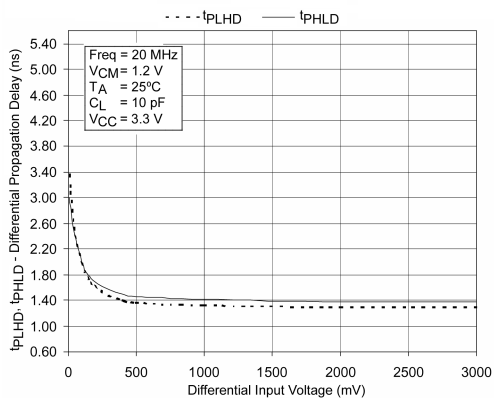


FIGURE 34. Differential Propagation Delay vs. Differential Input Voltage

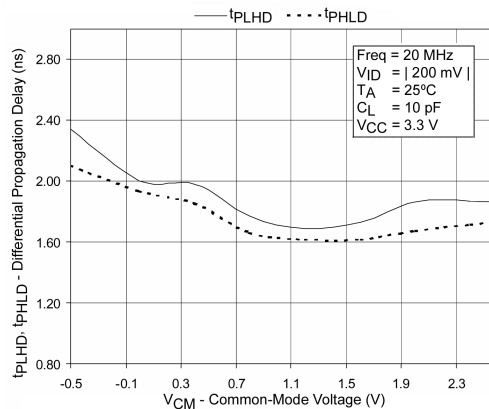


FIGURE 35. Differential Propagation Delay vs. Common-Mode Voltage

DC / AC Typical Performance Curves (Continued)

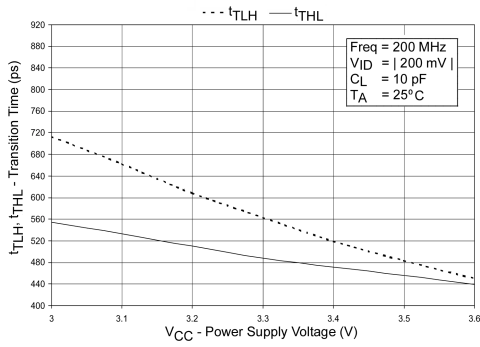


FIGURE 36. Transition Time vs. Power Supply Voltage

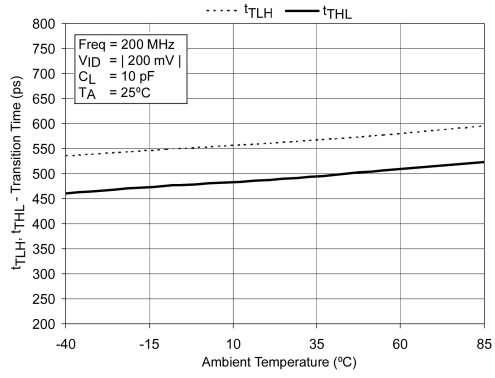


FIGURE 37. Transition Time vs. Ambient Temperature

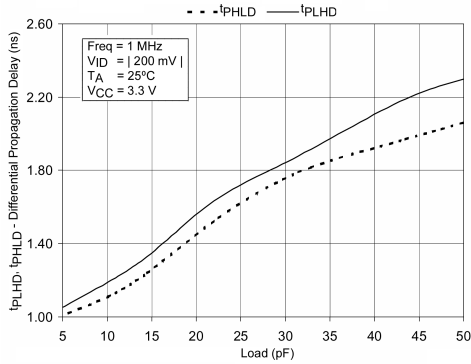


FIGURE 38. Differential Propagation Delay vs. Load

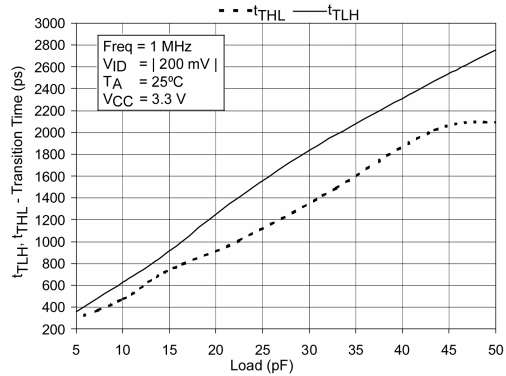


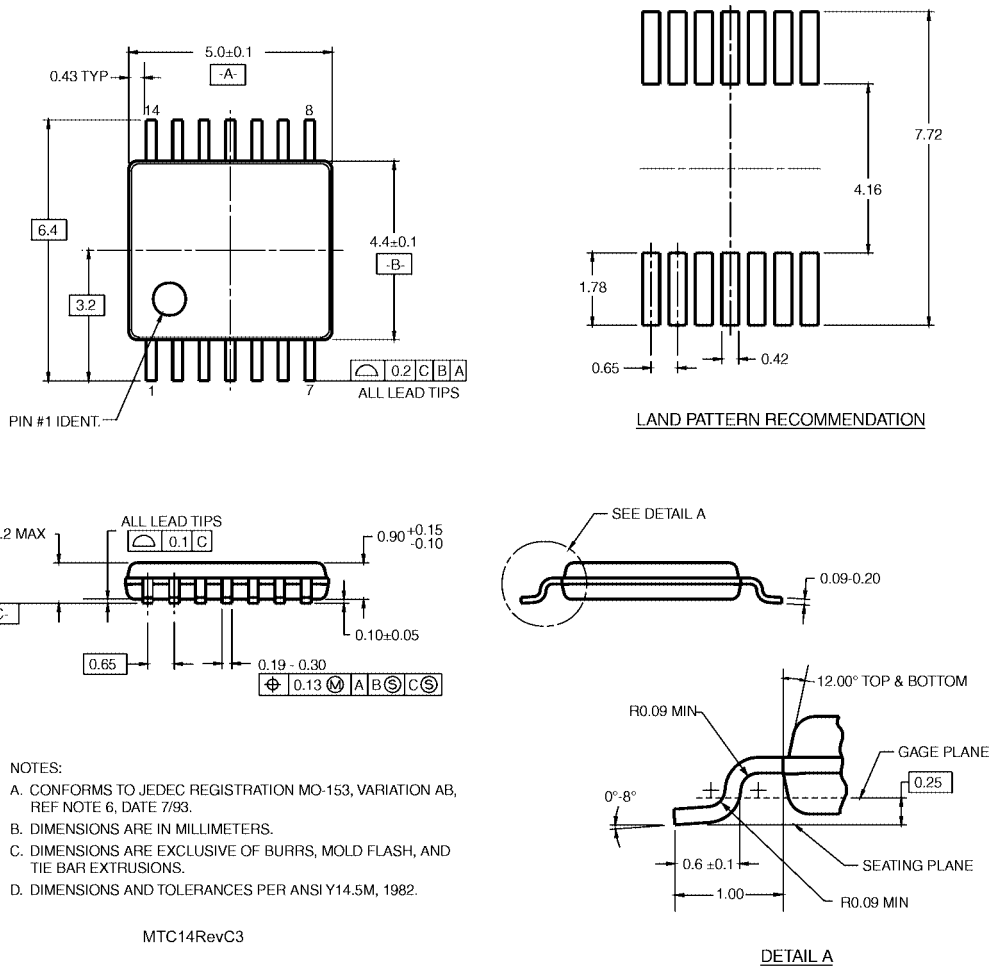
FIGURE 39. Transition Time vs. Load

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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