April 2009

FIN1017
3.3V LVDS, 1-Bit, High-Speed Differential Driver

Features

- Greater than 600Mbs Data Rate
- 3.3V Power Supply Operation
- 0.5ns Maximum Differential Pulse Skew
- 1.5ns Maximum Propagation Delay
- Low Power Dissipation
- Power-Off Protection
- Meets or Exceeds the TIA/EIA-644 LVDS Standard
- Flow-Through Pinout Simplifies PCB Layout
- 8-Lead SOIC and US8 Packages Save Space

Description

This single driver is designed for high-speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. The driver translates LVTTL signal levels to LVDS levels with a typical differential output swing of 350mV, which provides low EMI at ultra-low power dissipation even at high frequencies. This device is ideal for high-speed transfer of clock or data.

The FIN1017 can be paired with its companion receiver, the FIN1018, or with any other LVDS receiver.

Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	Packing Method
FIN1017MX	-40 to +85°C	Green	8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150inch Narrow	Tape and Reel
FIN1017K8X	-40 to +85°C	Green	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	Tape and Reel

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Pin Configuration

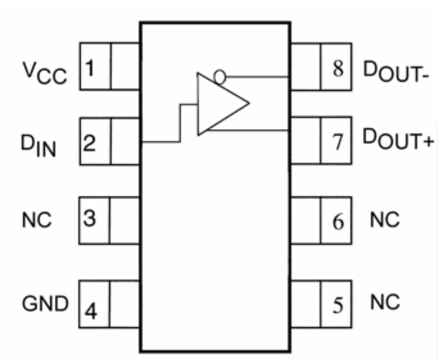

Figure 1. SOIC

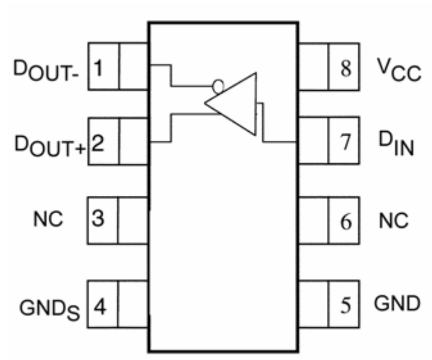

Figure 2. US-8 (Top View)[1]

Note:
1. Ground pins 4 and 5 for optimum performance.

Pin Definitions

Pin# US-8	Pin# SOIC	Name	Description
7	2	D_{IN}	LVTTL Data Input
2	7	D_{OUT+}	Non-inverting Driver Output
1	8	D_{OUT-}	Inverting Driver Output
8	1	V_{CC}	Power Supply
4, 5	4	GND / GND_S	Ground
3, 6	3, 5, 6	NC	No Connect

Function Table

Input	Outputs	
D_{IN}	D_{OUT+}	D_{OUT-}
LOW Logic Level	LOW Logic Level	HIGH Logic Level
HIGH Logic Level	HIGH Logic Level	LOW Logic Level
OPEN	LOW Logic Level	HIGH Logic Level

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	-0.5	+4.6	V
D_{IN}	DC Input Voltage	-0.5	+6.0	V
D_{OUT}	DC Output Voltage	-0.5	+4.7	V
I_{OSD}	Driver Short-Circuit Current	Continuous		A
T_{STG}	Storage Temperature Range	-65	+150	°C
T_J	Max Junction Temperature		+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)		+260	°C
ESD	Human Body Model, JESD22-A114		≥ 6500	V
	Bus Pins D_{OUT+}/D_{OUT-} to GND		≥ 10500	
	Machine Model, JESD22-A115		≥ 350	

XXX NOTE to Engineering – ESD values here do NOT match what's on WWW (pulled from PeopleSoft). XXX

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.6	V
V_{IN}	Input Voltage	0	V_{CC}	V
T_A	Operating Temperature	-40	+85	°C

DC Electrical Characteristics

Over-supply voltage and operating temperature ranges, unless otherwise specified. All typical values are at T_A = 25°C and with V_{CC} = 3.3V.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OD}	Output Differential Voltage	R_L = 100 Ω, See Figure 3	250	350	450	mV
ΔV_{OD}	V_{OD} Magnitude Change from Differential LOW-to-HIGH				25	mV
V_{OS}	Offset Voltage		1.125	1.250	1.375	V
ΔV_{OS}	Offset Magnitude Change from Differential LOW-to-HIGH				25	mV
I_{OFF}	Power-Off Output Current	V_{CC} = 0V, V_{OUT} = 0V or 3.6V			±20	mA
I_{OS}	Short-Circuit Output Current	V_{OUT} = 0V			-8	mA
		V_{OD} = 0V			±8	
V_{IH}	Input HIGH Voltage		2		V_{CC}	V
V_{IL}	Input LOW Voltage		GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0V or V_{CC}			±20	mA
$I_{I(OFF)}$	Power-Off Input Current	V_{CC} = 0V, V_{IN} = 0V or 3.6V			±20	mA
V_{IK}	Input Clamp Voltage	I_{IK} = -18mA	-1.5			V
I_{CC}	Power Supply Current	No Load, V_{IN} = 0V or V_{CC}			8	mA
		R_L = 100Ω, V_{IN} = 0V or V_{CC}			10	mA
C_{IN}	Input Capacitance			4		pF
C_{OUT}	Output Capacitance			6		pF

AC Electrical Characteristics

Over-supply voltage and operating temperature ranges, unless otherwise specified. All typical values are at T_A = 25°C and with V_{CC} = 3.3V. XXX there ARE no Typical values! XXX

Symbol	Parameter	Test Conditions	Min.	Max.	Units
t_{PLHD}	Differential Propagation Delay, LOW-to-HIGH	R_L = 100Ω, C_L = 10pF, see Figure 4 and Figure 5	0.5	1.5	ns
t_{PHLD}	Differential Propagation Delay, HIGH-to-LOW		0.5	1.5	ns
t_{TLHD}	Differential Output Rise Time (20% to 80%)		0.4	1.0	ns
t_{THLD}	Differential Output Fall Time (80% to 20%)		0.4	1.0	ns
$t_{SK(P)}$	Pulse Skew $\|t_{PLH} - t_{PHL}\|$			0.5	ns
$t_{SK(PP)}$	Part-to-Part Skew[2]			1.0	ns

Note:

2. $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.

Test Diagrams

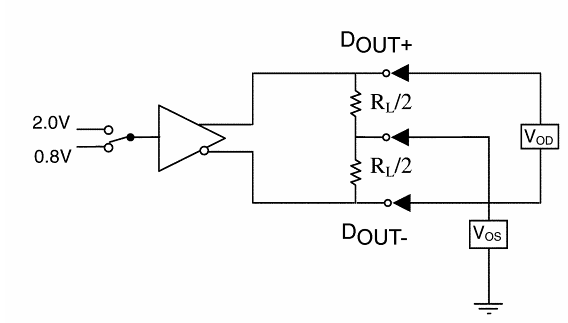

Figure 3. Differential Driver DC Test Circuit

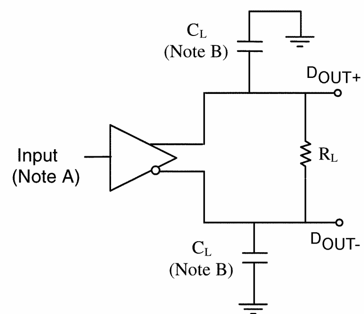

Figure 4. Differential Driver Propagation Delay and Transition Time Test Circuit

Notes:

Note A: All input pulses have frequency = 10MHz, t_R or t_F = 2ns.

Note B: C_L includes all probe and fixture capacitances.

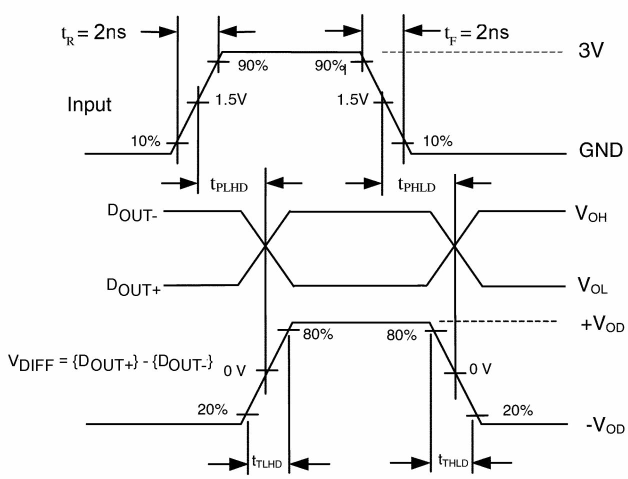

Figure 5. AC Waveforms

Typical Performance Characteristics

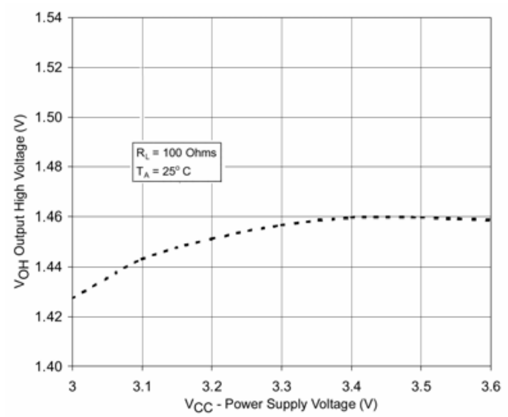

Figure 6. Output High Voltage vs. Power Supply Voltage

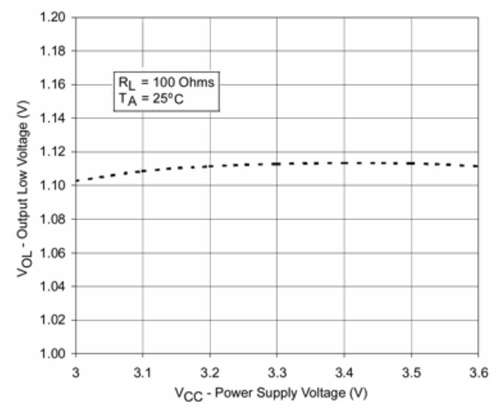

Figure 7. Output Low Voltage vs. Power Supply Voltage

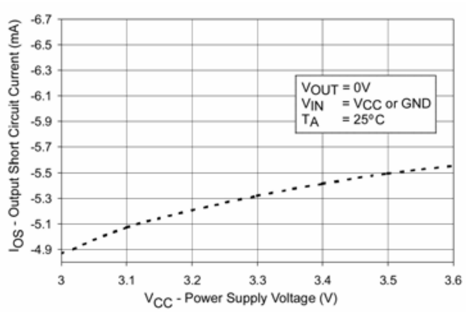

Figure 8. Output Short Circuit Current vs. Power Supply Voltage

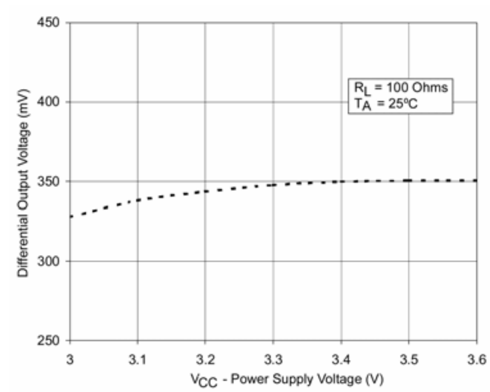

Figure 9. Differential Output Voltage vs. Power Supply Voltage

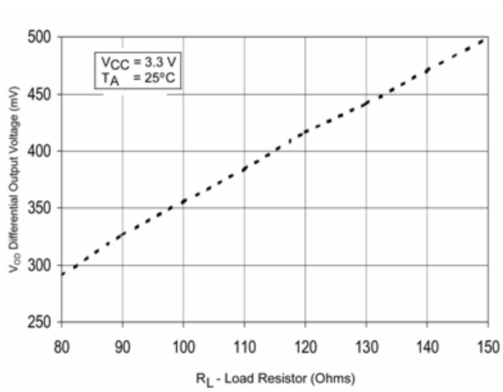

Figure 10. Differential Output Voltage vs. Load Resistor

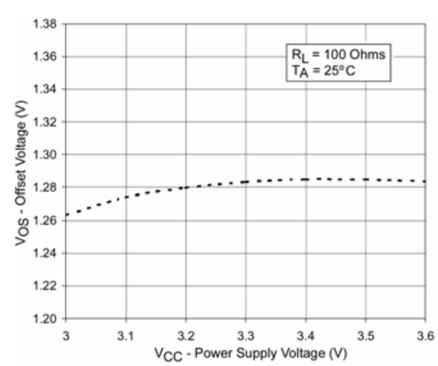

Figure 11. Offset Voltage vs. Power Supply Voltage

Typical Performance Characteristics

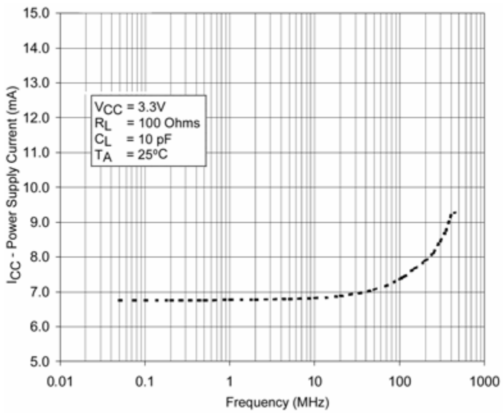

Figure 12.Power Supply Current vs. Frequency

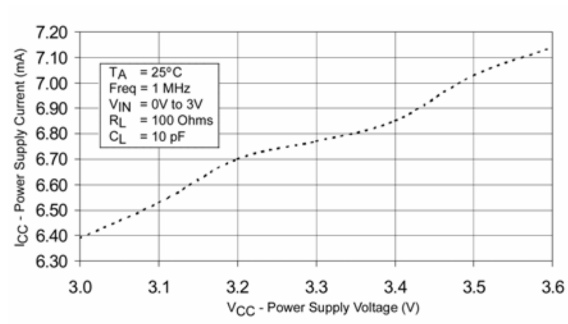

Figure 13.Power Supply Current vs. Power Supply Voltage

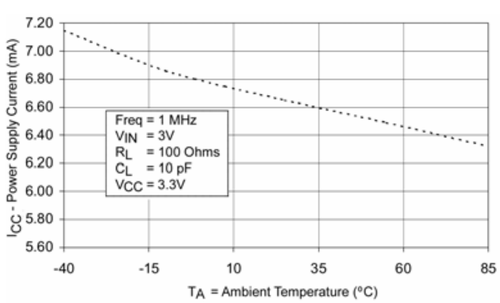

Figure 14.Power Supply Current vs. Ambient Temperature

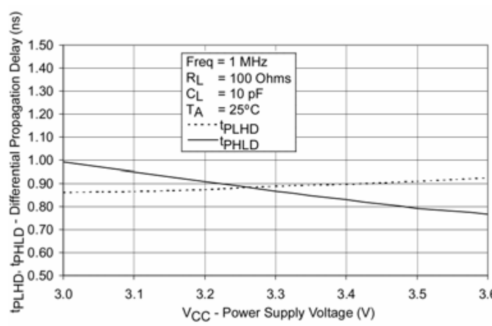

Figure 15.Differential Propagation Delay vs. Power Supply

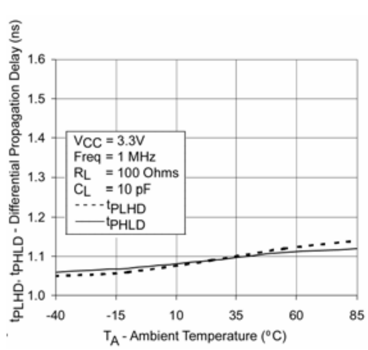

Figure 16.Differential Propagation Delay vs. Ambient Temperature

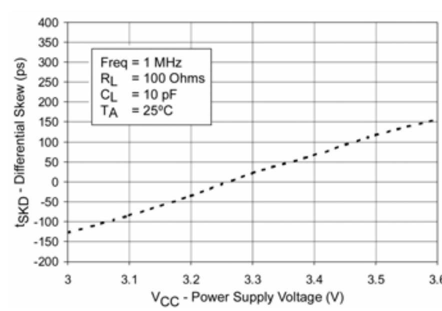

Figure 17.Differential Pulse Skew (t_{PLH} - t_{PHL}) vs. Power Supply Voltage

Typical Performance Characteristics

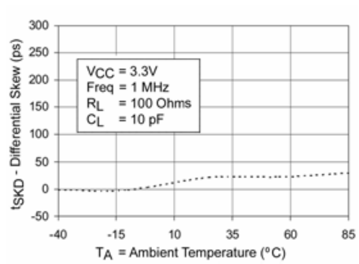

Figure 18.Differential Pulse Skew (t_{PLH} - t_{PHL}) vs. Ambient Temperature

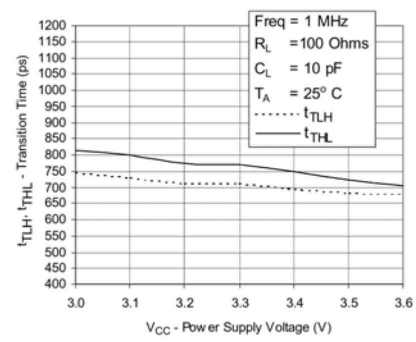

Figure 19.Transition Time vs. Power Supply Voltage

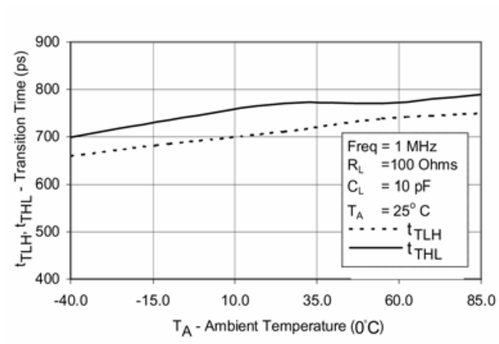

Figure 20.Transition Time vs. Ambient Temperature

Physical Dimensions

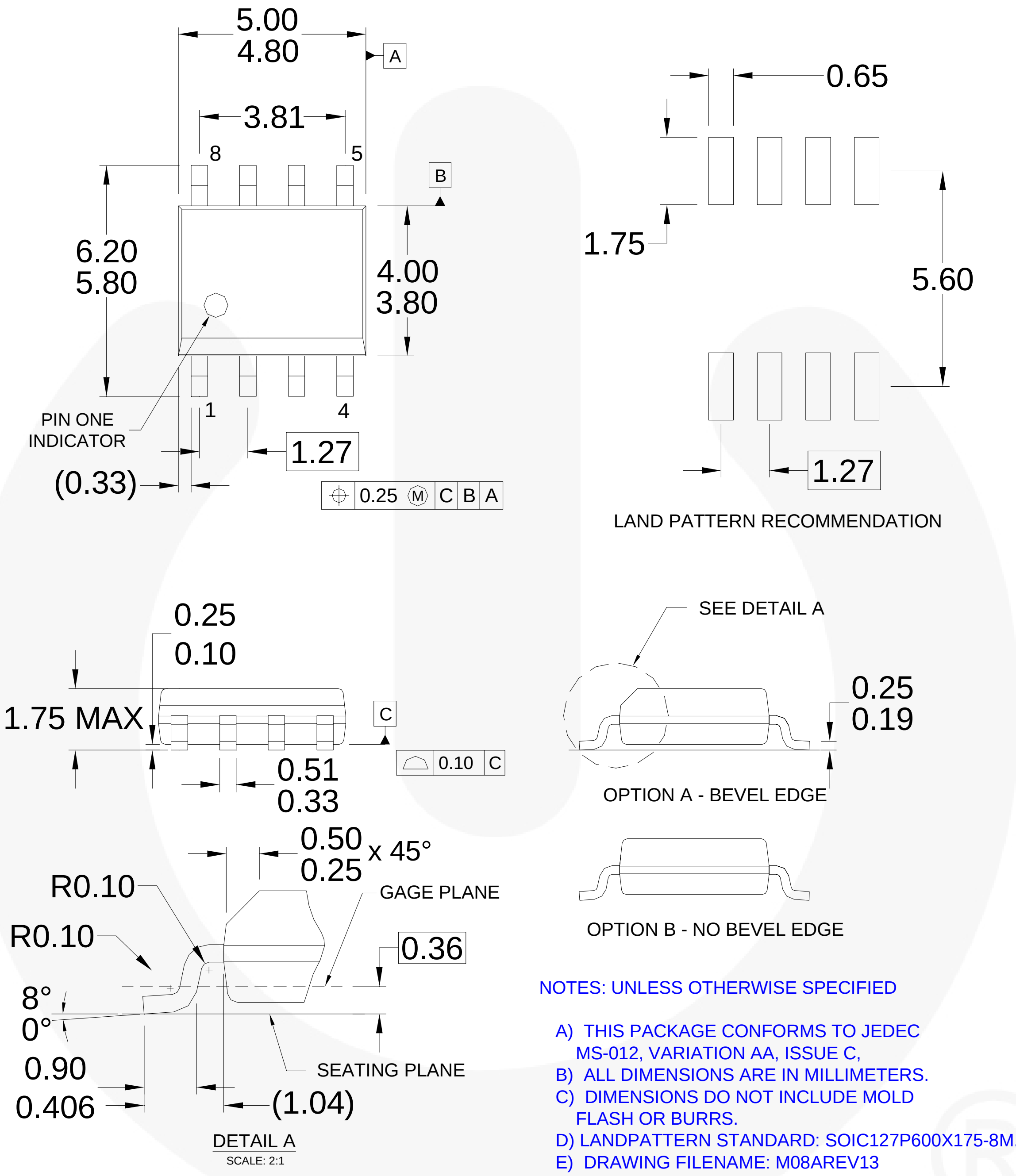

Figure 21.8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150inch Narrow

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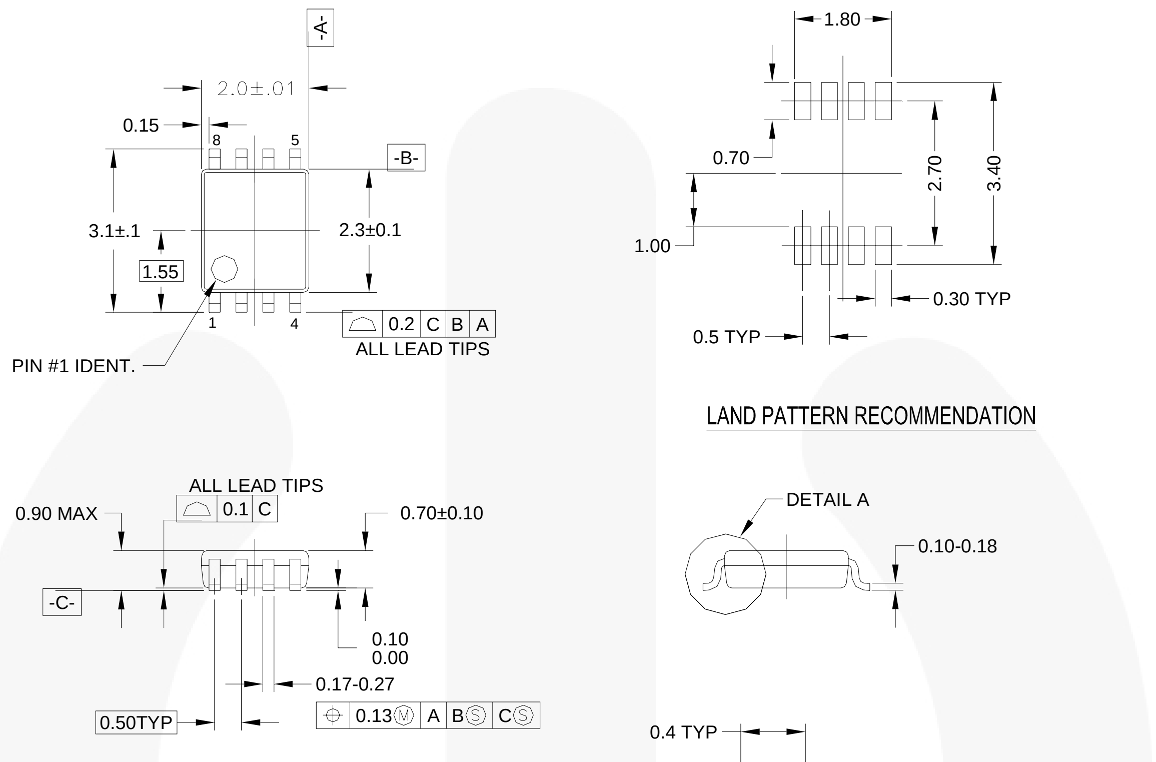
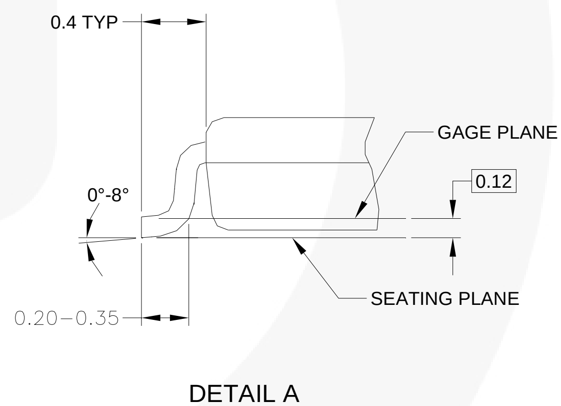
Physical Dimensions





NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-187
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MAB08AREVC

Figure 22.8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide

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