

FIN1002 LVDS 1-Bit High Speed Differential Receiver

General Description

This single receiver is designed for high speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. The receiver translates LVDS levels, with a typical differential input threshold of 100 mV, to LVTTTL signal levels. LVDS provides low EMI at ultra low power dissipation even at high frequencies. This device is ideal for high speed transfer of clock or data.

The FIN1002 can be paired with its companion driver, the FIN1001, or with any other LVDS driver.

Features

- Greater than 400Mbps data rate
- 3.3V power supply operation
- 0.4ns maximum pulse skew
- 2.5ns maximum propagation delay
- Bus pin ESD (HBM) protection exceeds 10kV
- Power-Off over voltage tolerant input and output
- Fail safe protection for open-circuit and non-driven, shorted or terminated conditions
- High impedance output at $V_{CC} < 1.5V$
- Meets or exceeds the TIA/EIA-644 LVDS standard
- 5-Lead SOT23 package saves space

Ordering Code:

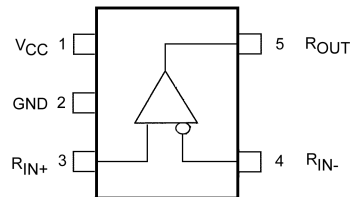
Order Number	Package Number	Package Description
FIN1002M5	MA05B	5-Lead SOT23, JEDEC MO-178, 1.6mm [250 Units on Tape and Reel]
FIN1002M5X	MA05B	5-Lead SOT23, JEDEC MO-178, 1.6mm [3000 Units on Tape and Reel]

Pin Descriptions

Pin Name	Description
R_{OUT}	LVTTTL Data Output
R_{IN+}	Non-inverting Driver Input
R_{IN-}	Inverting Driver Input
V_{CC}	Power Supply
GND	Ground
NC	No Connect

Connection Diagram

Pin Assignment for SOT package



Top View

Function Table

Input		Outputs
R_{IN+}	R_{IN-}	R_{OUT}
L	H	L
H	L	H
Fail Safe Condition		H

H = HIGH Logic Level
L = LOW Logic Level
Fail Safe = Open, Shorted, Terminated

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	-0.5V to +4.6V
DC Input Voltage (R_{IN+} , R_{IN-})	-0.5V to +4.6V
DC Output Voltage (D_{OUT})	-0.5V to +6V
DC Output Current (I_O)	16 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C
Max Junction Temperature (T_J)	150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	3.0V to 3.6V
Input Voltage (V_{IN})	0 to V_{CC}
Magnitude of Differential Voltage ($ V_{ID} $)	100mV to V_{CC}
Common-mode Input Voltage (V_{IC})	(0V + $ V_{ID} /2$) to (2.4 - $ V_{ID} /2$)
Operating Temperature (T_A)	-40°C to +85°C
ESD (Human Body Model)	
All Pins	8kV
LVDS pins to GND	10kV
ESD (Machine Model)	400V

Note 1: The "Absolute Maximum Ratings" are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specification.

DC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ (Note 2)	Max	Units
V_{TH}	Differential Input Threshold HIGH	See Figure 1; $V_{IC} = +0.05V, 1.2V, \text{ or } 2.35V$			100	mV
V_{TL}	Differential Input Threshold LOW	See Figure 1; $V_{IC} = +0.05V, 1.2V, \text{ or } 2.35V$	-100			mV
I_{IN}	Input Current	$V_{IN} = 0V \text{ or } V_{CC}$			± 20	μA
$I_{I(OFF)}$	Power-OFF Input Current	$V_{CC} = 0V, V_{IN} = 0V \text{ or } 3.6V$			± 20	μA
V_{OH}	Output HIGH Voltage	$I_{OH} = -100 \mu A$	$V_{CC} - 0.2$	3.3		V
		$I_{OH} = -8 \text{ mA}$	2.4	3.1		
V_{OL}	Output LOW Voltage	$I_{OH} = 100 \mu A$		0.0	0.2	V
		$I_{OL} = 8 \text{ mA}$		0.16	0.5	
V_{IK}	Input Clamp Voltage	$I_{IK} = -18 \text{ mA}$	-1.5	0.8		V
I_{CC}	Power Supply Current	($R_{IN+} = 1V \text{ and } R_{IN-} = 1.4V$), or ($R_{IN+} = 1.4V \text{ and } R_{IN-} = 1V$)		4	7	mA
C_{IN}	Input Capacitance	$V_{CC} = 3.3V$		2.3		pF
C_{OUT}	Output Capacitance	$V_{CC} = 0V$		2.8		pF

Note 2: All typical values are at $T_A = 25^\circ C$ and with $V_{CC} = 3.3V$.

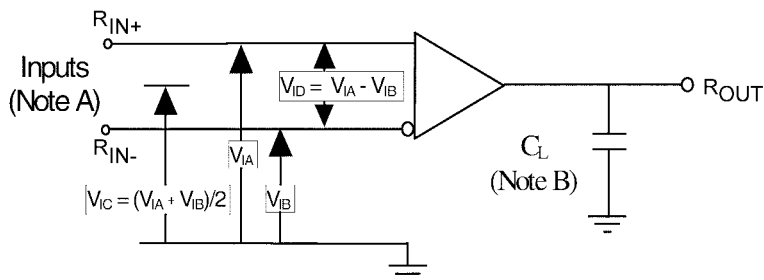
AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ (Note 3)	Max	Units	
t_{PLH}	Propagation Delay LOW-to-HIGH	See Figure 1 and Figure 2	0.9	1.5	2.5	ns	
t_{PHL}	Propagation Delay HIGH-to-LOW		0.9	1.5	2.5	ns	
t_{TLH}	Output Rise Time (20% to 80%)		$ V_{ID} = 400 \text{ mV}, C_L = 10 \text{ pF}$		0.6		ns
t_{THL}	Output Fall Time (80% to 20%)				0.5		ns
$t_{SK(P)}$	Pulse Skew ($t_{PLH} - t_{PHL}$)				0.02	0.4	ns
$t_{SK(PP)}$	Part-to-Part Skew (Note 4)					1.0	ns

Note 3: All typical values are at $T_A = 25^\circ C$ and with $V_{CC} = 3.3V$.

Note 4: $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.



Note A: All input pulses have frequency = 10MHz, t_r or $t_f = 1$ ns
Note B: C_L includes all probe and fixture capacitances

FIGURE 1. Differential Receiver Voltage Definitions and Propagation Delay and Transition Time Test Circuit

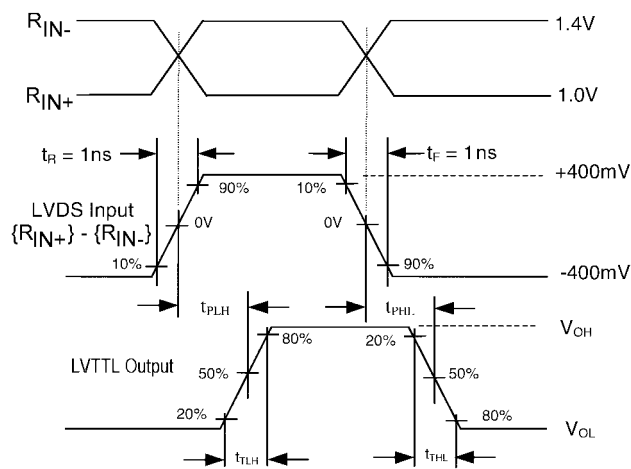


FIGURE 2. LVDS Input to LVTTTL Output AC Waveforms

DC / AC Typical Performance Curves

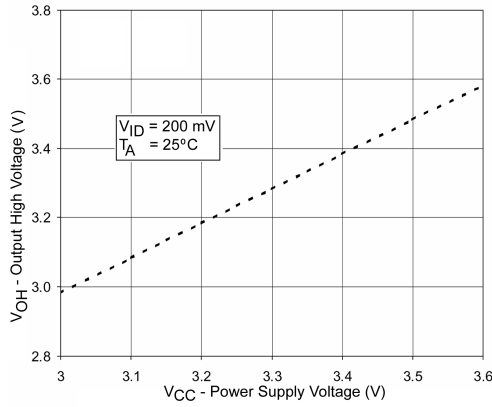


FIGURE 3. Output High Voltage vs. Power Supply Voltage

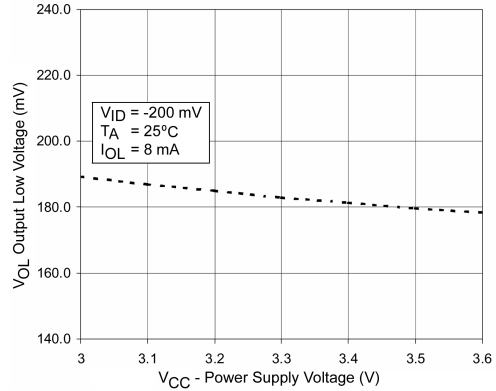


FIGURE 4. Output Low Voltage vs. Power Supply Voltage

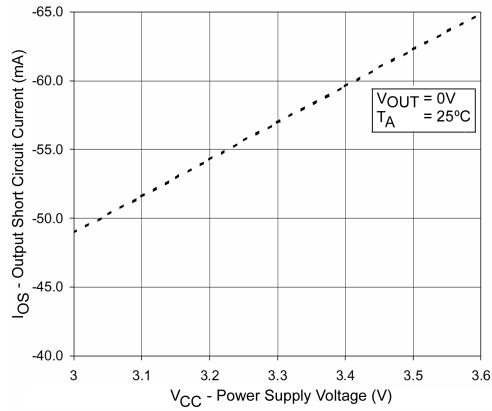


FIGURE 5. Output Short Circuit Current vs. Power Supply Voltage

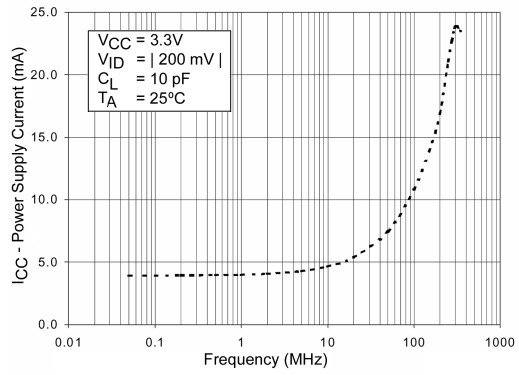


FIGURE 6. Power Supply Current vs. Frequency

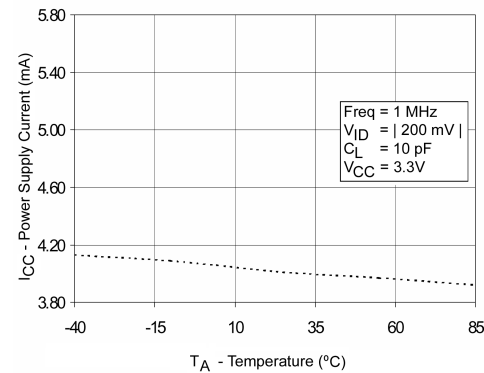


FIGURE 7. Power Supply Current vs. Ambient Temperature

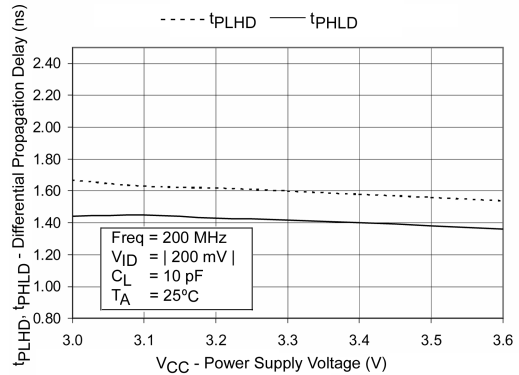


FIGURE 8. Differential Propagation Delay Power Supply Voltage

DC / AC Typical Performance Curves (Continued)

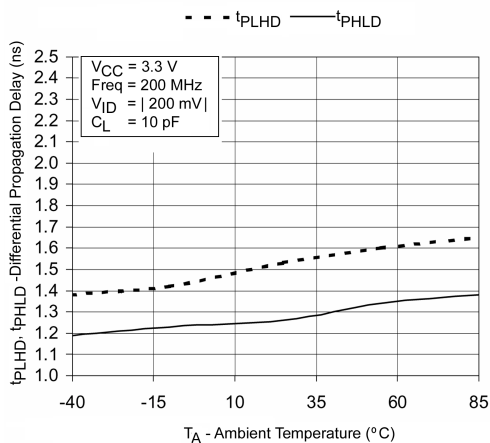


FIGURE 9. Differential Propagation Delay vs. Ambient Temperature

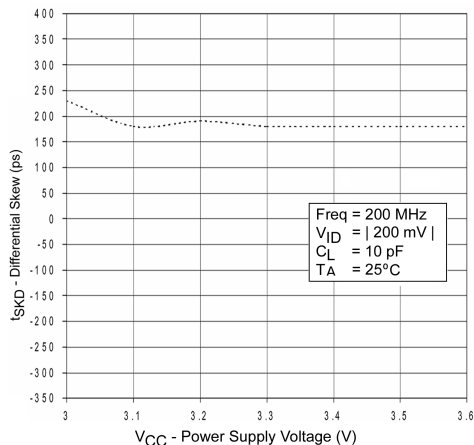


FIGURE 10. Differential Skew vs. Power Supply Voltage

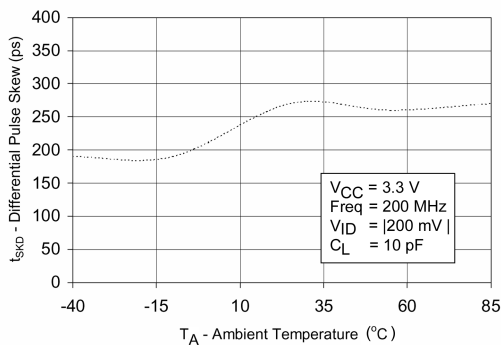


FIGURE 11. Differential Skew vs. Ambient Temperature

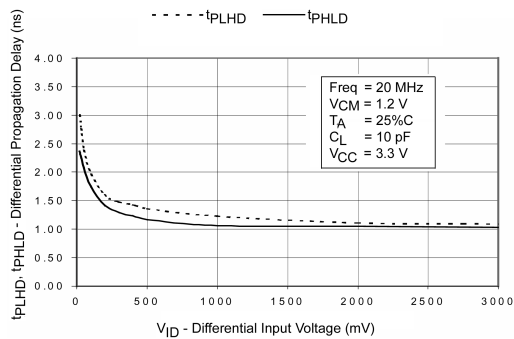


FIGURE 12. Differential Propagation Delay vs. Differential Input Voltage

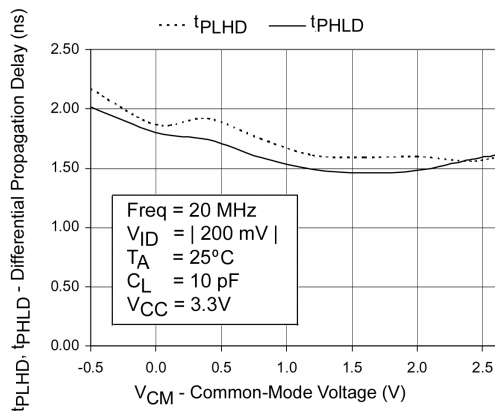


FIGURE 13. Differential Propagation Delay vs. Common-Mode Voltage

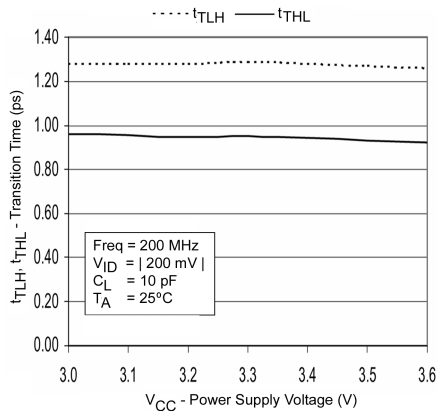


FIGURE 14. Transition Time vs. Power Supply Voltage

DC / AC Typical Performance Curves (Continued)

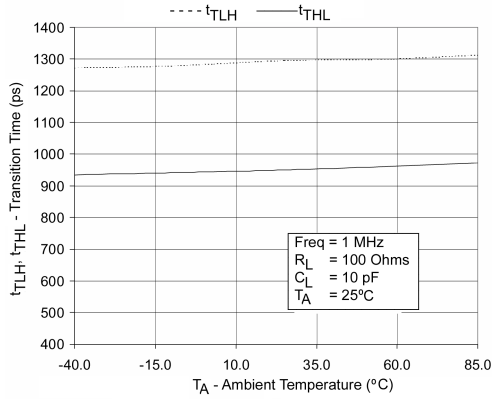


FIGURE 15. Transition Time vs. Ambient Temperature

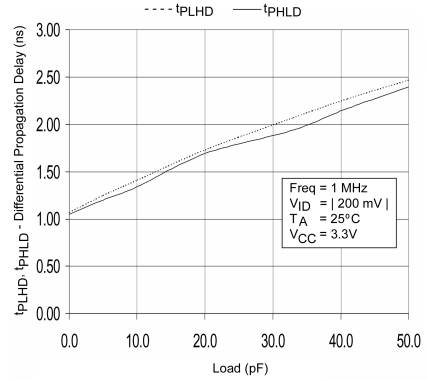


FIGURE 16. Differential Propagation Delay vs. Load

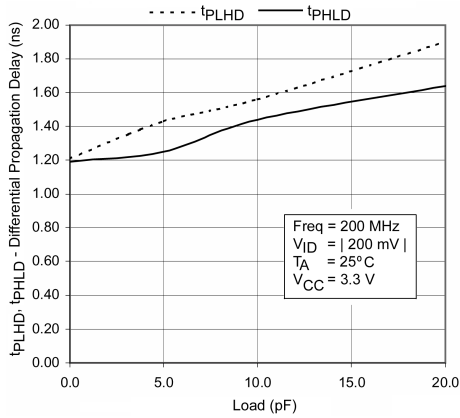


FIGURE 17. Differential Propagation Delay vs. Load

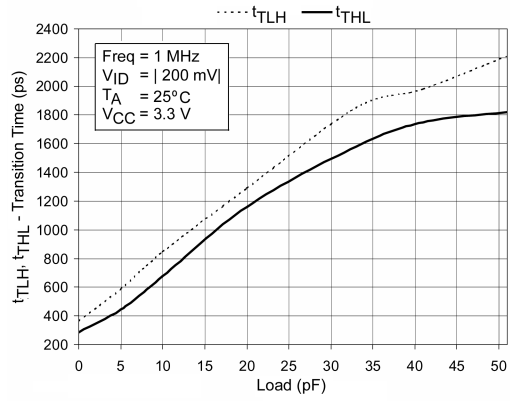


FIGURE 18. Transition Time vs. Load

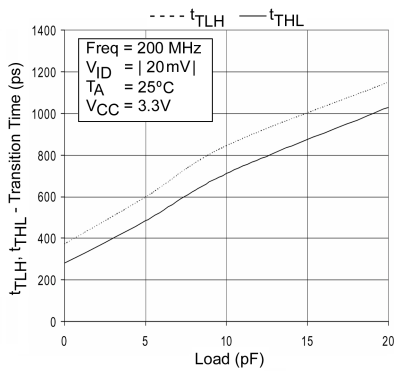


FIGURE 19. Transition Time vs. Load

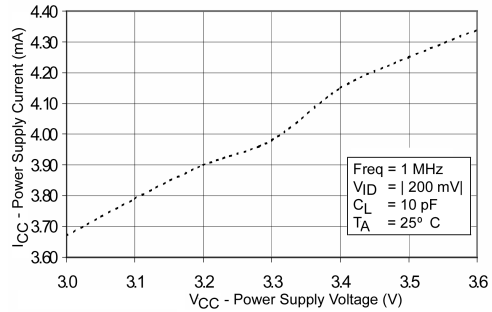
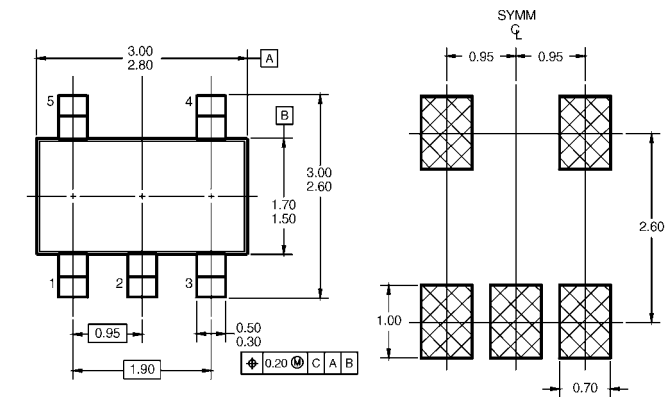
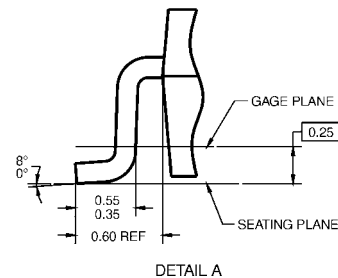
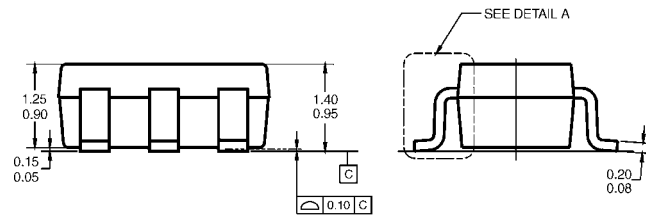


FIGURE 20. Power Supply Current vs. Power Supply Voltage

Physical Dimensions inches (millimeters) unless otherwise noted



LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED
 A) THIS PACKAGE CONFORMS TO JEDEC MO-178, ISSUE B, VARIATION AA, DATED JANUARY 1999.
 B) ALL DIMENSIONS ARE IN MILLIMETERS.

MA05BRevC

**5-Lead SOT23, JEDEC MO-178, 1.6mm
 Package Number MA05B**

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