



FHP3194

4:1 High-Speed Multiplexer

Features

- 0.1dB gain flatness to 90MHz @ 2V_{pp}
- 0.02%/0.05° differential gain/phase error
- 500MHz large signal -3dB bandwidth at G = 2
- 2200V/μs slew rate
- 75mA output current (easily drives two video loads)
- 70dB channel-to-channel isolation
- 13mA supply current
- 3.5mA supply current in disable mode
- 2.5mA supply current in shutdown mode
- Fully specified at ±5V supplies
- Lead-free SOIC-14 and TSSOP-14 packages

Applications

- Video switchers and routers
- Multiple input HDTV switching
- Picture-in-picture video switch
- Multi-channel ADC driver

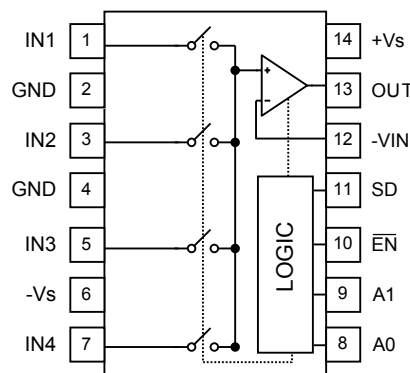
Description

The FHP3194 is a 4:1 analog multiplexer designed for high-speed video applications. The output amplifier is a high-speed current feedback amplifier that offers stellar large signal performance of 500MHz -3dB bandwidth and 90MHz 0.1dB bandwidth. The gain of the output amplifier is selectable through two external resistors (R_f and R_g), allowing further design flexibility. The 2V_{pp} bandwidth performance and 2200V/μs slew rate exceed the requirements of high-definition television (HDTV) and other multimedia applications. The output amplifier also provides ample output current to drive multiple video loads.

Two address bits (A0 and A1) are used to select one of the four inputs. The FHP3194 offers better than 70dB channel isolation.

The FHP3194 offers both shutdown and disable capability. During shutdown, the FHP3194 consumes only 2.5mA of supply current. During disable mode, only the output amplifier is disabled, reducing output glitches and allowing for multiplexer expansion.

Functional Block Diagram

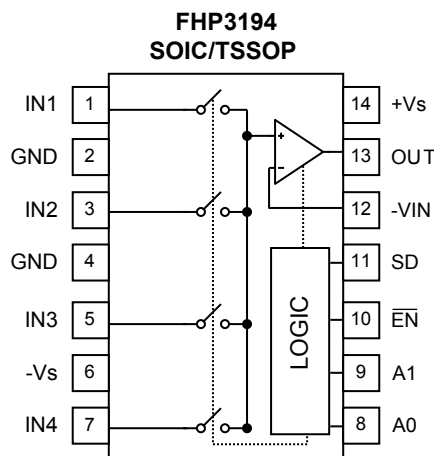


Ordering Information

| Part Number | Package | Pb-Free | Operating Temperature Range | Packaging Method |
|----------------|----------|---------|-----------------------------|------------------|
| FHP3194IM14X | SOIC-14 | Yes | -40°C to +85°C | Reel |
| FHP3194IMTC14X | TSSOP-14 | Yes | -40°C to +85°C | Reel |

Moisture sensitivity level for all parts is MSL-1.

Pin Configuration



Pin Assignments

| Pin# | Pin Name | Description |
|------|-----------------|---|
| 1 | IN1 | Input, channel 1 |
| 2 | GND | Must be connected to ground |
| 3 | IN2 | Input, channel 2 |
| 4 | GND | Must be connected to ground |
| 5 | IN3 | Input, channel 3 |
| 6 | -Vs | Negative supply |
| 7 | IN4 | Input, channel 4 |
| 8 | A0 | Logic input A0 |
| 9 | A1 | Logic input A1 |
| 10 | \overline{EN} | Enable pin, "1" = Disable, "0" = Enable; Enabled when left floating |
| 11 | SD | Shutdown pin, "1" = Shutdown, "0" = Active; Active when left floating |
| 12 | -VIN | Inverting Input of output amplifier |
| 13 | OUT | Output |
| 14 | +Vs | Positive supply |

Truth Table

| A0 | A1 | \overline{EN} | SD | OUT |
|----|----|-----------------|----|----------|
| 1 | 1 | 0 | 0 | CH4 |
| 0 | 1 | 0 | 0 | CH3 |
| 1 | 0 | 0 | 0 | CH2 |
| 0 | 0 | 0 | 0 | CH1 |
| X | X | 1 | 0 | Disable |
| X | X | X | 1 | Shutdown |

Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table defines the conditions for actual device operation.

| Parameter | Min. | Max. | Unit |
|---------------------|---------------|---------------|------|
| Supply Voltage | 0 | 12.6 | V |
| Input Voltage Range | $-V_s - 0.5V$ | $+V_s + 0.5V$ | V |

Reliability Information

| Parameter | Min. | Typ. | Max. | Unit |
|-----------------------------------|------|------|------|------|
| Junction Temperature | | | 150 | °C |
| Storage Temperature Range | -65 | | 150 | °C |
| Lead Temperature (Soldering, 10s) | | | 300 | °C |
| Package Thermal Resistance | | | | |
| 14-Lead TSSOP ¹ | | 113 | | °C/W |
| 14-Lead SOIC ¹ | | 125 | | °C/W |

Notes:

1. Package thermal resistance (θ_{JA}), JEDEC standard, multi-layer test boards, still air.

ESD Protection

| Product | SOIC-14 | TSSOP-14 |
|----------------------------|---------|----------|
| Human Body Model (HBM) | 3.5kV | 3kV |
| Charged Device Model (CDM) | 2kV | 2kV |

Recommended Operating Conditions

| Parameter | Min. | Typ. | Max. | Unit |
|-----------------------------|------|------|------|------|
| Operating Temperature Range | -40 | | +85 | °C |
| Supply Voltage Range | 5 | | 12 | V |

Electrical Characteristics at $\pm 5V$

$T_A = 25^\circ\text{C}$, $V_S = \pm 5V$, $R_f = 475\Omega$, $R_L = 150\Omega$, $G = 2$; unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|------------------------------------|---|---|------|---------|------|------------------------------|
| Frequency Domain Response | | | | | | |
| UGBW | -3dB Bandwidth | $G = +1$, $R_f = 1.5k\Omega$ $V_{OUT} = 0.2V_{pp}$ | | 1200 | | MHz |
| BW _{SS} | -3dB Bandwidth | $G = +2$, $V_{OUT} = 0.2V_{pp}$ | | 800 | | MHz |
| BW _{LS} | Full Power Bandwidth | $G = +2$, $V_{OUT} = 2V_{pp}$ | | 500 | | MHz |
| | 0.1dB Gain Flatness | $G = +2$, $V_{OUT} = 0.2V_{pp}$ | | 200 | | MHz |
| | 0.1dB Gain Flatness | $G = +2$, $V_{OUT} = 2V_{pp}$ | | 90 | | MHz |
| Time Domain Response | | | | | | |
| t_R, t_F | Rise and Fall Time | $V_{OUT} = 2V$ step; (10% to 90%) | | 1 | | ns |
| t_S | Settling Time to 0.1% | $V_{OUT} = 2V$ step | | 15 | | ns |
| OS | Overshoot | $V_{OUT} = 0.2V$ step | | 4 | | % |
| SR | Slew Rate | 4V step | | 2200 | | V/ μ s |
| Distortion / Noise Response | | | | | | |
| HD2 | 2nd Harmonic Distortion | $2V_{pp}$, 5MHz, worst channel | | -68 | | dBc |
| HD3 | 3rd Harmonic Distortion | $2V_{pp}$, 5MHz, worst channel | | -89 | | dBc |
| THD | Total Harmonic Distortion | $2V_{pp}$, 5MHz, worst channel | | -67 | | dB |
| DG | Differential Gain | NTSC (3.58MHz), DC-coupled | | 0.02 | | % |
| DP | Differential Phase | NTSC (3.58MHz), DC-coupled | | 0.05 | | $^\circ$ |
| e_n | Input Voltage Noise | > 1MHz | | 7 | | nV/ $\sqrt{\text{Hz}}$ |
| i_{n+} | Input Current Noise (+) | > 1MHz | | 22 | | pA/Hz |
| i_{n-} | Input Current Noise (-) | > 1MHz | | 16 | | pA/Hz |
| X _{TALK} | All Hostile Crosstalk | Channel-to-channel 5MHz/ 30MHz, worst CH combination | | -68/-53 | | dB |
| DC Performance | | | | | | |
| V_{IO} | Input Offset Voltage ⁽¹⁾ | | -9 | 1 | +9 | mV |
| dV_{IO} | Average Drift | | | 8.5 | | $\mu\text{V}/^\circ\text{C}$ |
| V_{IOM} | Input Offset Voltage Matching ⁽¹⁾ | Channel-to-channel | -5 | 0.8 | 5 | mV |
| I_{bn} | Input Bias Current Non-inverting ⁽¹⁾ | Pins 1,3,5,7 | -30 | 4 | 30 | μA |
| dI_{bn} | Average Drift | | | 25 | | nA/ $^\circ\text{C}$ |
| I_{bi} | Input Bias Current Inverting ⁽¹⁾ | Pin 12 | -35 | 13 | 35 | μA |
| dI_{bni} | Average Drift | | | 20 | | nA/ $^\circ\text{C}$ |
| GM | Gain Matching | Channel-to-channel | | 0.02 | | % |
| PSRR | Power Supply Rejection Ratio ⁽¹⁾ | DC | 54 | 65 | | dB |
| I_S | Supply Current ⁽¹⁾ | | | 13 | 18 | mA |
| I_{EN} | Disable Supply Current ⁽¹⁾ | Disable mode | | 3.5 | 6 | mA |
| I_{SD} | Shutdown Supply Current ⁽¹⁾ | Shutdown mode | | 2.5 | 5 | mA |
| Switching Characteristics | | | | | | |
| T_S | Switching Time 50% Logic to: | Channel-to-channel | | | | |
| | 90% output (10% output settling) ⁽²⁾ | IN1, IN3 = +0.5V; IN2, IN4 = -0.5V | | 25 | | ns |
| | 99% output (1% output settling) ⁽²⁾ | IN1, IN3 = +0.5V; IN2, IN4 = -0.5V | | 40 | | ns |
| V_{SW} | Channel Switch. Trans. (Glitch) | All inputs grounded | | 375 | | mV _{pp} |

Notes:

1. 100% tested at 25°C

Electrical Characteristics at $\pm 5V$ (Continued)

$T_A = 25^\circ\text{C}$, $V_S = \pm 5V$, $R_f = 475\Omega$, $R_L = 150\Omega$, and $G = 2$ unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------------------------------|--|---|-----------|-----------|------|---------------|
| Digital Inputs | | | | | | |
| V_{IH} | Logic-High Threshold | A0, A1, \overline{EN} , and SD pins | 2.0 | | | V |
| V_{IL} | Logic-Low Threshold | A0, A1, \overline{EN} , and SD pins | | | 0.8 | V |
| I_{IH} | Logic Pin Input Current High | A0, A1, \overline{EN} , and SD pins Logic input = 0V | | 22 | | μA |
| I_{IL} | Logic Pin Input Current Low | A0, A1, \overline{EN} , and SD pins Logic input = 0V | | 0 | | μA |
| Disable Characteristics | | | | | | |
| \overline{EN}_{ISO} | Disable Isolation | 5MHz/30MHz, worst comb. | | -76/-61 | | dB |
| SD_{ISO} | Shutdown Isolation | 5MHz/30MHz, worst comb. | | -76/-61 | | dB |
| CH_{ISO} | CH-to-CH Isolation ⁽³⁾ | 5MHz/30MHz, worst comb. | | -70/-55 | | dB |
| \overline{EN}_{TON} | Turn-on time (Disable to ON) | $V_{IN} = 500\text{mV}$ | | 30 | | ns |
| \overline{EN}_{TOFF} | Turn-off time (ON to Disable) | $V_{IN} = 500\text{mV}$ | | 65 | | ns |
| SD_{TON} | Turn-on time (Shutdown to ON) | $V_{IN} = 500\text{mV}$ | | 32 | | ns |
| SD_{TOFF} | Turn-off time (ON to Shutdown) | $V_{IN} = 500\text{mV}$ | | 66 | | ns |
| Input Characteristics | | | | | | |
| R_{IN} | Input Resistance | | | 188 | | k Ω |
| C_{IN} | Input Capacitance | | | 1.7 | | pF |
| CMIR | Input Common Mode V Range | | | ± 3.1 | | V |
| CMRR | Common Mode Rejection Ratio ⁽¹⁾ | DC | 50 | 60 | | dB |
| Output Characteristics | | | | | | |
| V_{OUT} | Output Voltage Swing | $R_L = 2\text{k}\Omega$ | | ± 4.0 | | V |
| | | $R_L = 150\Omega^{(1)}$ | ± 3.2 | ± 3.8 | | V |
| I_{OUT} | Linear Output Current | $V_{IN} = 0$ | | ± 75 | | mA |
| I_{SC} | Short-Circuit Output Current | $V_{OUT} = \text{GND}$, $R_L = 0\Omega$ | | ± 100 | | mA |
| R_{OUT} | Output Resistance | Enabled | | 0.1 | | Ω |
| | | Disabled | | 1 | | k Ω |
| C_{OUT} | Output Capacitance | | | 3.7 | | pF |

Notes:

1. 100% tested at 25°C

2. SD and \overline{EN} pins are grounded. IN1 and IN3 = +0.5V, IN2 and IN4 = -0.5V, see truth table to properly set A0 and A1 based on the channels driven. Switching time is the transition time from 50% of A0 or A1 input value (+2.5V) to the time at which the switched channel is at 90% (or 99%) of its final value.

3. Driving one channel and looking at worst case value from remaining channels.

Typical Performance Characteristics

$T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_f = 475\Omega$, $R_L = 150\Omega$, and $G = 2$ unless otherwise noted.

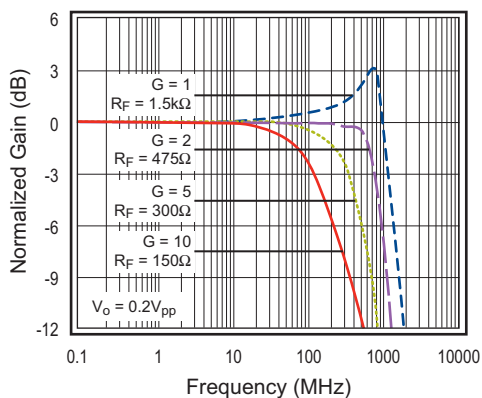


Figure 1. Non-Inverting Freq. Response

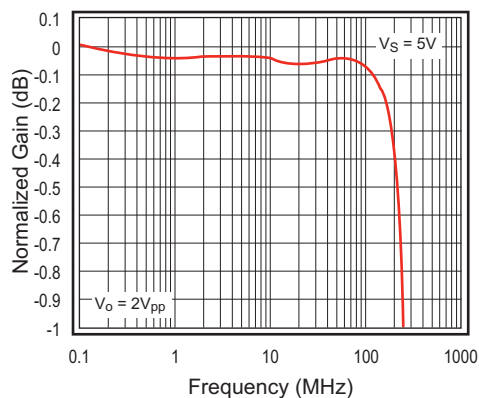


Figure 2. Gain Flatness vs. Frequency

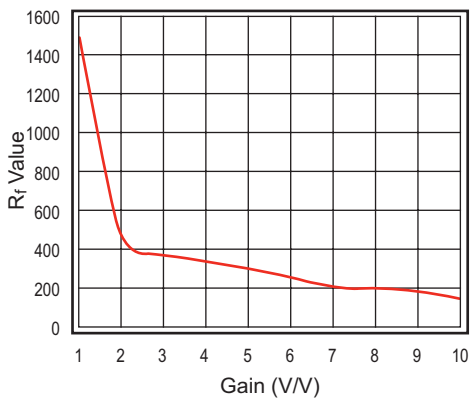


Figure 3. Recommended R_f vs. Gain

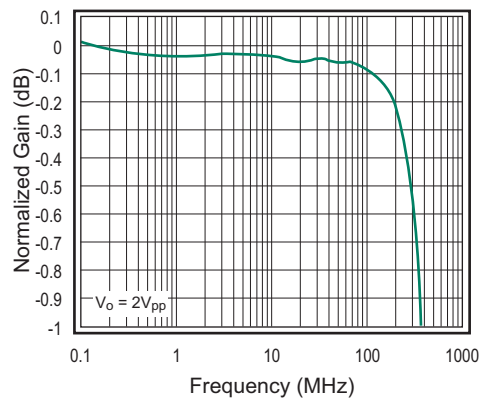


Figure 4. Gain Flatness vs. Frequency

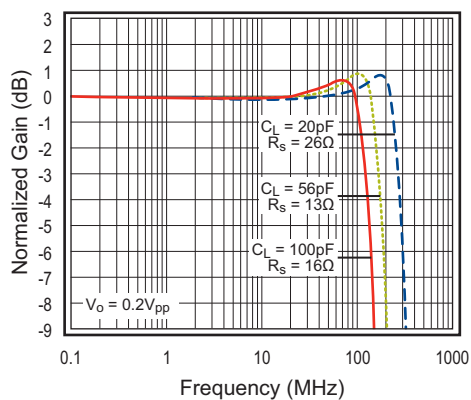


Figure 5. Frequency Response vs. C_L

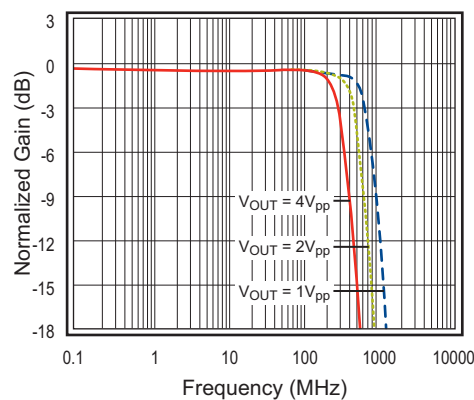


Figure 6. Frequency Response vs. V_{OUT}

Typical Performance Characteristics

$T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_f = 475\Omega$, $R_L = 150\Omega$, and $G = 2$ unless otherwise noted.

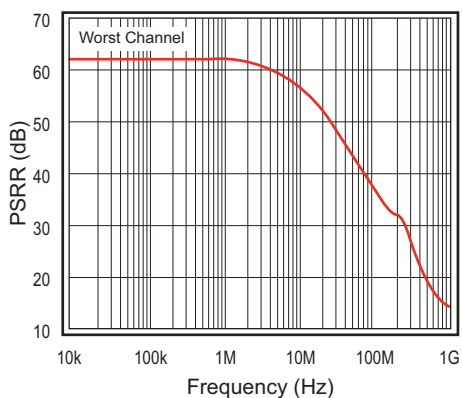


Figure 7. PSRR vs. Frequency

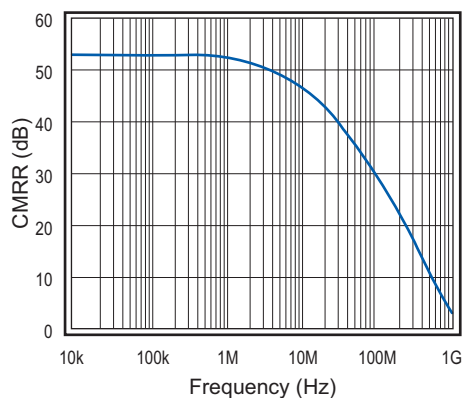


Figure 8. CMRR vs. Frequency

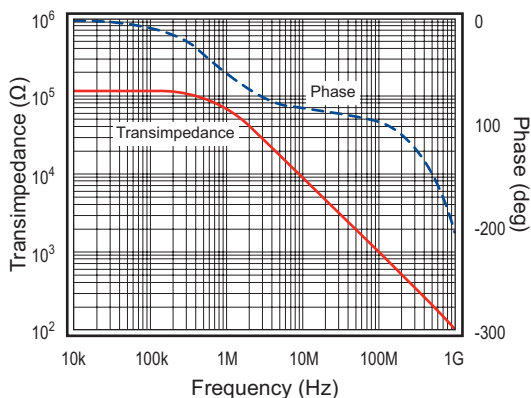


Figure 9. Open Loop Transimpedance Gain and Phase

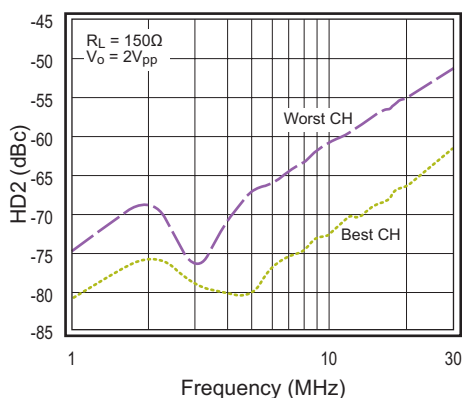


Figure 10. HD2 vs. Frequency

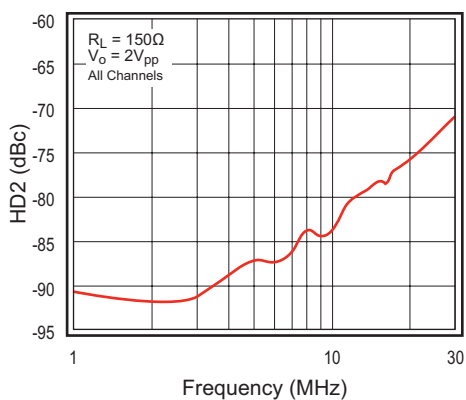


Figure 11. HD3 vs. Frequency

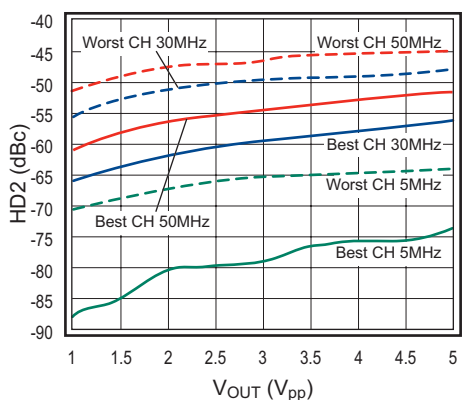


Figure 12. HD2 vs. V_{OUT}

Typical Performance Characteristics

$T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_f = 475\Omega$, $R_L = 150\Omega$, and $G = 2$ unless otherwise noted.

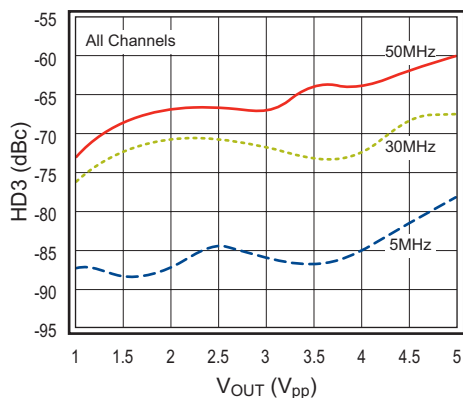


Figure 13. HD3 vs. V_{OUT}

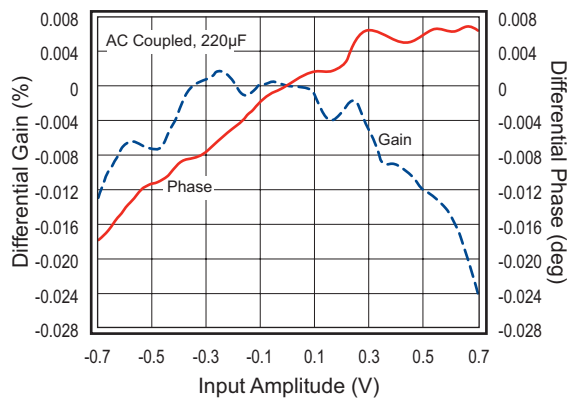


Figure 14. Differential Gain and Phase

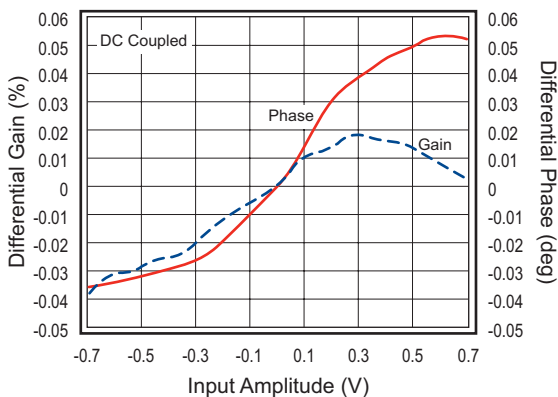


Figure 15. Differential Gain and Phase

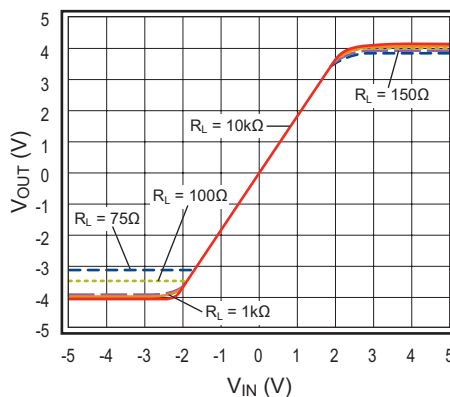


Figure 16. Output Swing vs. R_L

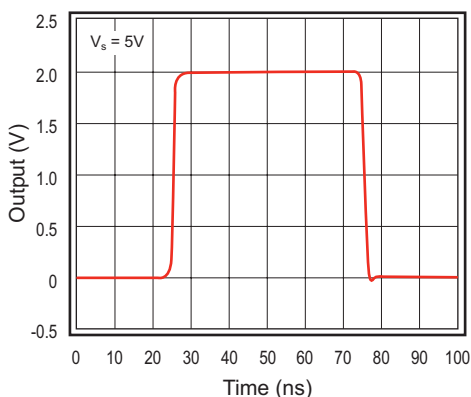


Figure 17. Pulse Response

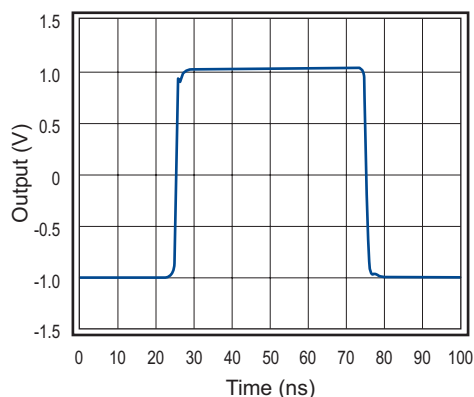


Figure 18. Pulse Response

Typical Performance Characteristics

$T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_f = 475\Omega$, $R_L = 150\Omega$, and $G = 2$ unless otherwise noted.

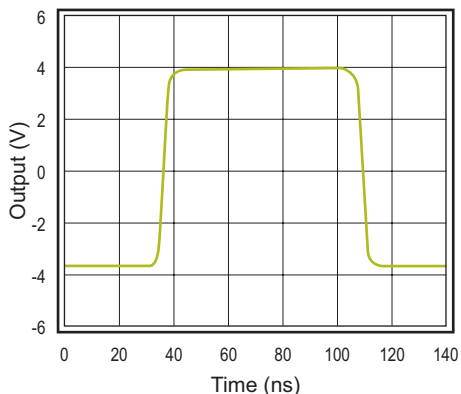


Figure 19. Pulse Response

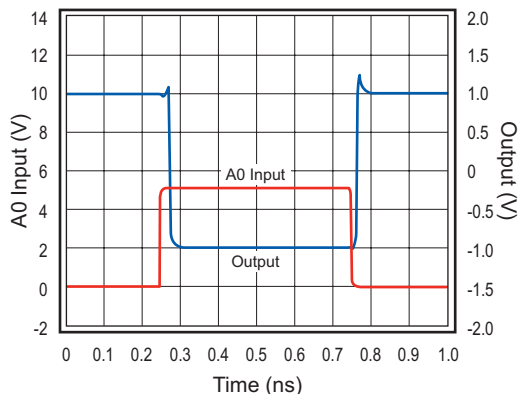


Figure 20. Channel Switching Time

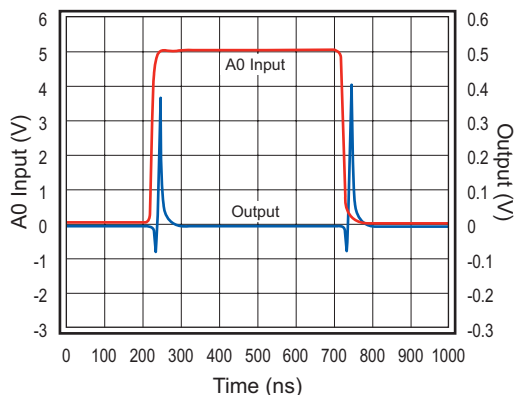


Figure 21. A0 Switching Glitch

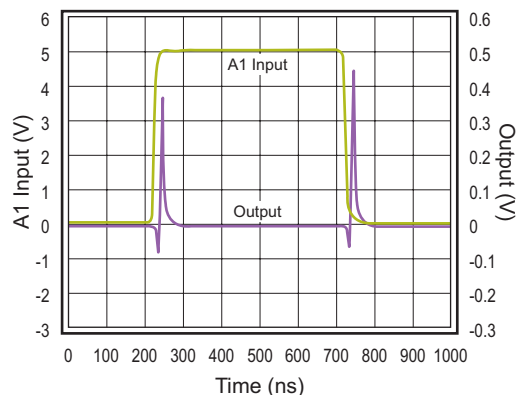


Figure 22. A1 Switching Glitch

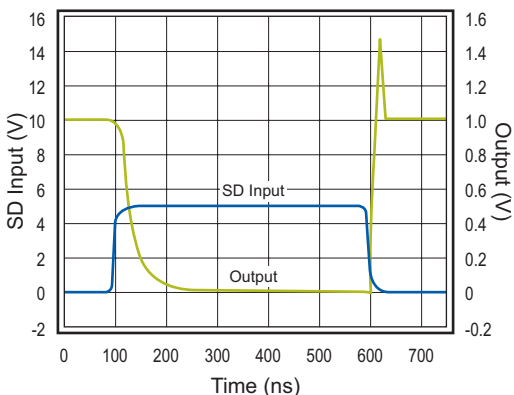


Figure 23. Shutdown Switching Time

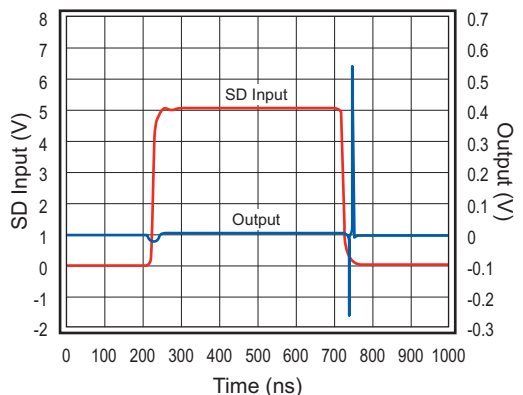


Figure 24. Shutdown Switching Glitch

Typical Performance Characteristics

$T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_f = 475\Omega$, $R_L = 150\Omega$, and $G = 2$ unless otherwise noted.

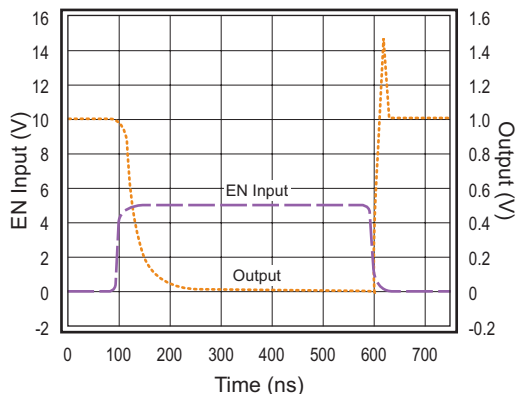


Figure 25. Enable Switching Time

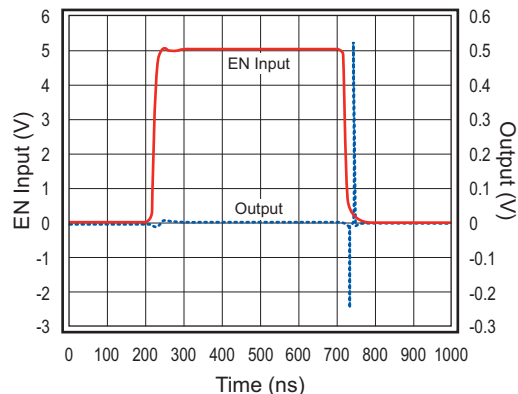


Figure 26. Enable Switching Glitch

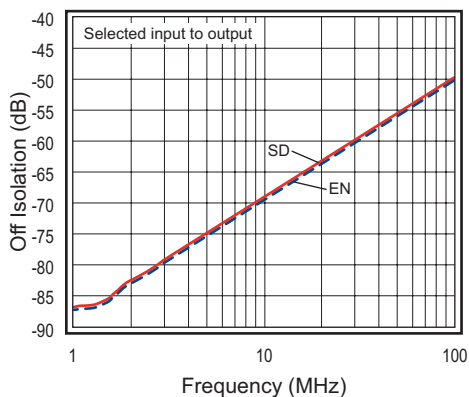


Figure 27. Off Isolation vs. Frequency

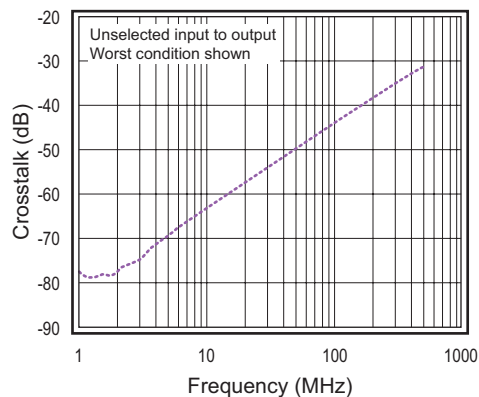


Figure 28. Crosstalk vs. Frequency

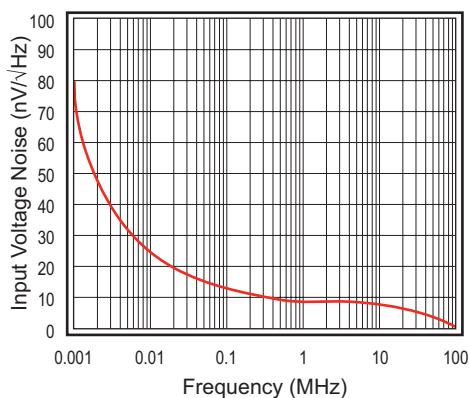


Figure 29. Input Voltage Noise

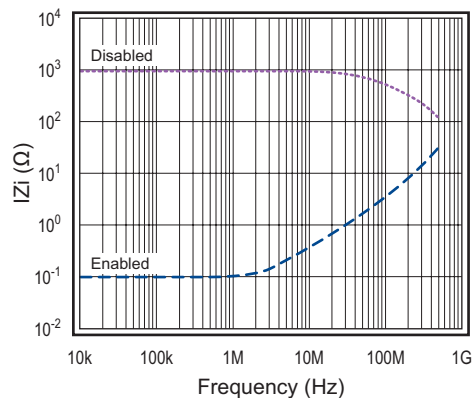


Figure 30. Closed-Loop Output Impedance

Application Information

Circuit Diagrams

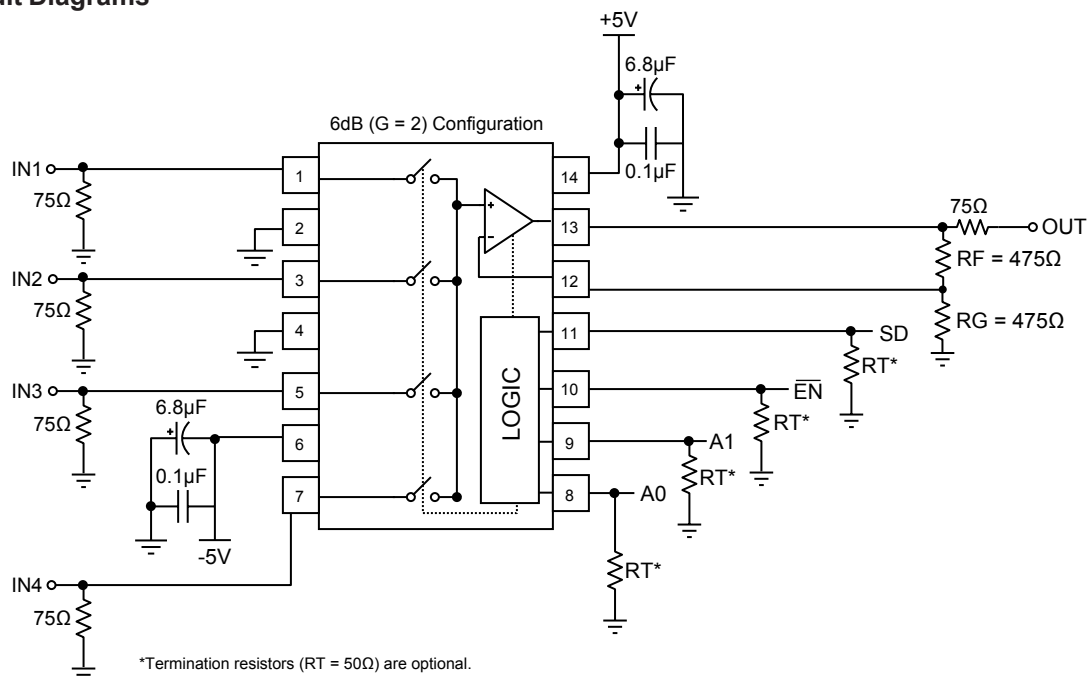


Figure 31. Typical Application Circuit 6dB Gain (G = 2)

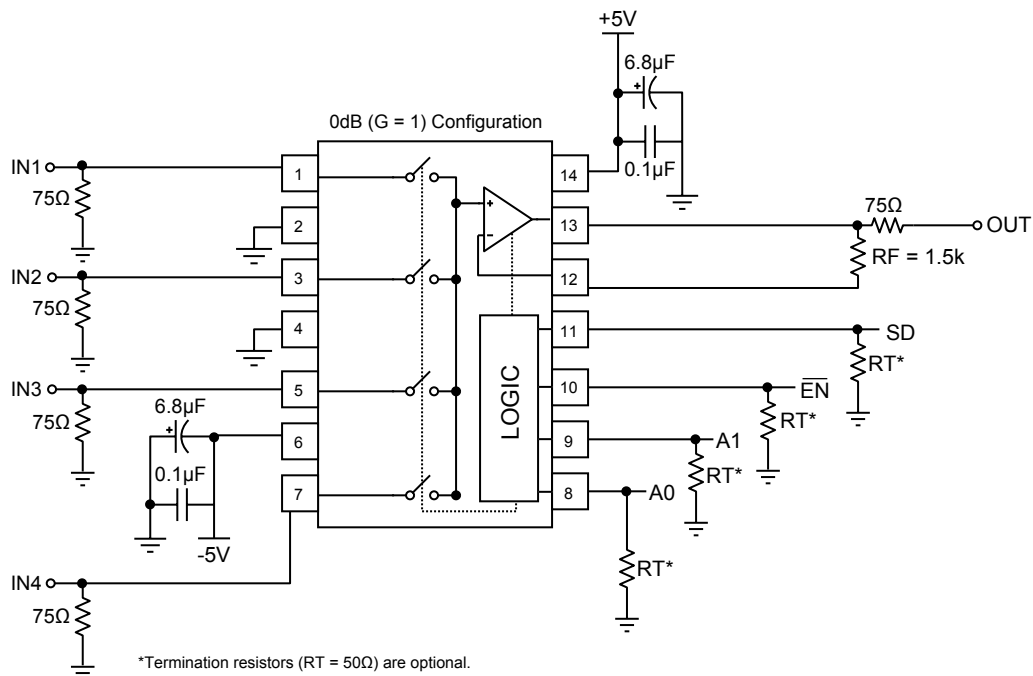


Figure 32. Typical Application Circuit 0dB Gain (G = 1)

Application Information

General Description

The FHP3194 4:1 multiplexer has four analog switches that drive the positive input of a high-speed current feedback amplifier. It is designed so that only one channel is on at a time. Tie unused inputs to ground.

Figures 31 and 32 show typical application circuits for the FHP3194 in 6dB ($G = 2$) and 0dB ($G = 1$) configurations.

R_f and R_g Selection

The output of the FHP3194 is a current feedback amplifier. The gain of this amplifier is set by two external resistors: R_f and R_g . The frequency response and closed-loop bandwidth of the current feedback amplifier are highly dependant on the value of R_f . For a gain of two, use $R_f = 475\Omega$. For other gains, refer to the R_f vs. GAIN plot in Figure 3. In general, a lower R_f peaks the frequency response and increases bandwidth, while a higher R_f will decrease bandwidth and roll off the frequency response. A feedback resistor is required for unity gain ($G = 1$); the recommended value is $1.5k\Omega$.

A0, A1

The A0 and A1 logic pins are TTL/CMOS compatible and are used to select which of the four inputs connects to the output. Refer to the TRUTH TABLE on page 2 for more information. Channel 1 is selected if both pins are left floating.

\overline{EN} , SD

The FHP3194 offers both shutdown and disable capability. The \overline{EN} (enable) pin is active low. During disable mode ($\overline{EN} = 1$), only the output amplifier is disabled, reducing output glitches and allowing for multiplexer expansion. The FHP3194 is enabled when the \overline{EN} pin is left floating or grounded.

The SD (shutdown) pin is active high. During shutdown ($SD = 1$), the FHP3194 consumes only 2.5mA of supply current. The FHP3194 is enabled when the SD pin is left floating or grounded.

Supply Voltage

The FHP3194 operates from a single supply of 5V to 12V or dual supplies of $\pm 2.5V$ to $\pm 6.0V$. For low supply voltage operation, ensure that the common mode input voltage range (CMIR) or output voltage range (V_o) are not exceeded. Exceeding the CMIR or V_o range puts the FHP3194 into an overdrive condition. For example, the typical CMIR for the FHP3194 is $\pm 3.1V$ at $\pm 5V$ supply, which means 1.9V of headroom is required from each supply.

At a single 5V supply, the CMIR becomes 1.9V to 3.1V. The same theory can be applied to the V_{OUT} range.

Driving Video

The FHP3194 is designed to drive high-speed video. 90MHz 0.1dB bandwidth at $2V_{pp}$ output, $0.02^\circ/0.05\%$ differential gain/phase, and $\pm 75mA$ output current make the FHP3194 suitable for driving standard-definition, high-definition, or PC graphics video.

Driving Video with a Single 5V Supply

The FHP3194 drives video signals from a single 5V supply at $G = 1$ only. At higher gains, the CMIR and V_o range is not suitable for passing video without clipping the signal.

Driving Capacitive Loads

The FREQUENCY RESPONSE VS. C_L plot in Figure 5, illustrates the response of the FHP3194. A small series resistance (R_s) at the output of the amplifier, illustrated in Figure 33, improves stability and settling performance. R_s values in the FREQUENCY RESPONSE VS. C_L plot were chosen to achieve maximum bandwidth with less than 1dB of peaking. For maximum flatness, use a larger R_s .

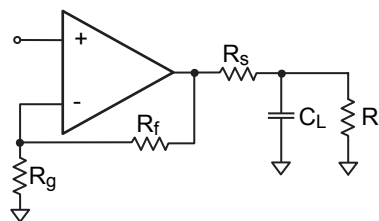


Figure 33. Typical Topology for Driving Capacitive Loads

Power Dissipation

The maximum internal power dissipation allowed is directly related to the maximum junction temperature. If the maximum junction temperature exceeds $150^\circ C$ for an extended time, device failure may occur. The FHP3194 is short-circuit protected; however, this may not guarantee that the maximum junction temperature ($+150^\circ C$) is not exceeded under all conditions. RMS power dissipation can be calculated using the following equation:

$$\text{Power Dissipation} = I_s * (V_{s+} - V_{s-}) + (V_{s+} - V_{o(RMS)}) * I_{OUT(RMS)}$$

where I_s is the supply current, V_{s+} is the positive supply pin voltage, V_{s-} is the negative supply pin voltage, $V_{o(RMS)}$ is the RMS output voltage, and $I_{OUT(RMS)}$ is the RMS output current delivered to the load. Follow the maximum power derating curves shown in Figure 34 to ensure proper operation.

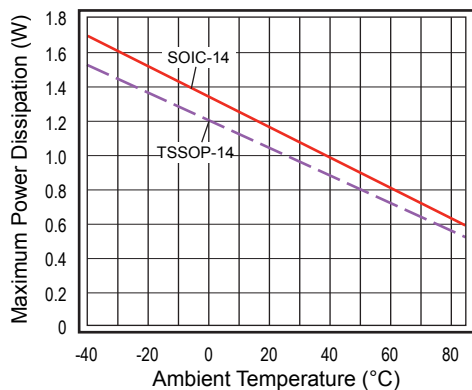


Figure 34. Maximum Power Derating

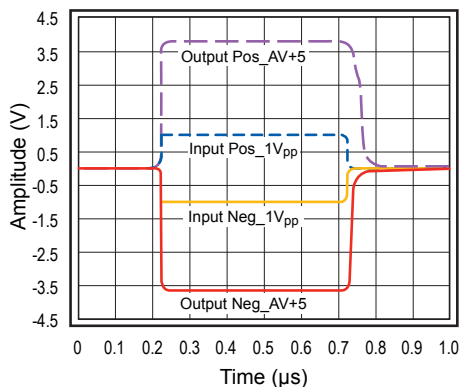


Figure 35. Overdrive Recovery

Overdrive Recovery

For an amplifier, an overdrive condition occurs when the output and/or input ranges are exceeded. The recovery time varies based on whether the input or output is overdriven and by how much the ranges are exceeded. The FHP3194 typically recovers in less than 75ns from an overdrive condition. Figure 35 shows the FHP3194 in an overdriven condition.

Layout Considerations

General layout and supply bypassing play major roles in high-frequency performance. Fairchild has evaluation boards to use as a guide for high-frequency layout and as aid in device testing and characterization. Follow the guidelines below as a basis for high-frequency layout:

- Include 6.8µF and 0.1µF ceramic capacitors.
- Place the 6.8µF capacitor within 0.75 inches of the power pin.
- Place the 0.1µF capacitor within 0.1 inches of the power pin.
- Remove the ground plane under and around the part, especially near the input and output pins and under R_f and R_g , to reduce parasitic capacitance.
- Minimize all trace lengths to reduce series inductances.

For current feedback amplifiers, stray capacitance from the inverting input (pin 12) to ground or to the output (pin 13) increases peaking in the AC response. For optimum performance, place R_f and R_g as close to the FHP3194 as possible. Small-size surface-mount resistors are recommended.

Avoid the use of vias near the device; vias add unwanted inductance.

If traces of greater than one inch are required, use stripline or microstrip techniques designed with characteristic impedances of 50Ω or 75Ω that are properly terminated with impedance-matching elements at each end.

Refer to the evaluation board layouts for more information.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

| Evaluation Board | Products |
|------------------|----------------|
| KEB022 | FHP3194IM14X |
| KEB025 | FHP3194IMTC14X |

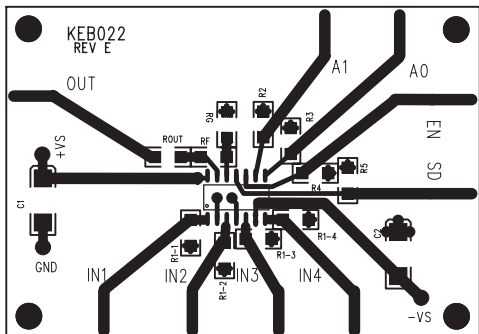


Figure 36. KEB022 Top-Side

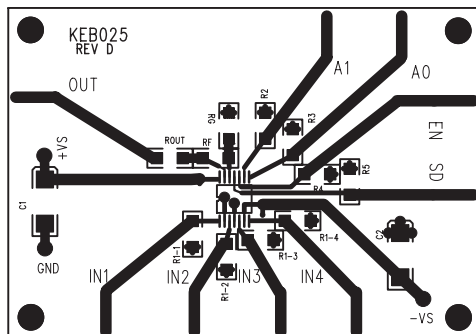


Figure 38. KEB025 Top-Side

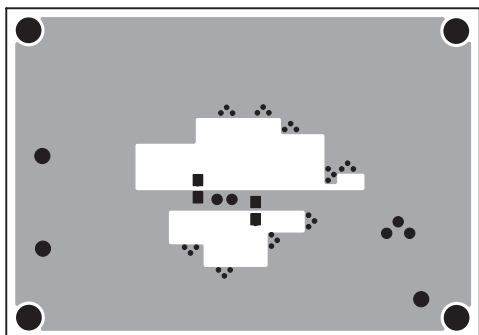


Figure 37. KEB022 Bottom-Side

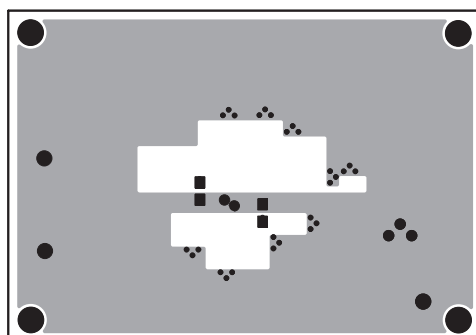
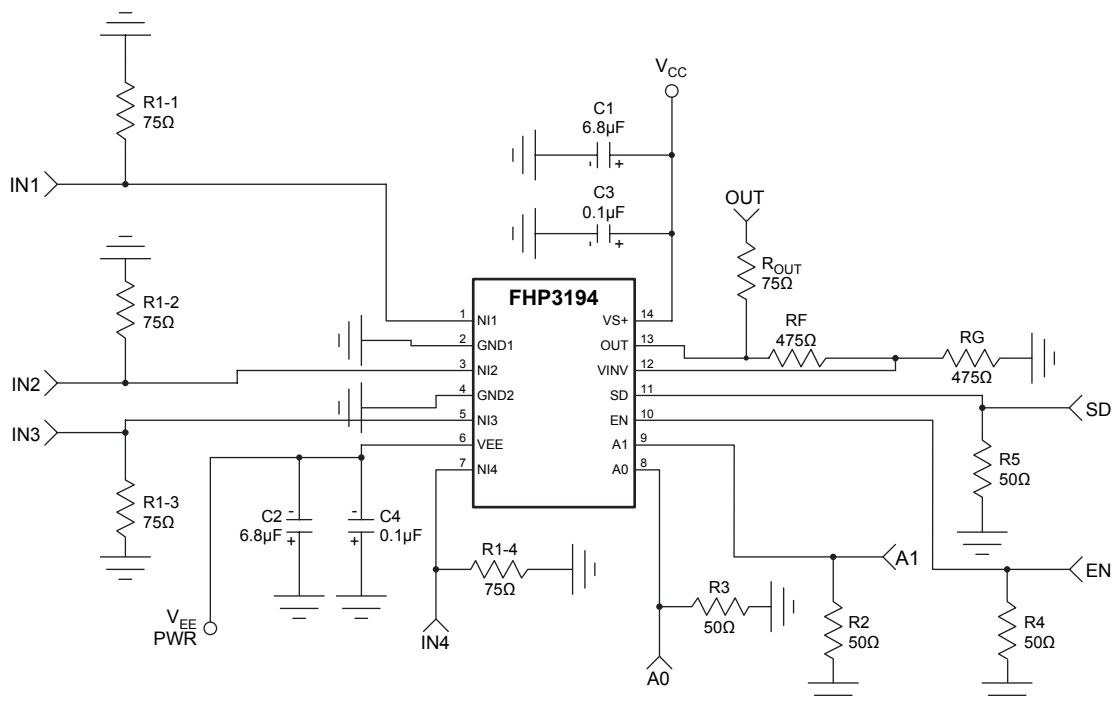


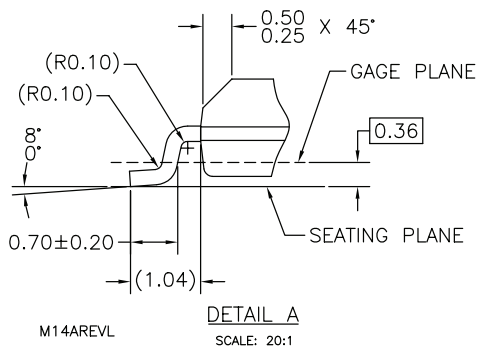
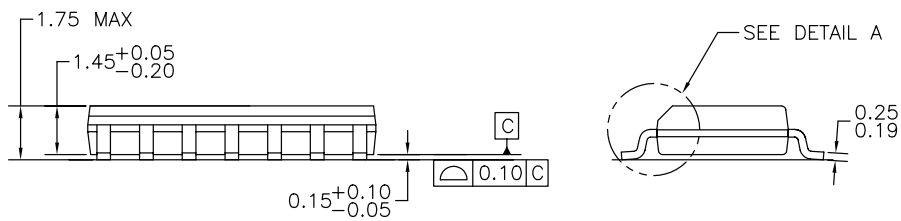
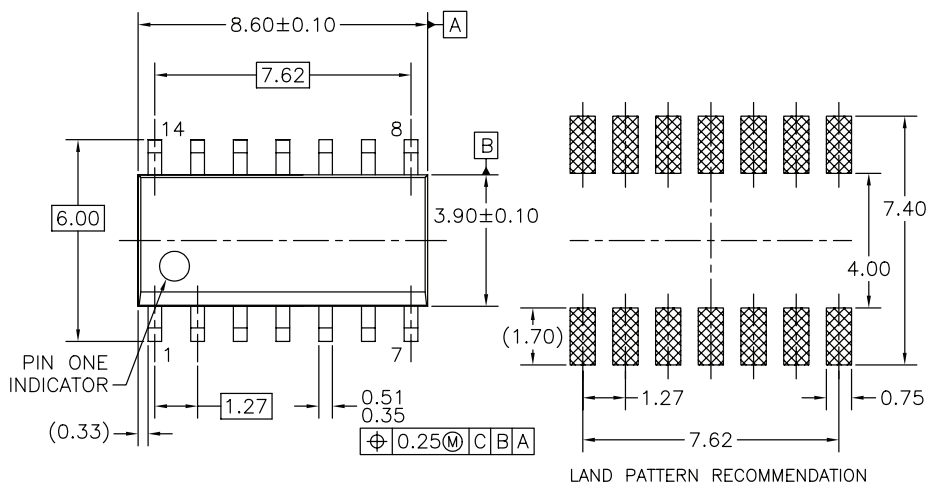
Figure 39. KEB025 Bottom-Side



*Choose R1-1, R1-2, R1-3, R1-4, and ROUT for proper impedance matching. R2, R3, R4, and R5 are optional.

Figure 40. FHP3194 Schematic Diagram

Mechanical Dimensions



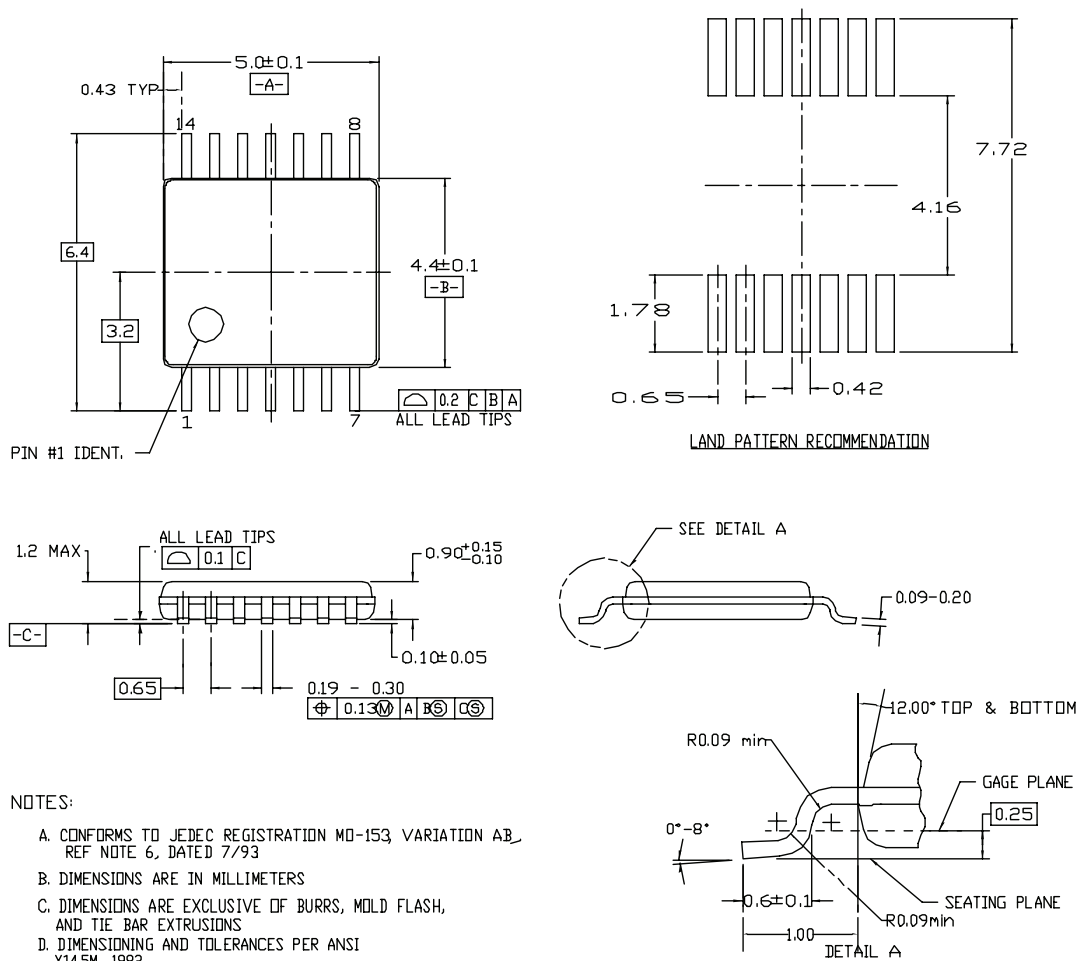
- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C, DATED MAY 1990.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.

M14AREVL

DETAIL A
SCALE: 20:1

Figure 41. SOIC-14 Package

Mechanical Dimensions



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD

Figure 42. TSSOP-14 Package

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| FAST _r ™ | MicroPak™ | QT Optoelectronics™ | TinyPWM™ | |
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| | MSXPro™ | RapidConnect™ | TINYOPTO™ | |
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