FAIRCHILD SEMICONDUCTOR®

February 2007

FHP3131
0.4mA, 2.5V to 12V, 70MHz Rail-to-Rail Amplifier

Features at +5V

- 0.4mA supply current
- 70MHz bandwidth at unity gain
- Power down to 30µA
- Output voltage range at R_L = 1kΩ : 0.07V to 4.8V
- Input extends below negative rail: -0.3V to 4V
- 50V/µs slew rate
- 12nV/Hz input voltage noise
- Small SOT23-6 and MicroPak™ -6 package options
- Fully specified at +2.7V, +5V, and ±5V supplies

Applications

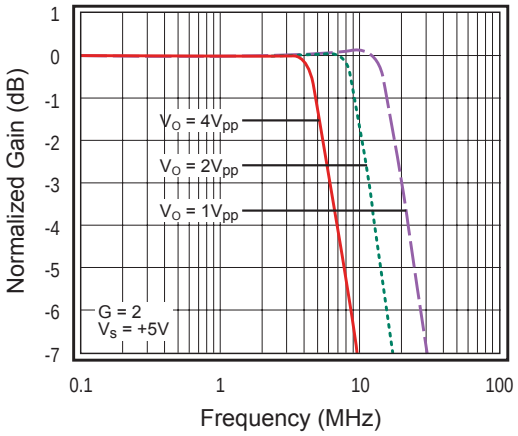
- Portable/battery-powered applications
- A/D buffer
- Active filters
- Portable test instruments
- Set-top box
- HDTV
- DVD players and recorders
- Coaxial cable drivers
- Video driver

Description

The FHP3131 is a high-performance, voltage-feedback amplifier that consumes only 0.4mA of supply current while providing 70MHz of bandwidth and 50V/µs slew rate. The FHP3131 is designed to operate from 2.5V to 12V (±6V) supplies. The common mode voltage range extends below the negative rail and the output provides rail-to-rail performance.

The FHP3131 is fabricated on a complementary bipolar process. The combination of low power, rail-to-rail performance, low voltage operation, and tiny package options make this amplifier well suited for use in many general-purpose, high-speed applications.

For power sensitive applications, the FHP3131 offers unparalleled dynamic performance. It also offers a shut-down feature to lower the supply current draw below 30µA. The FHP3131 is available in space-saving 6-lead SOT23 or MicroPak™ packages and operates from -40°C to +85°C.



Ordering Information

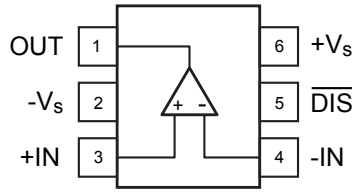
Part Number	Package	Pb-Free	Operating Temperature Range	Packaging Method
FHP3131IS6X	SOT23-6	Yes	-40°C to +85°C	Reel
FHP3131IL6X	MicroPak-6	Yes	-40°C to +85°C	Reel

Moisture sensitivity level for all parts is MSL-1.

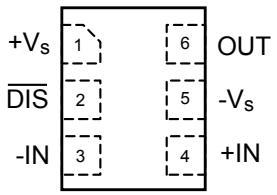
MicroPak™ is a trademark of Fairchild Semiconductor Corporation.

Pin Configurations

FHP3131
SOT23



FHP3131
MicroPak™



Top View

Pin Assignments

Pin # SOT/MicroPak	Name	Description
1/6	OUT	Output
2/5	$-V_S$	Negative supply
3/4	+IN	Positive input
4/3	-IN	Negative input
5/2	$\overline{DIS}$	Leave floating or pull high to enable. Pull low to disable.
6/1	$+V_S$	Positive supply

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Parameter	Min.	Max.	Unit
Supply Voltage	0	12.6	V
Input Voltage Range	$-V_S$-0.5V	$+V_S$+0.5V	V

Reliability Information

Parameter		Min.	Typ.	Max.	Unit
Junction Temperature				150	°C
Storage Temperature Range		-65		150	°C
Reflow Temperature (Soldering)				260	°C
Package Thermal Resistance	6-Lead SOT23(1)		302		°C/W
	6-Lead MicroPak™(1)		440		°C/W

Notes:
1. Package thermal resistance (θ_{JA}), JEDEC standard, multi-layer test boards, still air.

ESD Protection

Product	FHP3131
Human Body Model (HBM)	4kV
Charged Device Model (CDM)	2kV

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range	-40		+85	°C
Supply Voltage Range	2.5		12	V

Electrical Characteristics at +2.7V

T_A = 25°C, V_s = 2.7V, R_f = 1kΩ, R_L = 1kΩ to V_s/2, G = 2, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency Domain Response						
UGBW	-3dB Bandwidth	G = +1, V_{OUT} = 0.2V_{pp}		70		MHz
BW_{ss}	Small Signal Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		28		MHz
BW_{Ls}	Large Signal Bandwidth	G = +2, V_{OUT} = 2V_{pp}		10		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 0.2V step		11		ns
t_S	Settling Time to 0.1%	V_{OUT} = 1V step		85		ns
OS	Overshoot	V_{OUT} = 1V step		4		%
SR	Slew Rate	V_{OUT} = 2V step, G = -1		45		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT} = 1V_{pp}, 1MHz		67		dBc
HD3	3rd Harmonic Distortion	V_{OUT} = 1V_{pp}, 1MHz		65		dBc
THD	Total Harmonic Distortion	V_{OUT} = 1V_{pp}, 1MHz		63		dB
e_n	Input Voltage Noise	> 100kHz		12		nV/√Hz
DC Performance						
V_{IO}	Input Offset Voltage			1		mV
dV_{IO}	Average Drift			10		µV/°C
I_b	Input Bias Current			1.4		µA
dI_b	Average Drift			3.5		nA/°C
I_{IO}	Input Offset Current			30		nA
PSRR	Power Supply Rejection Ratio	DC		100		dB
A_{OL}	Open-Loop Gain	DC		95		dB
I_S	Supply Current			0.4		mA
Disable Characteristics						
T_{ON} / T_{OFF}	Turn-On/Turn-Off Time			0.4/2.2		µs
OFF_{ISO}	Off Isolation	5MHz, R_L = 100Ω		65		dB
V_{OFF}	Power Down Input Voltage	Disabled if pin is grounded or pulled below V_{OFF}		V_s-1.75		V
V_{ON}	Enable Input Voltage	Enabled if pin is floating or pulled above V_{ON}		V_s-1.1		V
I_{SD}	Disabled Supply Current	$\overline{DIS}$ pin grounded		15		µA
Input Characteristics						
R_{IN}	Input Resistance			14		MΩ
C_{IN}	Input Capacitance			1.1		pF
CMIR	Input Common Mode V Range			-0.3 to 1.7		V
CMRR	Common Mode Rejection Ratio	DC, V_{CM} = 0V to V_s - 1.5		95		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 1kΩ to V_s/2, G = -1		0.05 to 2.59		V
		R_L = 150Ω to V_s/2, G = -1		0.15 to 2.3		V
I_{OUT}	Linear Output Current			+20,-11		mA
I_{SC}	Short-Circuit Output Current	V_{OUT} = V_s/2		+25,-14		mA

Electrical Characteristics at +5V

T_A = 25°C, V_s = 5V, R_f = 1kΩ, R_L = 1kΩ to V_s/2, G = 2, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency Domain Response						
UGBW	-3dB Bandwidth	G = +1, V_{OUT} = 0.2V_{pp}		70		MHz
BW_{ss}	Small Signal Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		28		MHz
BW_{Ls}	Large Signal Bandwidth	G = +2, V_{OUT} = 2V_{pp}		11		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 0.2V step		11		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		80		ns
OS	Overshoot	V_{OUT} = 0.2V step		2		%
SR	Slew Rate	V_{OUT} = 2V step, G = -1		50		V/µs
Distortion / Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT} = 2V_{pp}, 1MHz		64		dBc
HD3	3rd Harmonic Distortion	V_{OUT} = 2V_{pp}, 1MHz		58		dBc
THD	Total Harmonic Distortion	V_{OUT} = 2V_{pp}, 1MHz		57		dB
e_n	Input Voltage Noise	> 100kHz		12		nV/√Hz
DG	Differential Gain	NTSC (3.58MHz); AC-coupled		0.04		%
DP	Differential Phase	NTSC (3.58MHz); AC-coupled		0.13		°
DC Performance						
V_{IO}	Input Offset Voltage(1)		-5	1	5	mV
dV_{IO}	Average Drift			10		µV/°C
I_b	Input Bias Current(1)		-3.5	1.4	3.5	µA
dI_b	Average Drift			3.5		nA/°C
I_{IO}	Input Offset Current(1)			30	350	nA
PSRR	Power Supply Rejection Ratio(1)	DC	70	100		dB
A_{OL}	Open-Loop Gain(1)	DC	65	100		dB
I_S	Supply Current(1)			0.40	0.62	mA
Disable Characteristics						
T_{ON} / T_{OFF}	Turn-On/Turn-Off Time			0.5/1.9		µs
OFF_{ISO}	Off Isolation	5MHz, R_L = 100Ω		65		dB
V_{OFF}	Power Down Input Voltage(1)	Disabled if pin is grounded or pulled below V_{OFF}			V_s-1.9	V
V_{ON}	Enable Input Voltage(1)	Enabled if pin is floating or pulled above V_{ON}	V_s-1.2			V
I_{SD}	Disabled Supply Current(1)	$\overline{DIS}$ pin grounded		30	45	µA
Input Characteristics						
R_{IN}	Input Resistance			20		MΩ
C_{IN}	Input Capacitance			1		pF
CMIR	Input Common Mode V Range			-0.3 to 4		V
CMRR	Common Mode Rejection Ratio(1)	DC, V_{CM} = 0V to V_s - 1.5	78	100		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 1kΩ to V_s/2(1)	0.2	0.07 to 4.8	4.65	V
		R_L = 150Ω to V_s/2		0.25 to 4.4		V
I_{OUT}	Linear Output Current			+30,-18		mA
I_{SC}	Short-Circuit Output Current	V_{OUT} = V_s/2		+35,-24		mA

Note:
1. 100% tested at 25°C.

Electrical Characteristics at ±5V

T_A = 25°C, V_s = ±5V, R_f = 1kΩ, R_L = 1kΩ to GND, G = 2, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency Domain Response						
UGBW	-3dB Bandwidth	G = +1, V_{OUT} = 0.2V_{pp}		70		MHz
BW_{ss}	Small Singal Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		28		MHz
BWLs	Large Signal Bandwidth	G = +2, V_{OUT} = 2V_{pp}		11		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 0.2V step		11		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		80		ns
OS	Overshoot	V_{OUT} = 0.2V step		2		%
SR	Slew Rate	V_{OUT} = 2V step, G = -1		45		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		64		dBc
HD3	3rd Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		58		dBc
THD	Total Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		57		dB
e_n	Input Voltage Noise	> 100kHz		12		nV/√Hz
DG	Differential Gain	NTSC (3.58MHz); AC-coupled		0.08		%
DP	Differential Phase	NTSC (3.58MHz); AC-coupled		0.16		°
DC Performance						
V_{IO}	Input Offset Voltage			1		mV
dV_{IO}	Average Drift			10		µV/°C
I_b	Input Bias Current			1.4		µA
dI_b	Average Drift			3.5		nA/°C
I_{IO}	Input Offset Current			30		nA
PSRR	Power Supply Rejection Ratio	DC		100		dB
A_{OL}	Open-Loop Gain	DC		100		dB
I_S	Supply Current per Amplifier			0.4		mA
Disable Characteristics						
T_{ON} / T_{OFF}	Turn-On/Turn-Off Time			0.5/2		µs
OFF_{ISO}	Off Isolation	5MHz, R_L = 100Ω		65		dB
V_{OFF}	Power Down Input Voltage	Disabled if pin is grounded or pulled below V_{OFF}		V_s-2.9		V
V_{ON}	Enable Input Voltage	Enabled if pin is floating or pulled above V_{ON}		V_s-1.4		V
I_{SD}	Disabled Supply Current	$\overline{DIS}$ pin grounded		45		µA
Input Characteristics						
R_{IN}	Input Resistance			25		MΩ
C_{IN}	Input Capacitance			1		pF
CMIR	Input Common Mode V Range			-5.3 to 4		V
CMRR	Common Mode Rejection Ratio	DC, V_{CM} = -5V to 3.5V		100		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 1kΩ		±4.8		V
		R_L = 150Ω		+2.9,-4.23		V
I_{OUT}	Linear Output Current			+35,-25		mA
I_{SC}	Short-Circuit Output Current	V_{OUT} = 0V		+43,-33		mA

Typical Performance Characteristics

T_A = 25°C, R_L = 1kΩ to V_s/2 for V_s = 5V and 2.7V, R_L = 1kΩ to GND for V_s = ±5V, G = 2 and R_f = R_g = 1kΩ, unless otherwise noted.

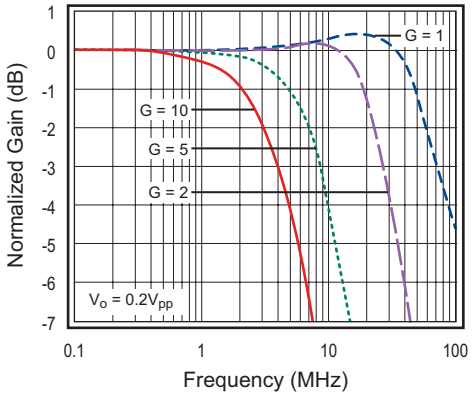


Figure 1. Non-Inverting Freq. Response (±5V)

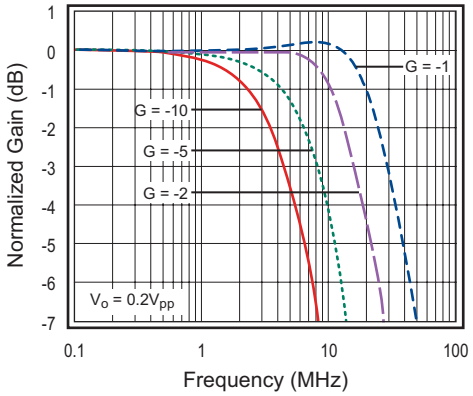


Figure 2. Inverting Freq. Response (±5V)

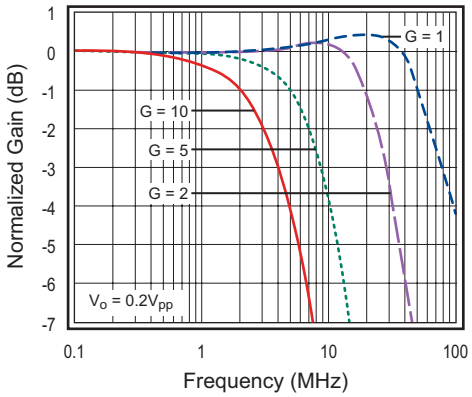


Figure 3. Non-Inverting Freq. Response (+5V)

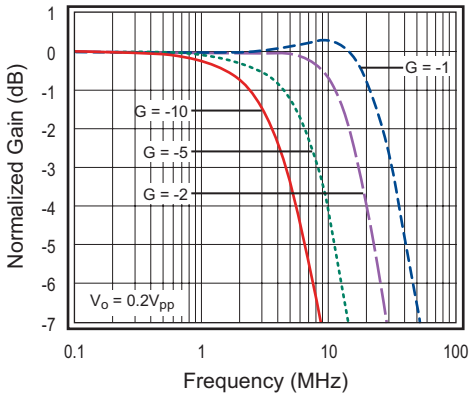


Figure 4. Inverting Freq. Response (+5V)

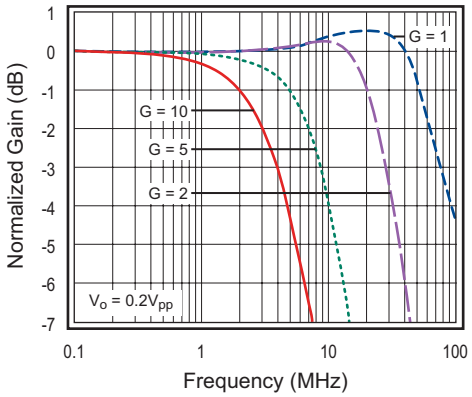


Figure 5. Non-Inverting Freq. Response (+2.7V)

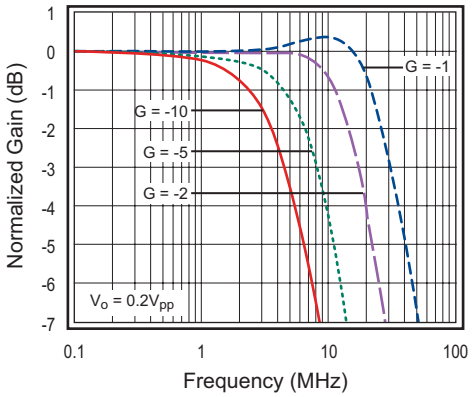


Figure 6. Inverting Freq. Response (+2.7V)

Typical Performance Characteristics - Continued

T_A = 25°C, R_L = 1kΩ to V_s/2 for V_s = 5V and 2.7V, R_L = 1kΩ to GND for V_s = ±5V, G = 2 and R_f = R_g = 1kΩ, unless otherwise noted.

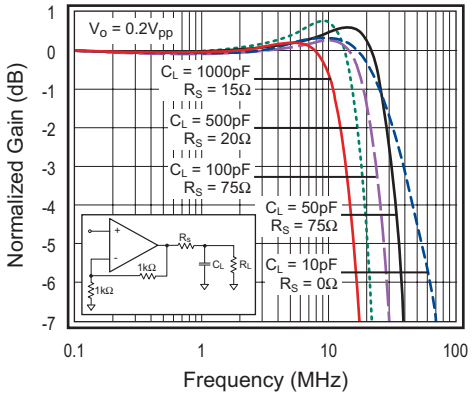


Figure 7. Frequency Response vs. C_L (+5V)

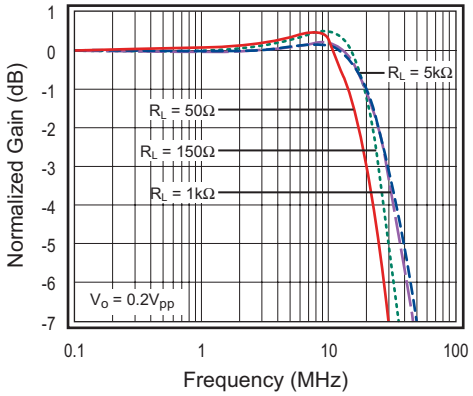


Figure 8. Frequency Response vs. R_L (+5V)

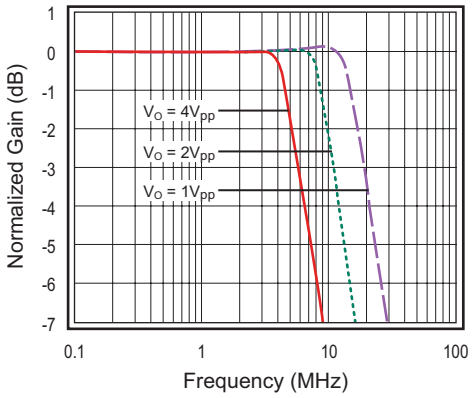


Figure 9. Large Signal Freq. Response (±5V)

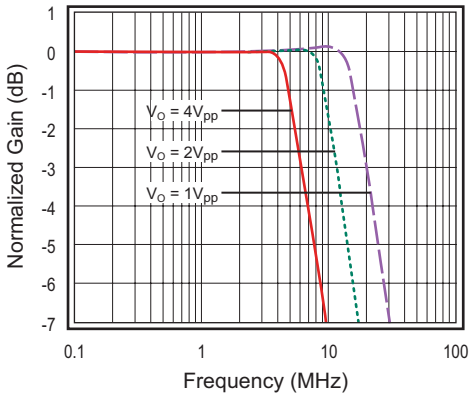


Figure 10. Large Signal Freq. Response (+5V)

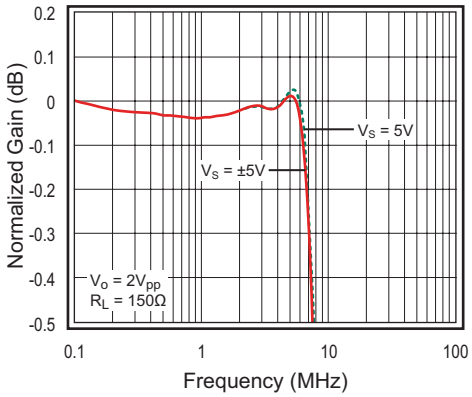


Figure 11. Gain Flatness vs. Frequency

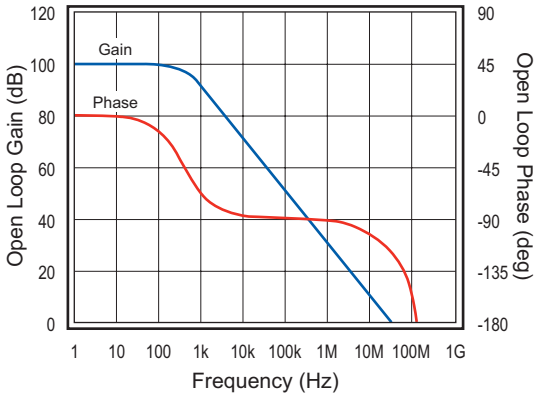


Figure 12. Open-Loop Gain and Phase (+5V)

Typical Performance Characteristics - Continued

T_A = 25°C, R_L = 1kΩ to V_s/2 for V_s = 5V and 2.7V, R_L = 1kΩ to GND for V_s = ±5V, G = 2 and R_f = R_g = 1kΩ, unless otherwise noted.

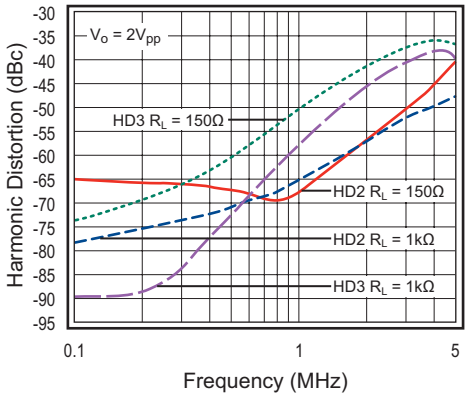


Figure 13. HD vs. Frequency (±5V)

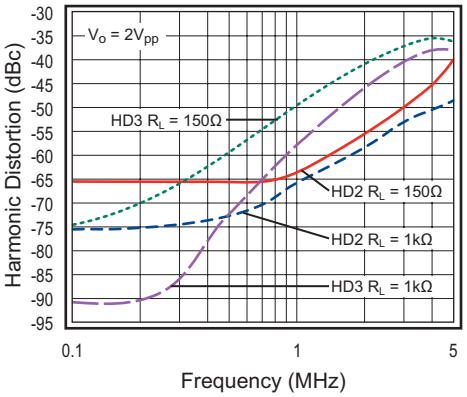


Figure 14. HD vs. Frequency (+5V)

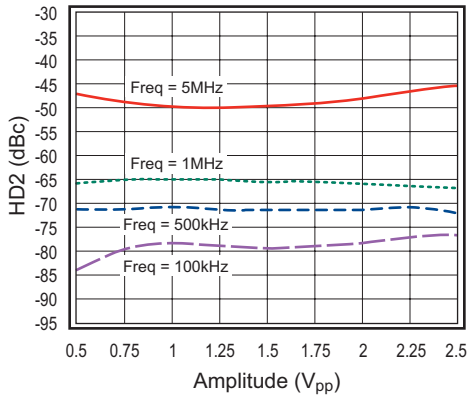


Figure 15. HD2 vs. V_{OUT} (±5V)

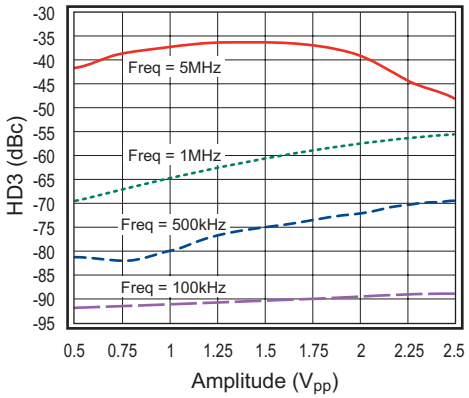


Figure 16. HD3 vs. V_{OUT} (±5V)

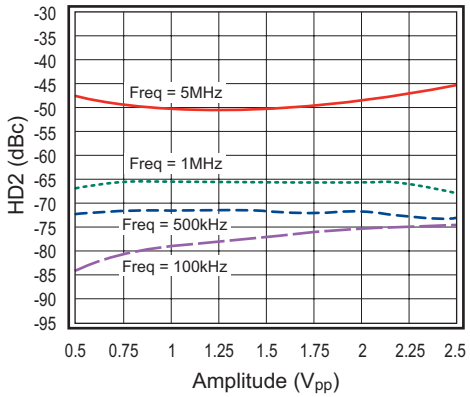


Figure 17. HD2 vs. V_{OUT} (+5V)

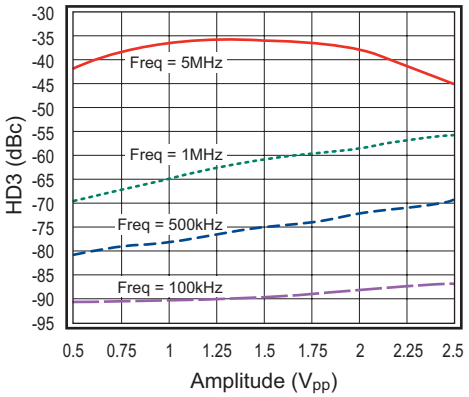


Figure 18. HD3 vs. V_{OUT} (+5V)

Typical Performance Characteristics - Continued

T_A = 25°C, R_L = 1kΩ to V_s/2 for V_s = 5V and 2.7V, R_L = 1kΩ to GND for V_s = ±5V, G = 2, and R_f = R_g = 1kΩ, unless otherwise noted.

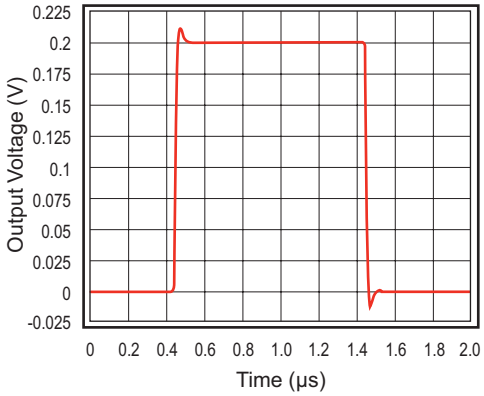


Figure 19. Small Signal Pulse Response (+2.7V)

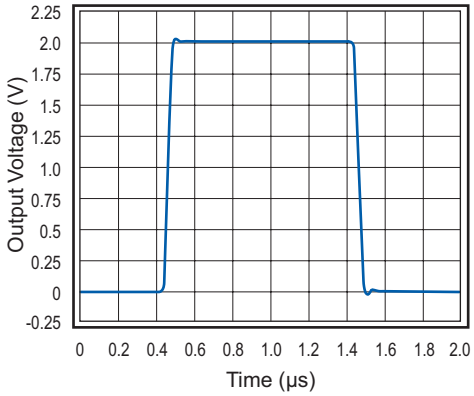


Figure 20. Large Signal Pulse Response (+2.7V)

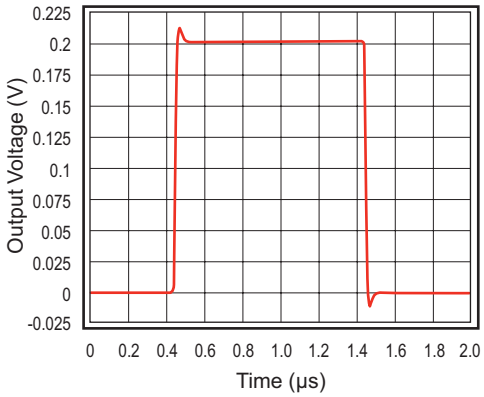


Figure 21. Small Signal Pulse Response (+5V)

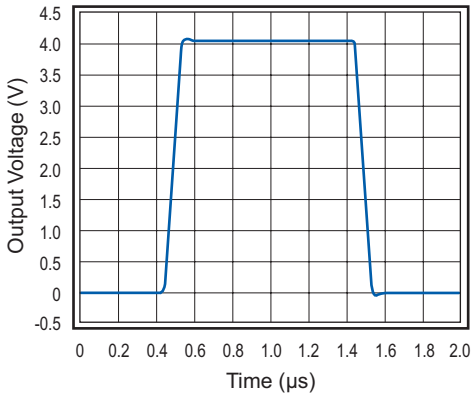


Figure 22. Large Signal Pulse Response (+5V)

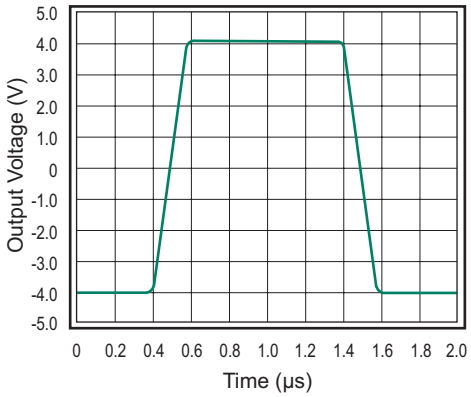


Figure 23. Large Signal Pulse Response (±5V)

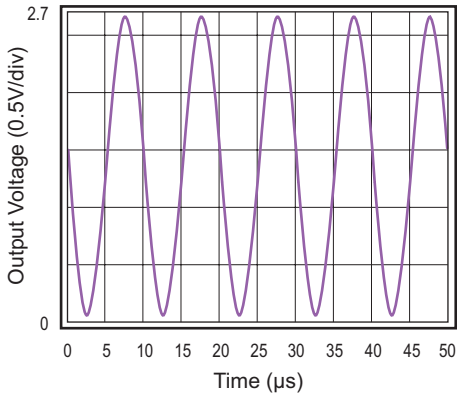


Figure 24. Output Swing: V_S = +2.7V; G = 1

Typical Performance Characteristics - Continued

T_A = 25°C, R_L = 1kΩ to V_s/2 for V_s = 5V and 2.7V, R_L = 1kΩ to GND for V_s = ±5V, G = 2, and R_f = R_g = 1kΩ, unless otherwise noted.

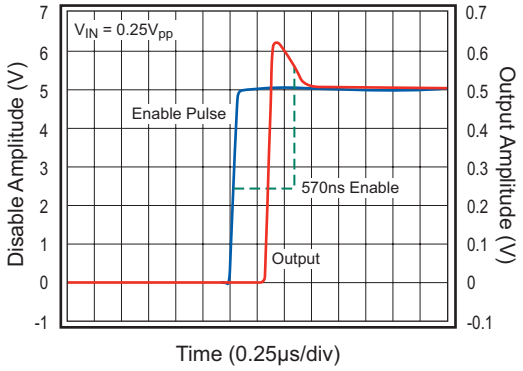


Figure 25. Enable Time to 10% Settling (+5V)

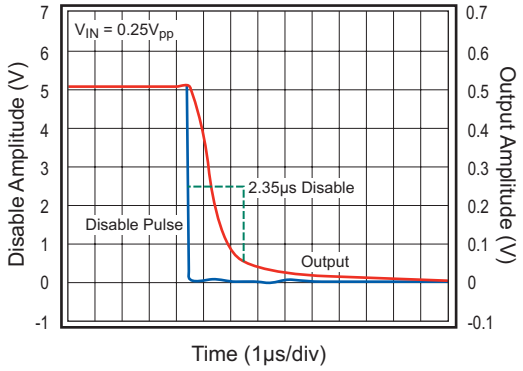


Figure 26. Disable Time to 10% Settling (+5V)

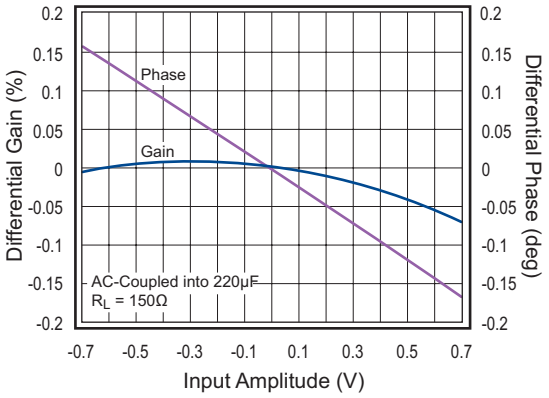


Figure 27. Differential Gain and Phase (±5V)

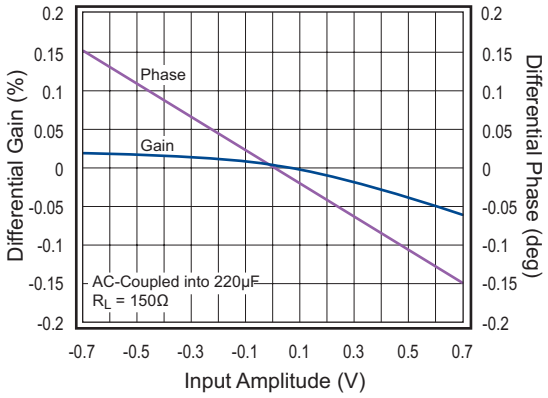


Figure 28. Differential Gain and Phase (±2.5V)

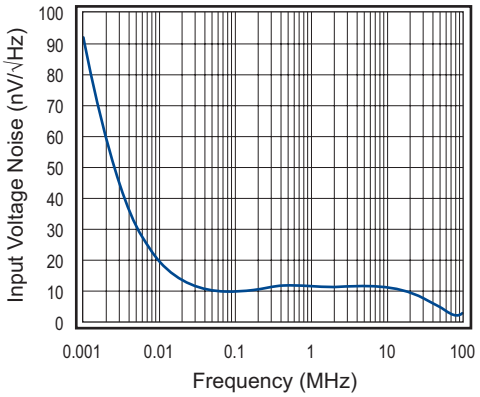


Figure 29. Input Voltage Noise (+5V)

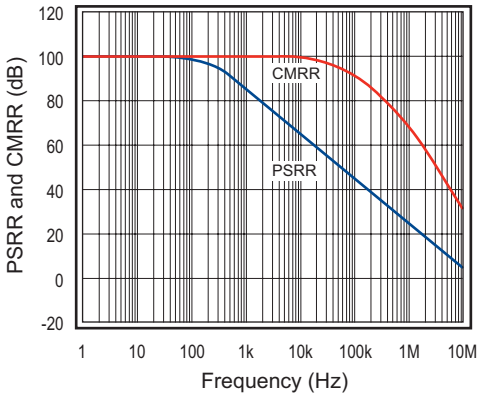


Figure 30. PSRR and CMRR (+5V)

Application Information

Driving Capacitive Loads

The *Frequency Response vs. C_L* Figure 7 on page 8, illustrates the response of the FHP3131. A small series resistance (R_s) at the output of the amplifier, illustrated in Figure 31, improves stability and settling performance. R_s values in the *Frequency Response vs. C_L* figure were chosen to achieve maximum bandwidth with less than 1dB of peaking. For maximum flatness, use a larger R_s.

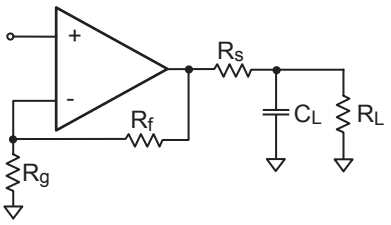


Figure 31. Typical Topology for Driving Capactive Loads

Enable/Disable Function

The FAN3131 offers an active-low disable pin that can be used to lower its supply current. Leave the pin floating to enable the part. Pull the disable pin to the negative supply (which is ground in a single-supply application) to disable the output. V_{ON} and V_{OFF} thresholds are listed in the table below. During the disable condition, the nominal supply current drops to below 33µA and the output is at high impedance with about 2.8pF capacitance.

At 2.7V		At 5V		At ±5V	
V_{ON}	V_{OFF}	V_{ON}	V_{OFF}	V_{ON}	V_{OFF}
V_s-1.1	V_s-1.75	V_s-1.2	V_s-1.9	V_s-1.4	V_s-2.9

±5V Drive Capability

Figure 32 illustrates the drive capability of the FHP3131 during ±5V supply voltage operation. The two examples below demonstrate the use of this graph:

1. To adequately drive $2V_{pp}$ into a 150Ω ground-centered load, the FHP3131 must supply ±6.67mA of output current. From the graph, the points created by (-6.7mA, -1V) and (+6.7mA, +1V) both lie within the linear region of the curve. So, the FHP3131 can drive $2V_{pp}$ into a 150Ω ground-centered load.
2. To adequately drive $5V_{pp}$ into a 100Ω load, the FHP3131 must supply ±25mA of output current. From the graph, the point created by (+25mA, +2.5V) lies within the linear region of the curve; however, the point created by (-25mA, -2.5V) does not. So, the FHP3131 is not capable of driving $5V_{pp}$ into a 100Ω ground-centered load at ±5V.

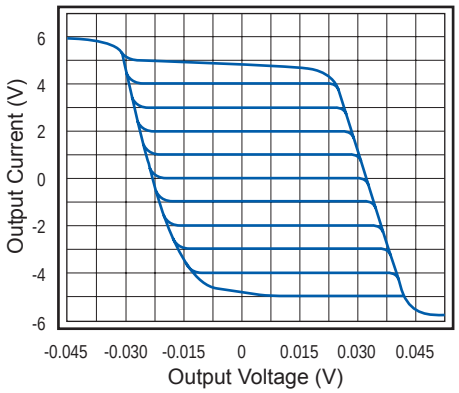


Figure 32. Output Current vs. Output Voltage

Power Dissipation

The maximum internal power dissipation allowed is directly related to the maximum junction temperature. If the maximum junction temperature exceeds 150°C for an extended time, device failure may occur. While the FHP3131 is short-circuit protected, this may not guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. RMS Power Dissipation can be calculated using the following equation:

Power Dissipation =

$$I_s * (V_{s+} - V_{s-}) + (V_{s+} - V_{OUT(RMS)}) * I_{OUT(RMS)} \qquad \text{EQ. 1}$$

where I_s is the supply current, V_{s+} is the positive supply pin voltage, V_{s-} is the negative supply pin voltage, $V_{OUT(RMS)}$ is the RMS output voltage, and $I_{OUT(RMS)}$ is the RMS output current delivered to the load. Follow the maximum power derating curves shown in Figure 33 below to ensure proper operation.

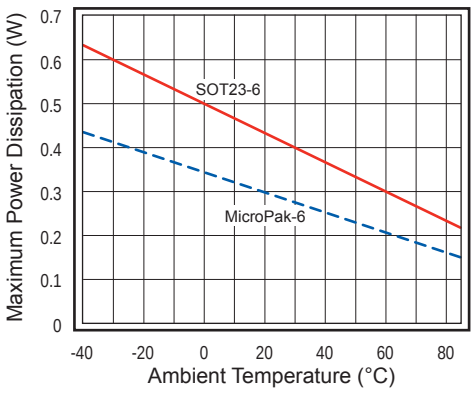


Figure 33. Maximum Power Derating

Overdrive Recovery

For an amplifier, an overdrive condition occurs when the output and/or input ranges are exceeded. The recovery time varies based on whether the input or output is overdriven and by how much the ranges are exceeded. The FHP3131 typically recovers in less than 25ns from an overdrive condition. Figure 34 shows the FHP3131 in an overdriven condition.

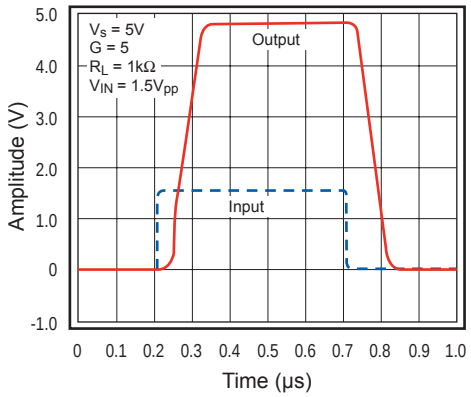


Figure 34. Overdrive Recovery

Layout Considerations

General layout and supply bypassing play major roles in high-frequency performance. Fairchild has evaluation boards to guide high-frequency layout and aid device testing and characterization. Follow the guidelines below as a basis for high-frequency layout:

- Include 6.8µF and 0.01µF ceramic capacitors.
- Place the 6.8µF capacitor within 0.75 inches of the power pin.
- Place the 0.01µF capacitor within 0.1 inches of the power pin.
- Remove the ground plane under and around the part, especially near the input and output pins, to reduce parasitic capacitance.
- Minimize all trace lengths to reduce series inductances.

Refer to the evaluation board layouts shown in Figures 36-39 for more information.

Evaluation Board Information

The following evaluation boards are available to aid testing and layout of these devices:

Evaluation Board	Products
KEB002	FHP3131IS6X
KEB029	FHP3131IL6X

Evaluation Board Schematic

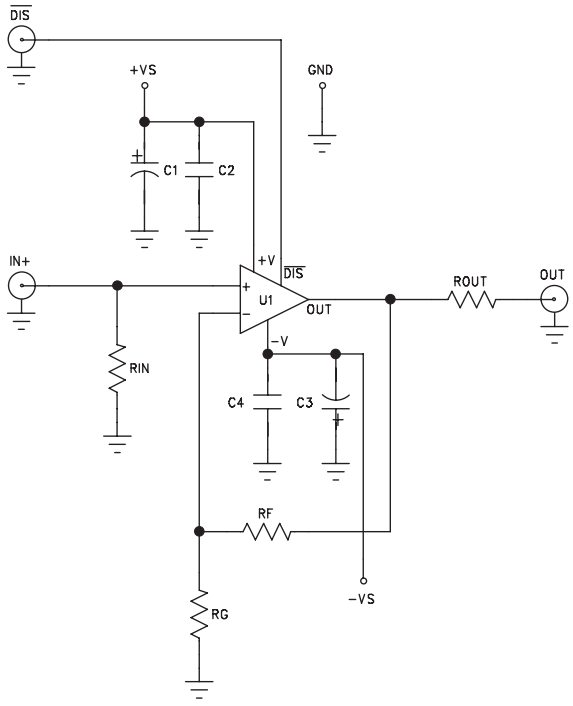


Figure 35. KEB002/KEB029 Schematic

Evaluation Board Layouts

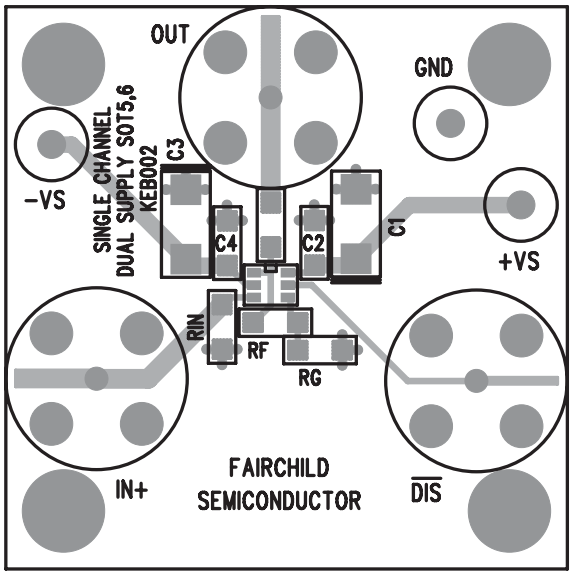


Figure 36. KEB002 (Top-side)

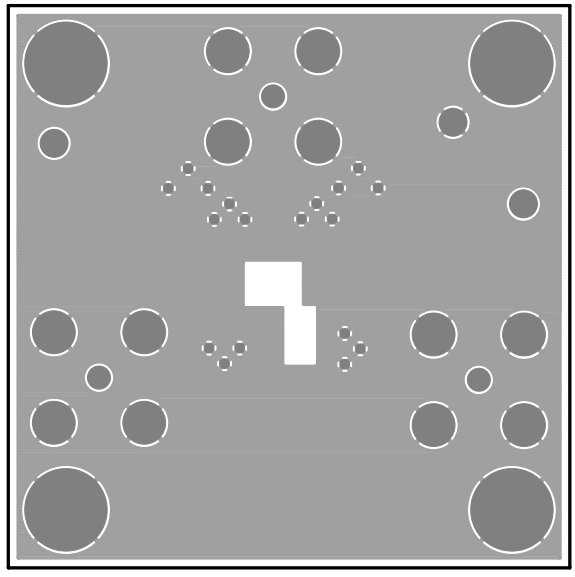


Figure 37. KEB002 (Bottom-side)

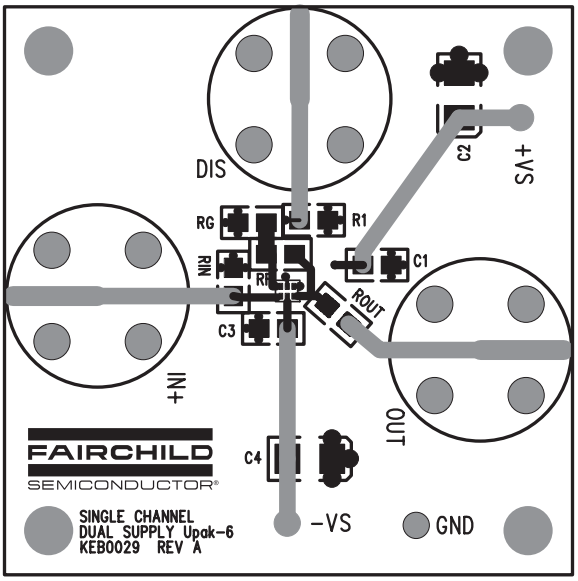


Figure 38. KEB029 (Top-side)

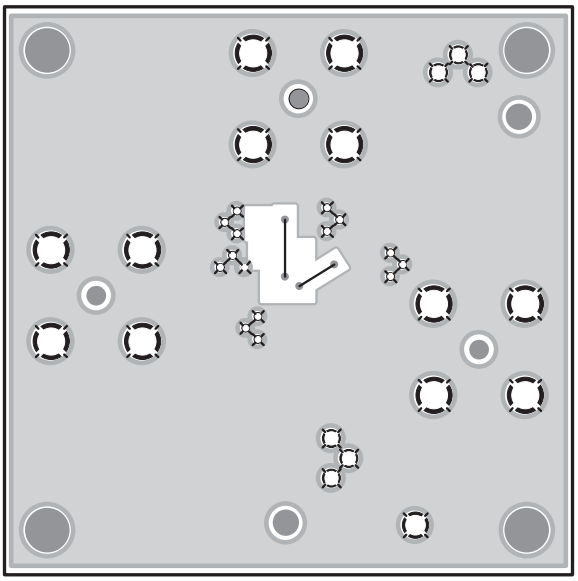
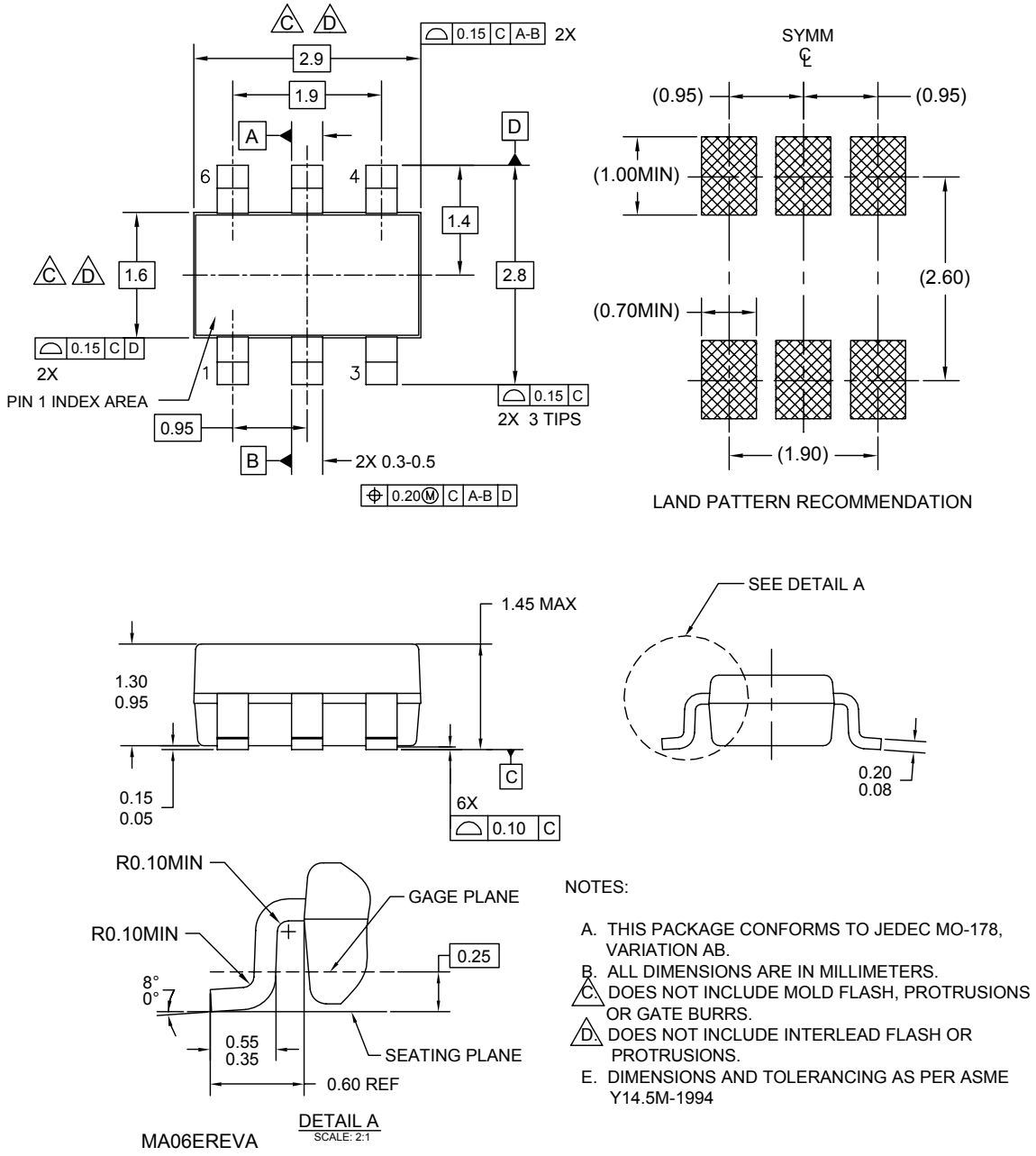


Figure 39. KEB029 (Bottom-side)

Mechanical Dimensions

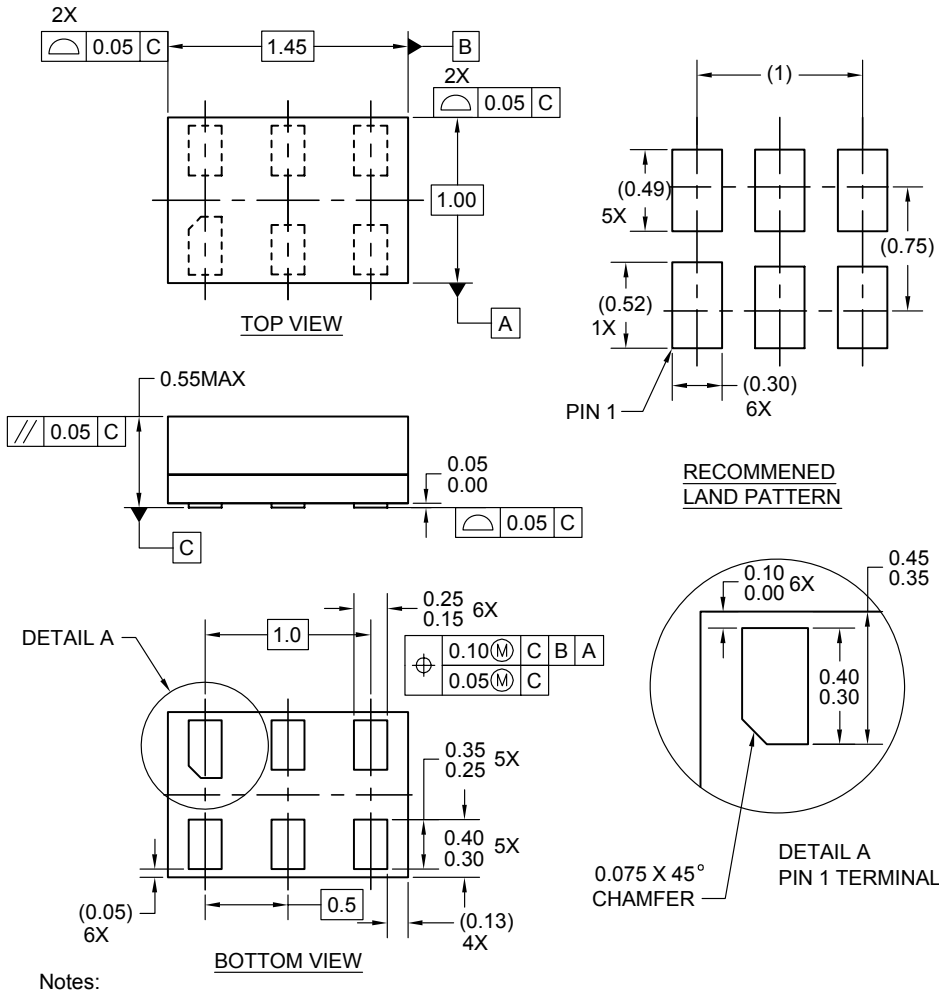


NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC MO-178, VARIATION AB.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
D. DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
E. DIMENSIONS AND TOLERANCING AS PER ASME Y14.5M-1994

Figure 40. 6-Lead SOT23 Package

Mechanical Dimensions



Notes:

1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06AREVC

Figure 41. 6-Lead MicroPak™ Package

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