FAIRCHILD SEMICONDUCTOR®

March 2008

FDZ4670S

N-Channel PowerTrench® SyncFET ™

30V, 25A, 2.4mΩ

Features

- Max $r_{DS(on)}$ = 2.4mΩ at V_{GS} = 10V, I_D = 25A
- Max $r_{DS(on)}$ = 4.0mΩ at V_{GS} = 4.5V, I_D = 19A
- Ultra-thin package: less than 0.85mm height when mounted to PCB
- Outstanding thermal transfer characteristics
- Ultra-low gate charge x $r_{DS(on)}$ product
- RoHS Compliant

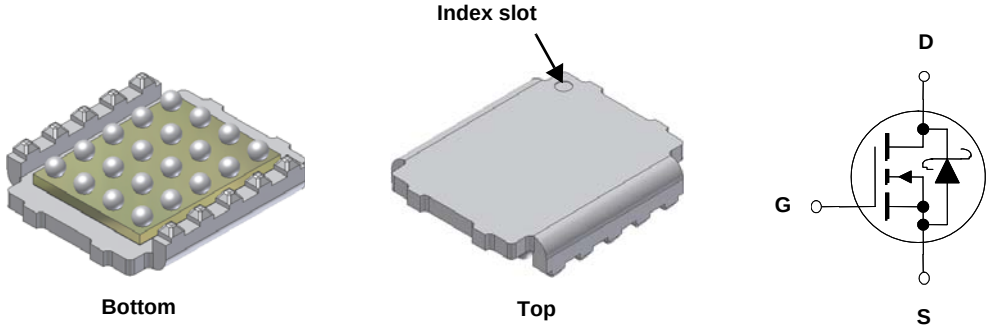
General Description

Combining Fairchild's 30V PowerTrench® process with state-of-the-art BGA packaging, the FDZ4670S minimizes both PCB space and $r_{DS(on)}$. This BGA MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, high current handling capacity, ultra-low profile packaging, low gate charge and low $r_{DS(on)}$ incorporating SyncFET technology. This device has the added benefit of an efficient monolithic Schottky body diode to reduce Trr and diode forward voltage.

This MOSFET feature faster switching and lower gate charge than other MOSFETs with comparable $r_{DS(on)}$ specifications resulting in DC/DC power supply designs and POL converters with higher overall efficiency.

Applications

- DC - DC Conversion
- POL converters



FLFBGA 3.5X4.0

MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			30	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous	T_A = 25°C	(Note 1a)	25	A
	-Pulsed			107	
P_D	Power Dissipation	T_A = 25°C	(Note 1a)	2.5	W
	Power Dissipation	T_A = 25°C	(Note 1b)	1.25	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		0.85	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	100	

Package Marking and Ordering Information

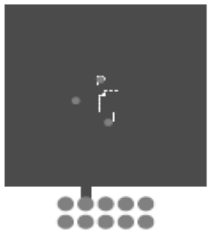
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
4670S	FDZ4670S	FLFBGA 3.5X4.0	13”	12mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 1mA, V_{GS} = 0V	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 1mA, referenced to 25°C		25		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0V, V_{DS} = 24V,			500	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 1mA	1.0	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 1mA, referenced to 25°C		-3.6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 25A		1.7	2.4	mΩ
		V_{GS} = 4.5V, I_D = 19A		2.8	4.0	
		V_{GS} = 10V, I_D = 25A, T_J = 125°C		2.7	3.6	
g_{FS}	Forward Transconductance	V_{DD} = 10V, I_D = 25A		118		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz		2890	3845	pF
C_{oss}	Output Capacitance			1610	2145	pF
C_{rss}	Reverse Transfer Capacitance			160	240	pF
R_g	Gate Resistance	f = 1MHz		1.0		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15V, I_D = 25A, V_{GS} = 10V, R_{GEN} = 6Ω		13	23	ns
t_r	Rise Time			4.5	10	ns
$t_{d(off)}$	Turn-Off Delay Time			31	50	ns
t_f	Fall Time			3.1	10	ns
Q_g	Total Gate Charge	V_{GS} = 10V, V_{DD} = 15V, I_D = 25A		49	69	nC
Q_{gs}	Gate to Source Charge			9.1		nC
Q_{gd}	Gate to Drain “Miller” Charge			7.6		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 3.5A (Note 2)		0.4	0.7	V
t_{rr}	Reverse Recovery Time	I_F = 25A, di/dt = 300A/μs		37		ns
Q_{rr}	Reverse Recovery Charge			46		nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50°C/W when mounted on a 1in^2 pad of 2 oz copper.

b. 100°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

Typical Characteristics T_J = 25°C unless otherwise noted

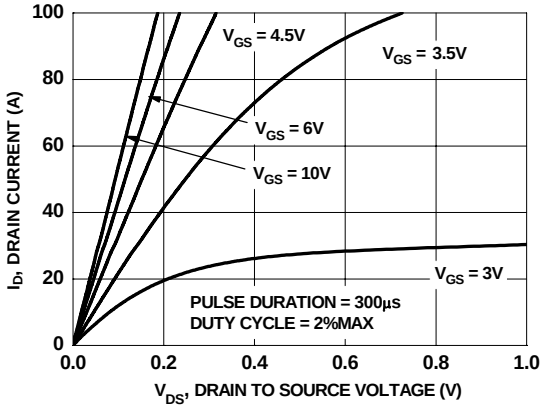


Figure 1. On-Region Characteristics

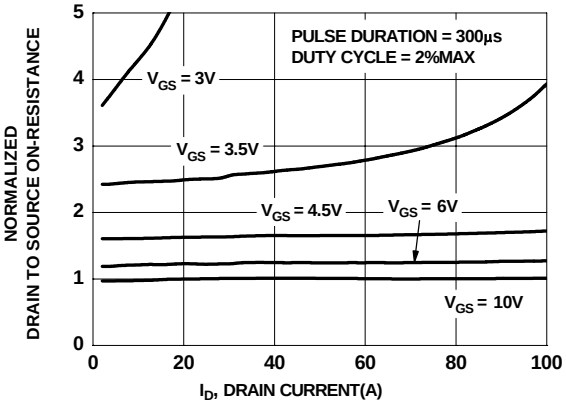


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

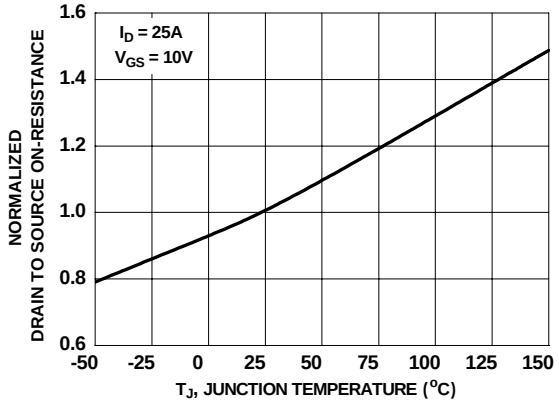


Figure 3. Normalized On-Resistance vs Junction Temperature

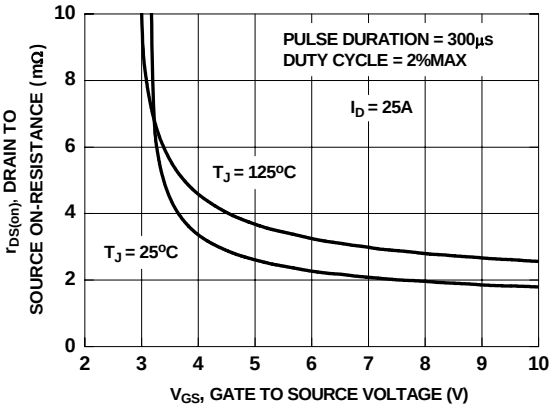


Figure 4. On-Resistance vs Gate to Source Voltage

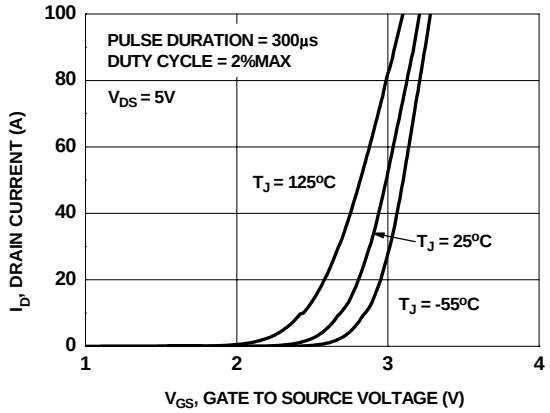


Figure 5. Transfer Characteristics

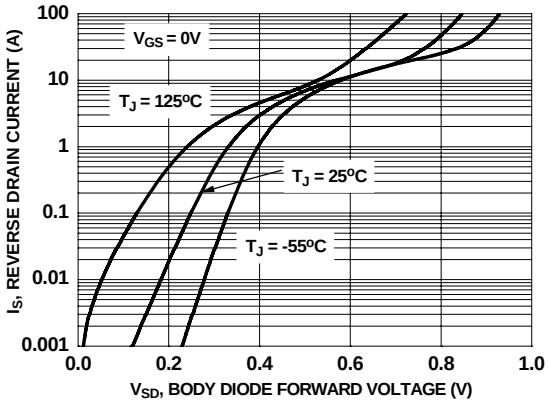


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

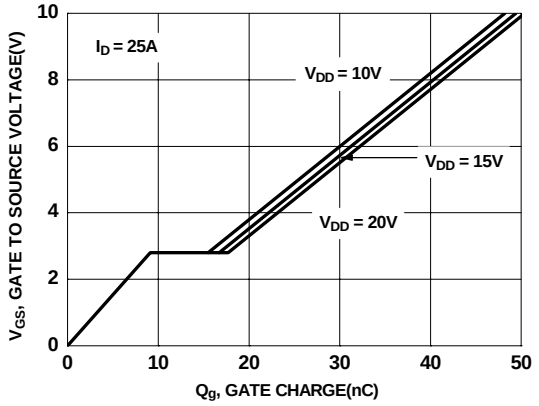


Figure 7. Gate Charge Characteristics

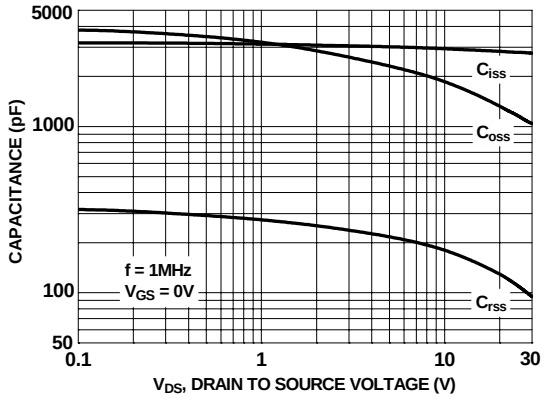


Figure 8. Capacitance vs Drain to Source Voltage

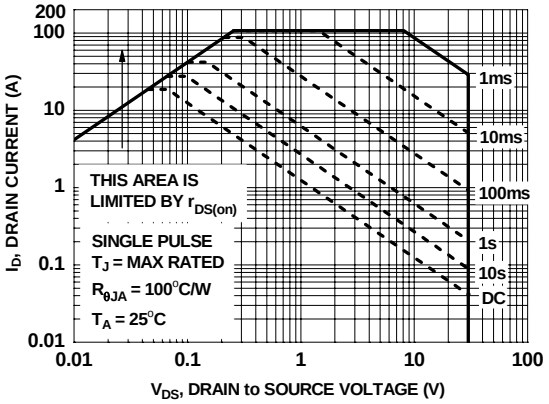


Figure 9. Forward Bias Safe Operating Area

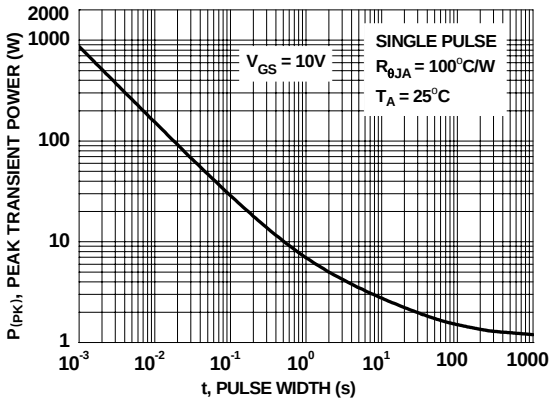


Figure 10. Single Pulse Maximum Power Dissipation

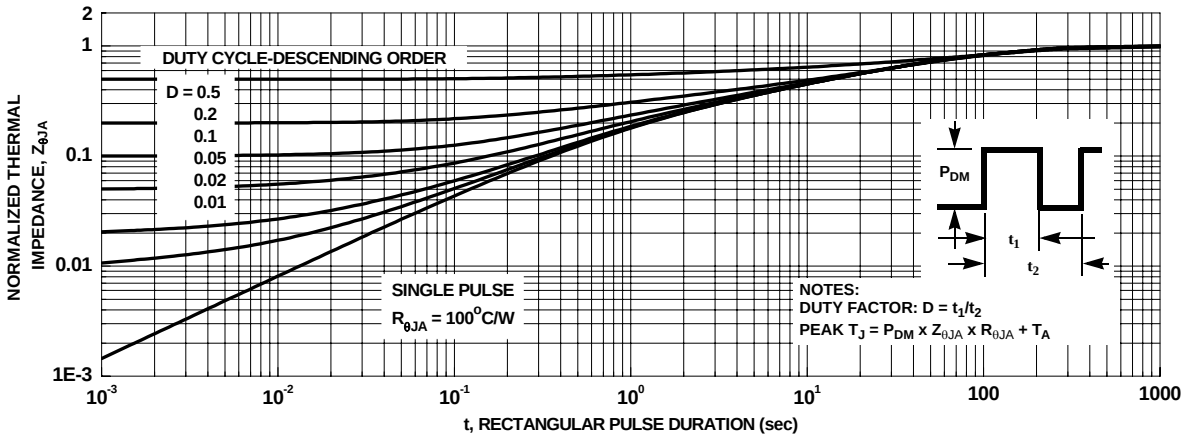


Figure 11. Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET Schottky Body Diode Charateristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 22 shows the reverse recovery characteristic of the FDZ4670S.

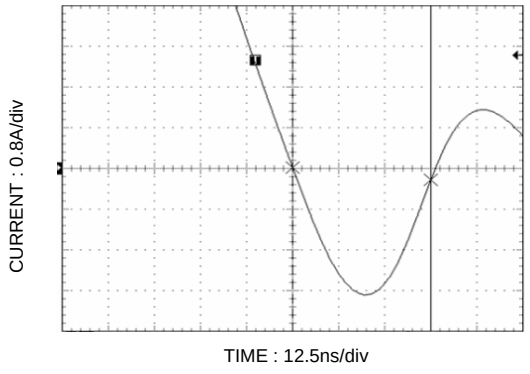


Figure 22. FDZ4670S SyncFET body diode reverse recovery characteristic

For comparison purposes, Figure 23 shows the reverse recovery characteristics of the body diode of an equivalent size MOSFET produced without SyncFET (FDZ4670).

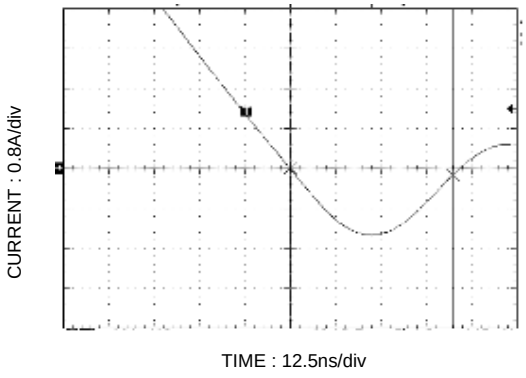


Figure 23. Non-SyncFET (FDZ4670) body diode reverse recovery characteristic

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

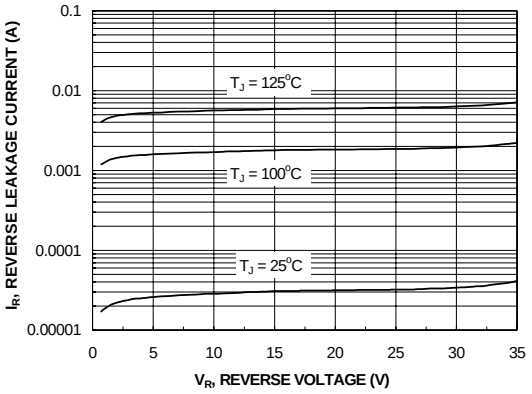
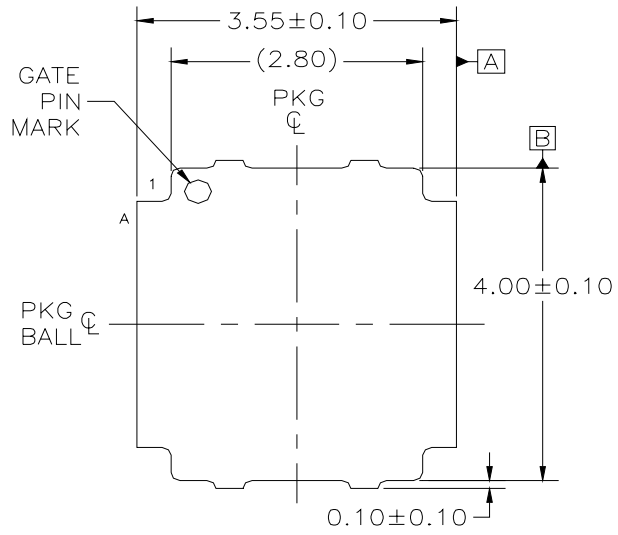
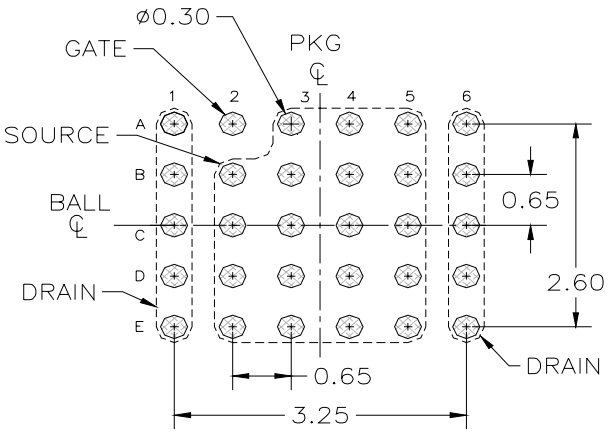


Figure 24. SyncFET body diode reverses leakage versus drain-source voltage and temperature

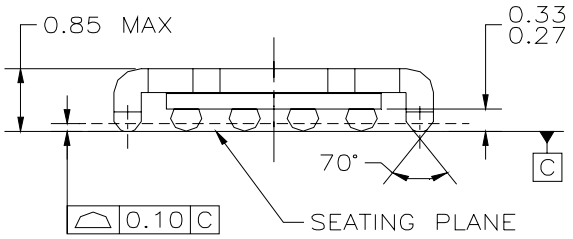
Dimensional Outline and Pad Layout



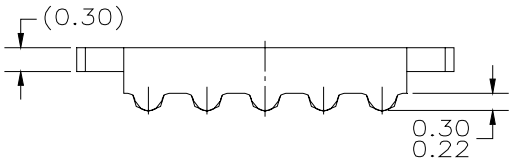
TOP VIEW



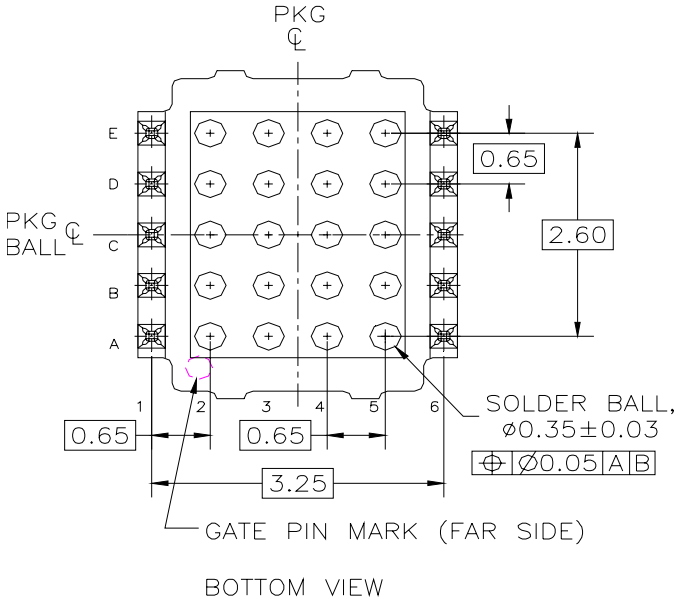
LAND PATTERN
RECOMMENDATION



FRONT VIEW



SIDE VIEW



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.

B) NO JEDEC REGISTRATION REFERENCE AS OF MARCH 2006.

C) TERMINAL CONFIGURATION TABLE

POSITION	DESIGNATION	TYPE
A1,B1,C1,D1,E1, A6,B6,C6,D6,E6	DRAIN	COPPER STUD
A2	GATE	SOLDER BALL
A3,A4,A5,B2,B3, B4,B5,C2,C3,C4, C5,D2,D3,D4,D5, E2,E3,E4,E5	SOURCE	

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