July 2005

FDZ294N

FAIRCHILD

N-Channel 2.5 V Specified PowerTrench[®] BGA MOSFET

General Description

Combining Fairchild's advanced 2.5V specified PowerTrench process with state of the art BGA packaging, the FDZ294N minimizes both PCB space and $R_{DS(ON)}$. This BGA MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, high current handling capability, ultralow profile packaging, low gate charge, and low $R_{DS(ON)}$.

Applications

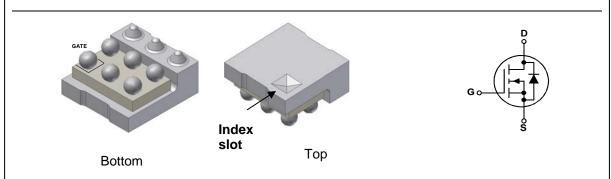
- Battery management
- Battery protection

Features

• 6 A, 20 V

$$\begin{split} R_{DS(ON)} &= 23 \ \text{m}\Omega \ @ \ V_{GS} = 4.5 \ \text{V} \\ R_{DS(ON)} &= 34 \ \text{m}\Omega \ @ \ V_{GS} = 2.5 \ \text{V} \end{split}$$

- Occupies only 2.25 mm² of PCB area. Less than 50% of the area of a SSOT-6
- Ultra-thin package: less than 0.85mm height when mounted to PCB
- Outstanding thermal transfer characteristics: 4 times better than SSOT-6
- Ultra-low Q_g x R_{DS(ON)} figure-of-merit
- High power and current handling capability.



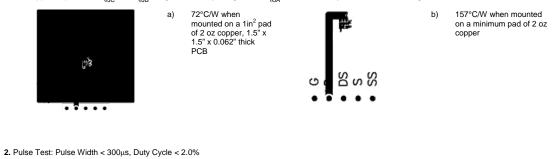
Symbol	Parameter			Ratings	Units
V _{DSS}	Drain-Source Voltage			20	V
V _{GSS}	Gate-Source Voltage			±12	V
ID	Drain Current – Continuous (Note 1a)			6	
		 Pulsed 		10	
PD	Power Dissipation for Single Operation (Note 1a)			1.7	W
T _J , T _{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C
Therma	I Charac	teristics			
R _{0JA}	Thermal Resistance, Junction-to-Ambient (Note 1a)			72	
Packag	e Markin	g and Ordering	Information		
Device Marking		Device	Reel Size	Tape width	Quantity
F	E FDZ294N 7" 8mm 3		3000 units		

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Electrical Characteristics						
Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics					
BV _{DSS}	Drain–Source Breakdown Voltage	$V_{GS}=0~V, \qquad I_D=250~\mu A$	20			V
<u>ΔBV_{DSS}</u> ΔT _J	Breakdown Voltage Temperature Coefficient	I_D = 250 µA,Referenced to 25°C		12		mV/°C
DSS	Zero Gate Voltage Drain Current	$V_{\text{DS}} = 16 \text{ V}, \qquad V_{\text{GS}} = 0 \text{ V}$			1	μA
I _{GSS}	Gate-Body Leakage.	$V_{GS}=\pm 12~V, \qquad V_{DS}=0~V$			±100	nA
On Chara	acteristics (Note 2)					
V _{GS(th)}	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}, \qquad I_{\text{D}} = 250 \; \mu\text{A}$	0.6	0.9	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 µA,Referenced to 25°C		-3		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	$ \begin{array}{ll} V_{GS} = 4.5 \ V, & I_D = 6 \ A, \\ V_{GS} = 2.5 \ V, & I_D = 5 A, \\ V_{GS} = 4.5 \ V, & I_D = 6 \ A, \ T_J {=} 125^\circ C \end{array} $		18 26 24	23 34 31	mΩ
9 _{FS}	Forward Transconductance	$V_{DS} = 5 V$, $I_D = 6 A$		24		S
Dynamic	Characteristics					
C _{iss}	Input Capacitance	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V},$		670		pF
Coss	Output Capacitance	f = 1.0 MHz		172		pF
C _{rss}	Reverse Transfer Capacitance			105		pF
R _G	Gate Resistance	V_{GS} = 15 mV, f = 1.0 MHz		1.4		Ω
Switching	Characteristics (Note 2)					
t _{d(on)}	Turn-On Delay Time	$V_{\text{DD}} = 10 \text{ V}, \qquad I_{\text{D}} = 1 \text{ A},$		8	16	ns
t _r	Turn–On Rise Time	$V_{GS} = 4.5 V, R_{GEN} = 6 \Omega$		5	10	ns
t _{d(off)}	Turn-Off Delay Time			14	25	ns
t _f	Turn–Off Fall Time			6	12	ns
Q _g	Total Gate Charge	$V_{DS} = 10V, \qquad I_D = 6 A,$		7	10	nC
Q _{gs}	Gate-Source Charge	$V_{GS} = 4.5 V$		1.4		nC
Q _{gd}	Gate-Drain Charge			2.1		nC
Drain–So	ource Diode Characteristics	and Maximum Ratings				
ls	Maximum Continuous Drain–Sour	ce Diode Forward Current			1.4	А
V _{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0 V$, $I_S = 1.4 A$ (Note 2)		0.7	1.2	V
t _{rr}	Diode Reverse Recovery Time	$I_{F} = 6 A,$		15		nS
Q _{rr}	Diode Reverse Recovery Charge	$d_{iF}/d_t = 100 \text{ A}/\mu\text{s}$		4		nC

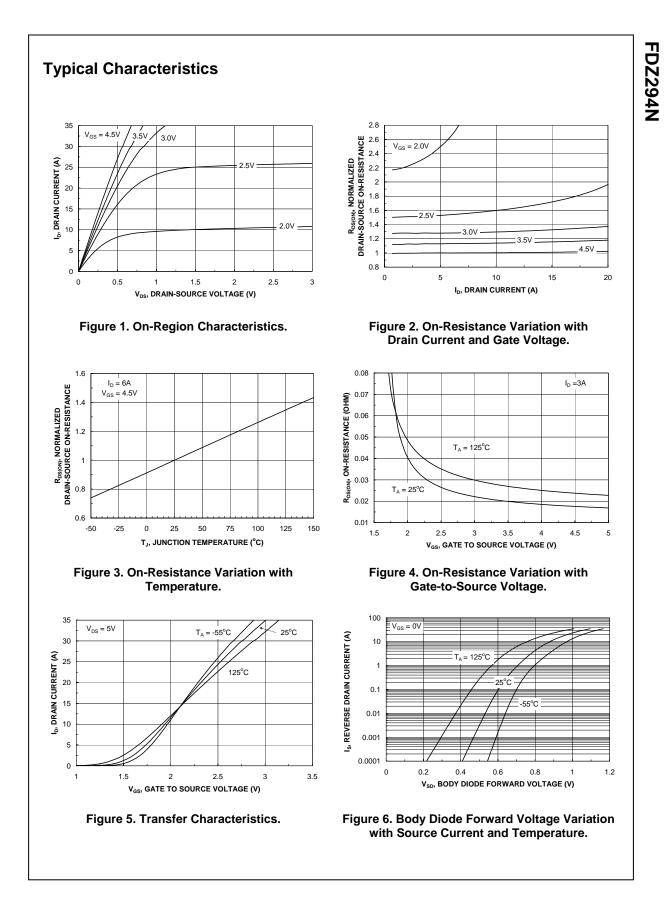
Notes:

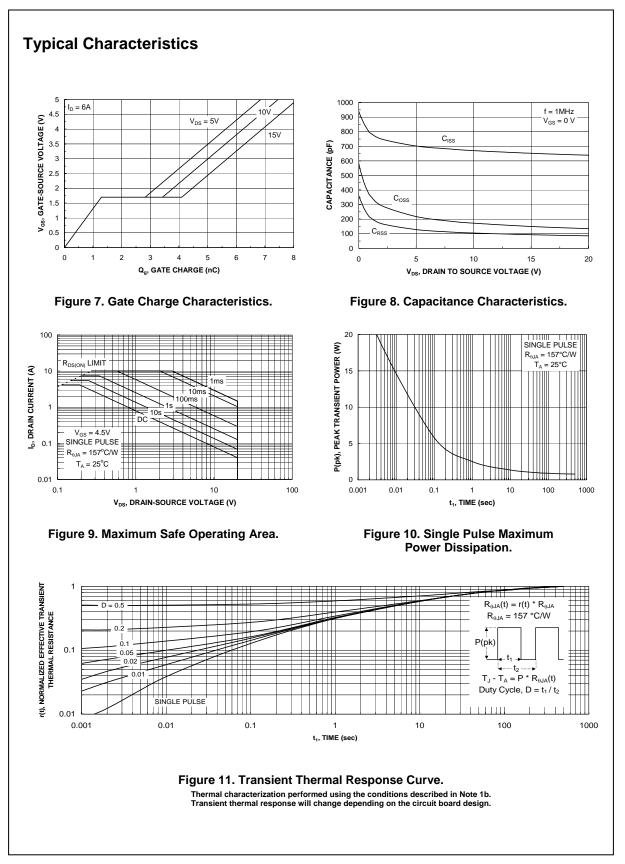
1. R_{0JA} is determined with the device mounted on a 1 in² 2 oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. The thermal resistance from the junction to the circuit board side of the solder ball, R_{0JB}, is defined for reference. For R_{0JC} the thermal reference point for the case is defined as the top surface of the copper chip carrier. R_{0JC} and R_{0JB} are guaranteed by design while R_{0JA} is determined by the user's board design.



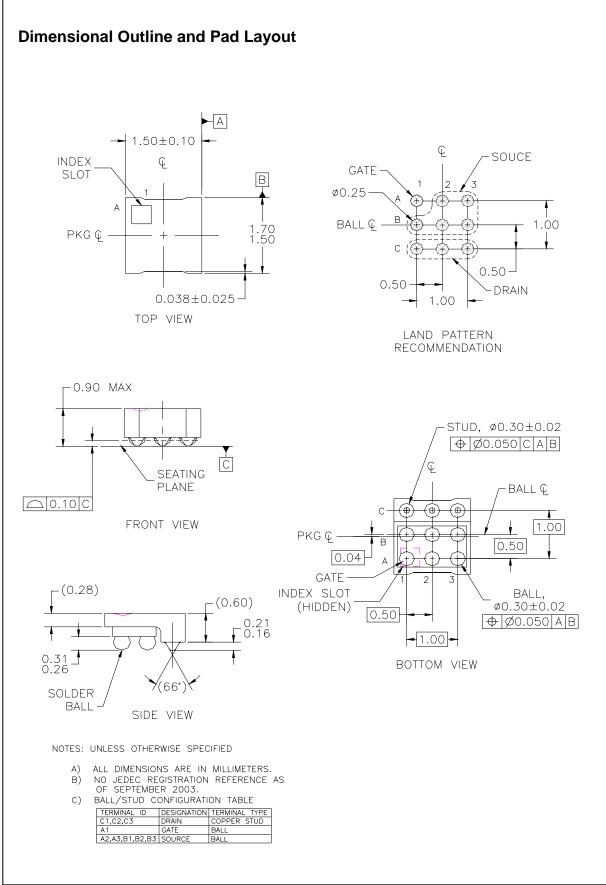
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