FAIRCHILD SEMICONDUCTOR®

February 2006

FDZ291P

P-Channel 1.5 V Specified PowerTrench® BGA MOSFET

General Description

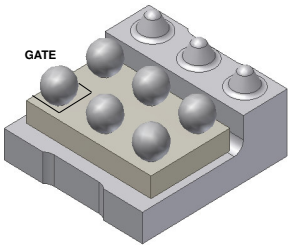
Combining Fairchild's advanced 1.5V specified PowerTrench process with state of the art BGA packaging, the FDZ291P minimizes both PCB space and $R_{DS(ON)}$. This BGA MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, high current handling capability, ultra-low profile packaging, low gate charge, and low $R_{DS(ON)}$.

Applications

- Battery management
- Load switch
- Battery protection

Features

- –4.6 A, –20 V $R_{DS(ON)}$ = 40 mΩ @ V_{GS} = –4.5 V
  $R_{DS(ON)}$ = 60 mΩ @ V_{GS} = –2.5 V
  $R_{DS(ON)}$ = 160 mΩ @ V_{GS} = –1.5 V
- Occupies only 2.25 mm^2 of PCB area.
  Less than 50% of the area of a SSOT-6
- Ultra-thin package: less than 0.85 mm height when mounted to PCB
- Outstanding thermal transfer characteristics:
  4 times better than SSOT-6
- Ultra-low Q_g x $R_{DS(ON)}$ figure-of-merit
- High power and current handling capability.



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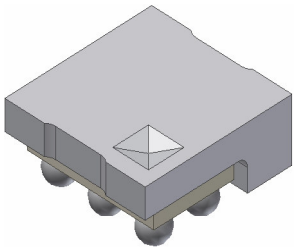

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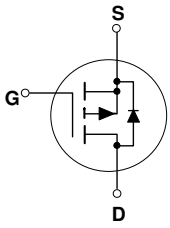


Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		–20	V
V_{GSS}	Gate-Source Voltage		±8	V
I_D	Drain Current – Continuous	(Note 1a)	–4.6	A
	– Pulsed		–10	
P_D	Power Dissipation for Single Operation	(Note 1a)	1.7	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	72	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1a)	2	

Package Marking and Ordering Information

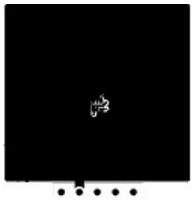
Device Marking	Device	Reel Size	Tape width	Quantity
D	FDZ291P	13”	8mm	10000 units

Electrical Characteristics T_A = 25°C unless otherwise noted

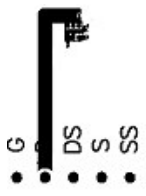
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 µA	–20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 µA, Referenced to 25°C		–12		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –16 V, V_{GS} = 0 V			–1	µA
I_{GSS}	Gate–Body Leakage.	V_{GS} = ±8 V, V_{DS} = 0 V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 µA	–0.4	–0.7	–1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = –250 µA, Referenced to 25°C		2		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = –4.5 V, I_D = –4.6 A V_{GS} = –2.5 V, I_D = –3.6 A V_{GS} = –1.5 V, I_D = –1.0 A V_{GS} = –4.5 V, I_D = –4.6 A, T_J=125°C		31 43 85 42	40 60 160 55	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = –4.5 V, V_{DS} = –5 V	–10			A
g_{FS}	Forward Transconductance	V_{DS} = –5 V, I_D = –4.6 A		16		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = –10 V, V_{GS} = 0 V, f = 1.0 MHz		1010		pF
C_{oss}	Output Capacitance			160		pF
C_{rss}	Reverse Transfer Capacitance			80		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –10 V, I_D = –1 A, V_{GS} = –4.5 V, R_{GEN} = 6 Ω		11	19	ns
t_r	Turn–On Rise Time			9	18	ns
$t_{d(off)}$	Turn–Off Delay Time			36	58	ns
t_f	Turn–Off Fall Time			16	29	ns
Q_g	Total Gate Charge	V_{DS} = –10V, I_D = –4.6 A, V_{GS} = –4.5 V		9	13	nC
Q_{gs}	Gate–Source Charge			1.6		nC
Q_{gd}	Gate–Drain Charge			1.9		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				–1.4	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0V, I_S = –1.4 A (Note 2)		–0.7	–1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = –4.6 A, dI_F/dt = 100A/µs		17		ns
Q_{rr}	Diode Reverse Recovery Charge			5		nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² 2 oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. The thermal resistance from the junction to the circuit board side of the solder ball, $R_{\theta JB}$, is defined for reference. For $R_{\theta JC}$, the thermal reference point for the case is defined as the top surface of the copper chip carrier. $R_{\theta JC}$ and $R_{\theta JB}$ are guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 72°C/W when mounted on a 1in² pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB



b) 157°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics

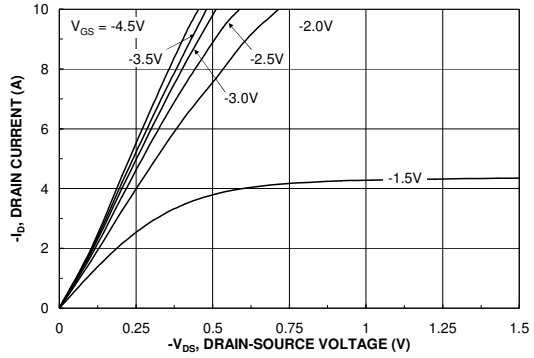


Figure 1. On-Region Characteristics.

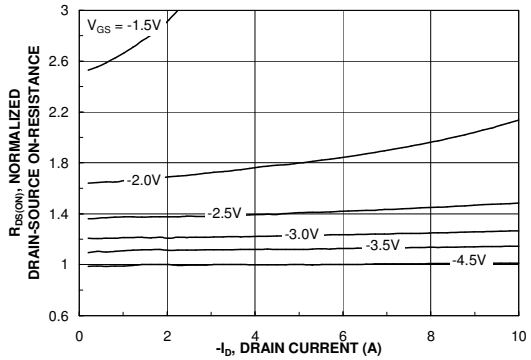


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

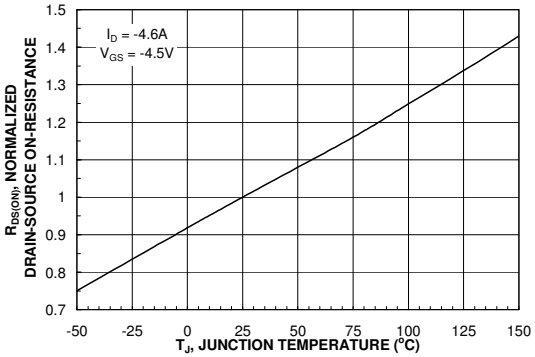


Figure 3. On-Resistance Variation with Temperature.

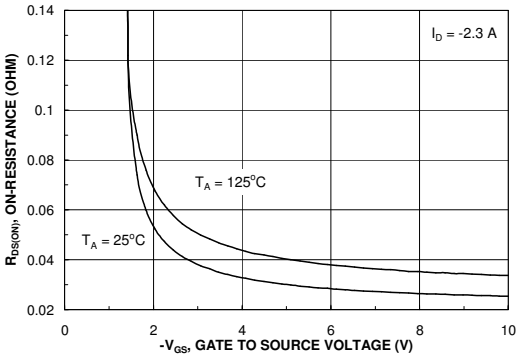


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

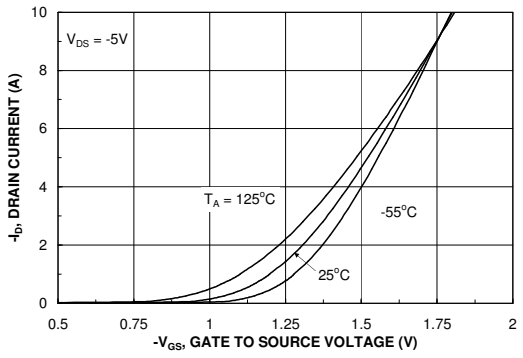


Figure 5. Transfer Characteristics.

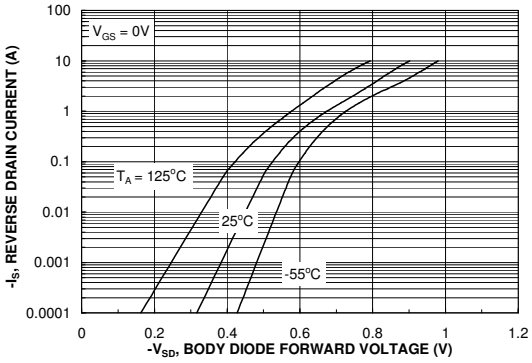


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

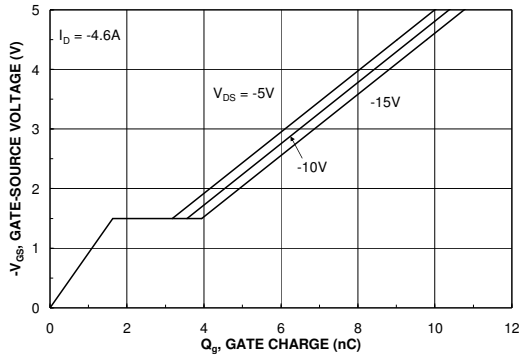


Figure 7. Gate Charge Characteristics.

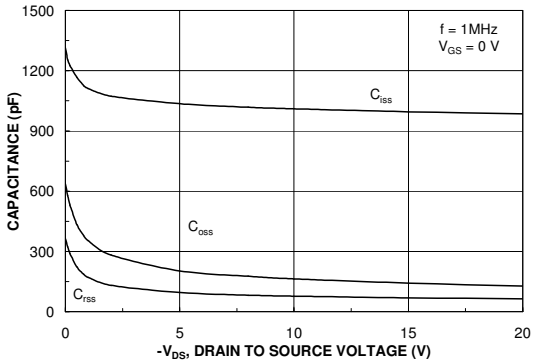


Figure 8. Capacitance Characteristics.

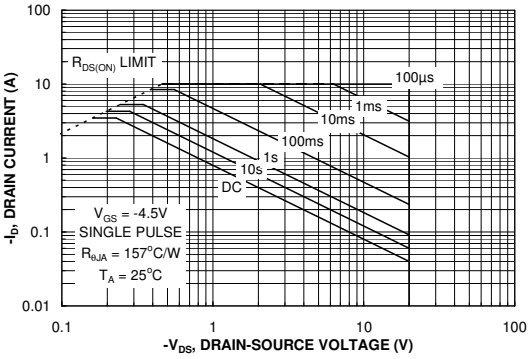


Figure 9. Maximum Safe Operating Area.

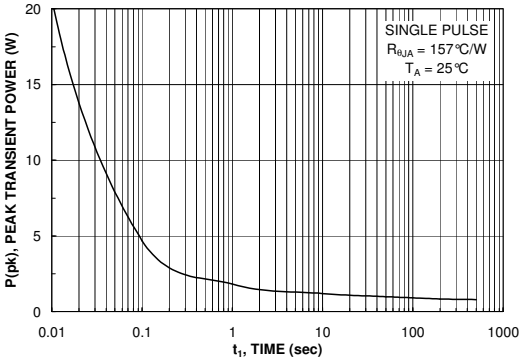


Figure 10. Single Pulse Maximum Power Dissipation.

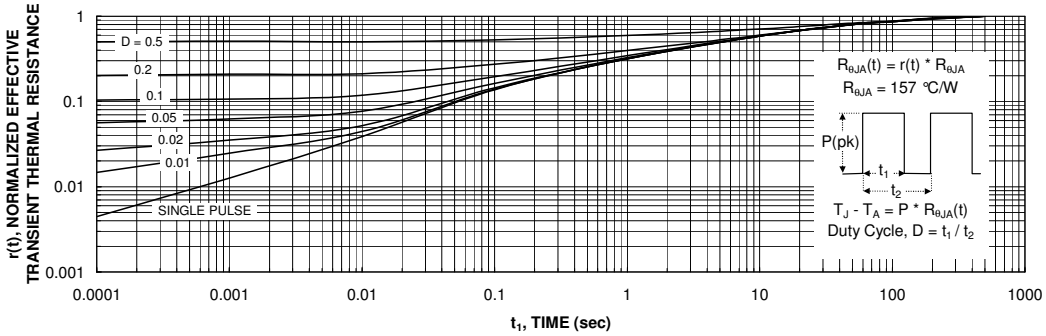
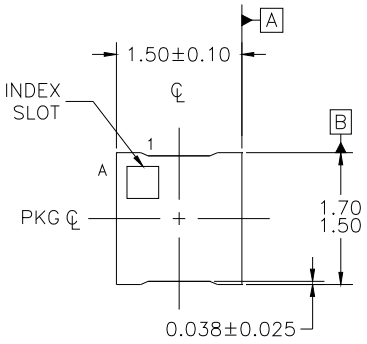


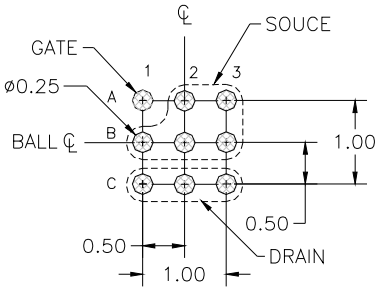
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

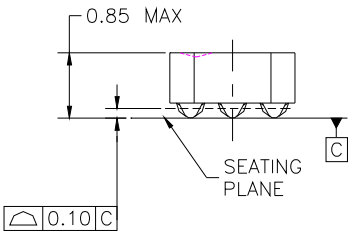
Dimensional Pad and Layout



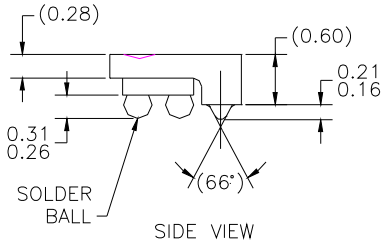
TOP VIEW



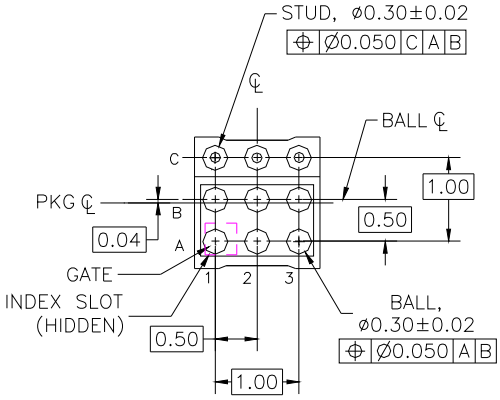
LAND PATTERN
RECOMMENDATION



FRONT VIEW



SIDE VIEW



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) NO JEDEC REGISTRATION REFERENCE AS OF SEPTEMBER 2003.
C) BALL/STUD CONFIGURATION TABLE

TERMINAL ID	DESIGNATION	TERMINAL TYPE
C1,C2,C3	DRAIN	COPPER STUD
A1	GATE	BALL
A2,A3,B1,B2,B3	SOURCE	BALL

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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