

FDZ204P

P-Channel 2.5V Specified PowerTrench® BGA MOSFET

General Description

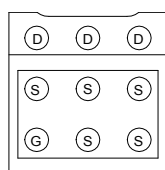
Combining Fairchild's advanced 2.5V specified PowerTrench process with state of the art BGA packaging, the FDZ204P minimizes both PCB space and $R_{DS(ON)}$. This BGA MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, high current handling capability, ultra-low profile packaging, low gate charge, and low $R_{DS(ON)}$.

Applications

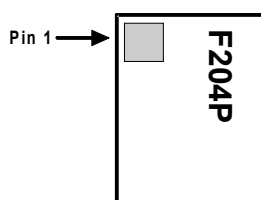
- Battery management
- Load switch
- Battery protection

Features

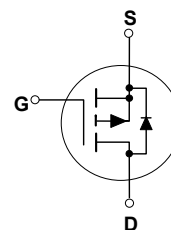
- -4.5 A, -20 V. $R_{DS(ON)} = 45 \text{ m}\Omega @ V_{GS} = -4.5 \text{ V}$
 $R_{DS(ON)} = 75 \text{ m}\Omega @ V_{GS} = -2.5 \text{ V}$
- Occupies only 4 mm² of PCB area. Less than 40% of the area of a SSOT-6
- Ultra-thin package: less than 0.80 mm height when mounted to PCB
- Ultra-low $Q_g \times R_{DS(ON)}$ figure-of-merit.
- High power and current handling capability.



Bottom



Top



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Rated	Units
V_{DSS}	Drain-Source Voltage	-20	V
V_{GSS}	Gate-Source Voltage	±12	V
I_D	Drain Current – Continuous (Note 1a)	-4.5	A
	– Pulsed	-20	
P_D	Power Dissipation (Steady State) (Note 1a)	1.8	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	67	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Ball (Note 1)	11	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	1	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
204P	FDZ204P	7"	8mm	3000 units

Electrical Characteristics

 $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C		-17		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
I_{GSSF}	Gate–Body Leakage, Forward	$V_{GS} = -12\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	$V_{GS} = 12\text{ V}, V_{DS} = 0\text{ V}$			100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.6	-0.9	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C		3		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -4.5\text{ V}, I_D = -4.5\text{ A}$ $V_{GS} = -2.5\text{ V}, I_D = -3.5\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -4.5\text{ A}, T_J = 125^\circ\text{C}$		37 57 50	45 75 65	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -4.5\text{ A}$		15		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$		884		pF
C_{oss}	Output Capacitance	$f = 1.0\text{ MHz}$		258		pF
C_{rss}	Reverse Transfer Capacitance			103		pF

Switching Characteristics (Note 2)

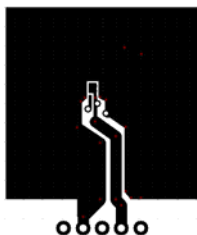
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -6\text{ V}, I_D = -1\text{ A},$		12	22	ns
t_r	Turn–On Rise Time	$V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$		9	18	ns
$t_{d(off)}$	Turn–Off Delay Time			36	58	ns
t_f	Turn–Off Fall Time			24	38	ns
Q_g	Total Gate Charge	$V_{DS} = -10\text{ V}, I_D = -4.5\text{ A},$		9	13	nC
Q_{gs}	Gate–Source Charge	$V_{GS} = -4.5\text{ V}$		2		nC
Q_{gd}	Gate–Drain Charge			3		nC

Drain–Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain–Source Diode Forward Current				-1.5	A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -1.5\text{ A}$ (Note 2)		-0.76	-1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = -5.5\text{ A},$		25		nS
Q_{rr}	Diode Reverse Recovery Charge	$dI_F/dt = 100\text{ A}/\mu\text{s}$		26		nC

Notes:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² 2 oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. The thermal resistance from the junction to the circuit board side of the solder ball, $R_{\theta JB}$, is defined for reference. For $R_{\theta JC}$, the thermal reference point for the case is defined as the top surface of the copper chip carrier. $R_{\theta JC}$ and $R_{\theta JB}$ are guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



- a) 67 °C/W when mounted on a 1in² pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB

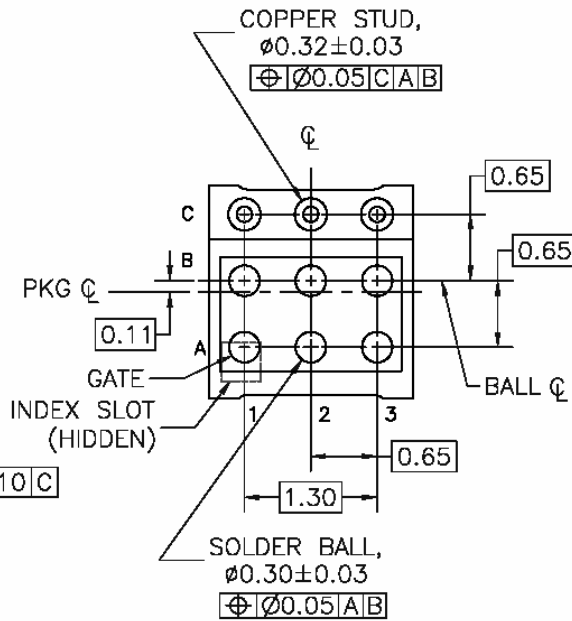
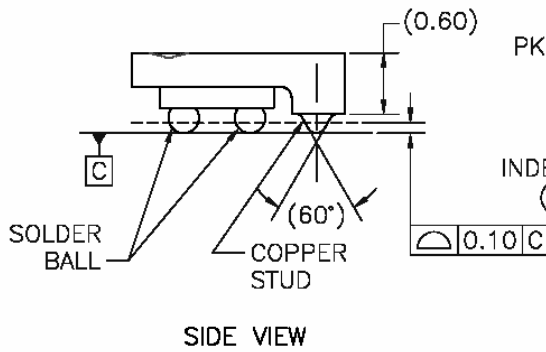
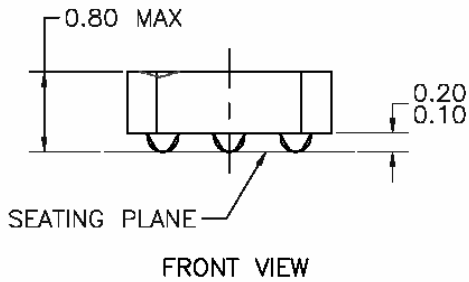
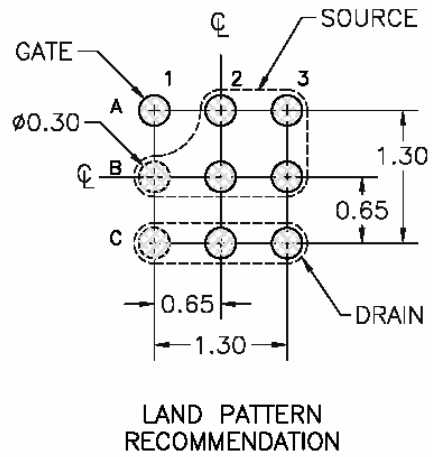
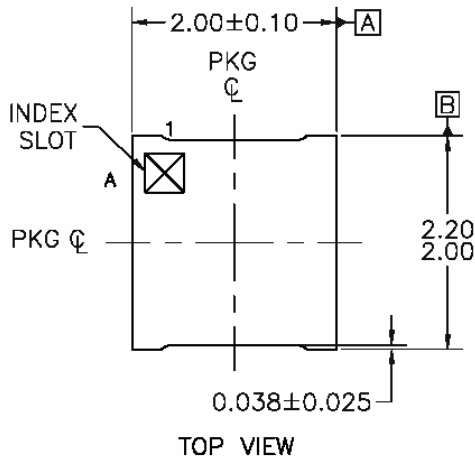


- b) 155 °C/W when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) NO JEDEC REGISTRATION REFERENCE AS OF JULY 1999.
- C) TERMINAL CONFIGURATION TABLE.

POSITION	DESIGNATION	TYPE
C1,C2,C3	DRAIN	COPPER STUD
A1	GATE	SOLDER BALL
A2,A3,B1,B2,B3	SOURCE	SOLDER BALL

Typical Characteristics

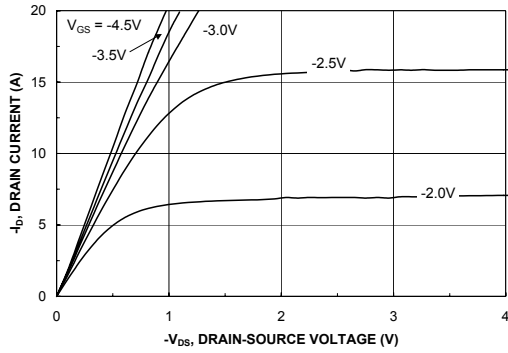


Figure 1. On-Region Characteristics.

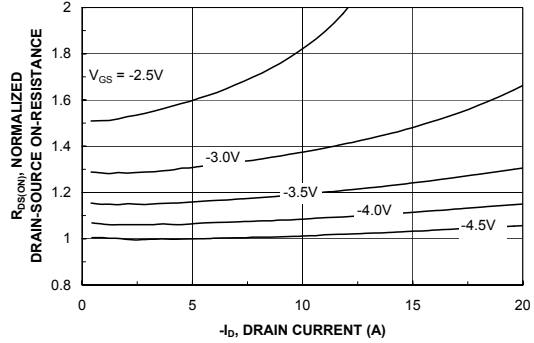


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

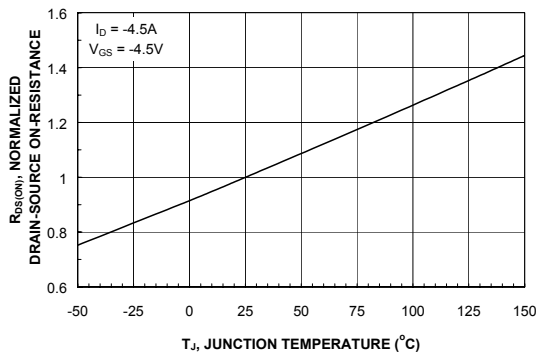


Figure 3. On-Resistance Variation with Temperature.

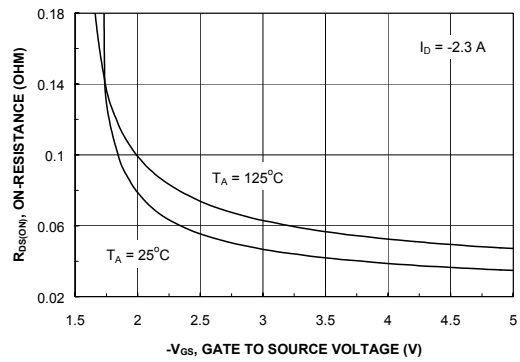


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

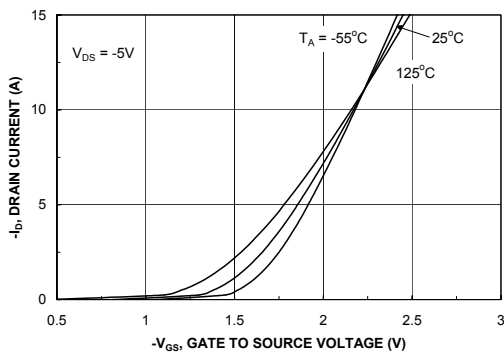


Figure 5. Transfer Characteristics.

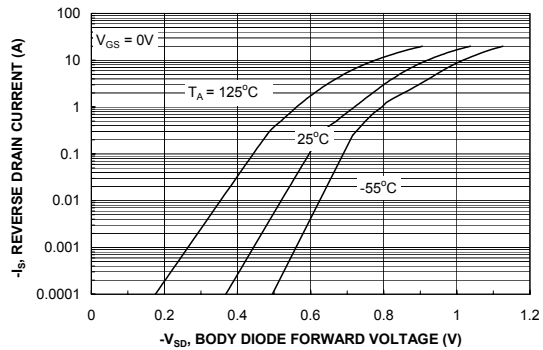


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

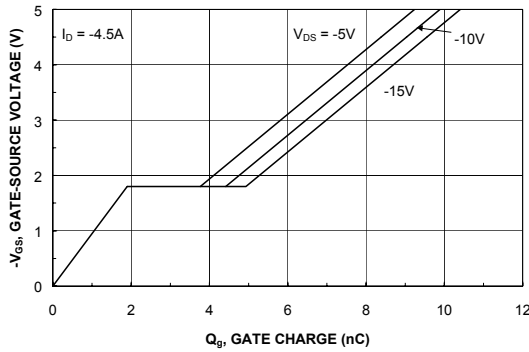


Figure 7. Gate Charge Characteristics.

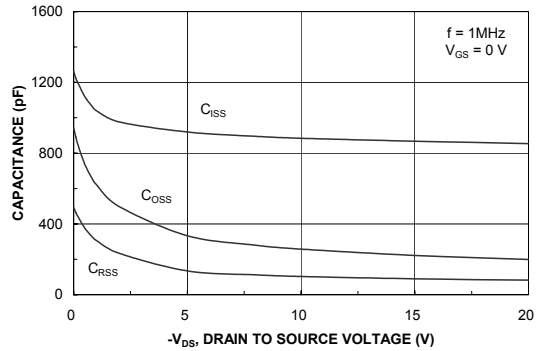


Figure 8. Capacitance Characteristics.

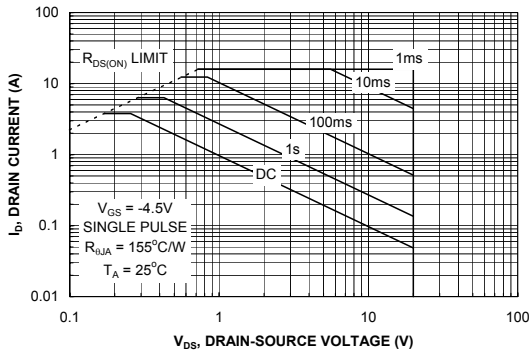


Figure 9. Maximum Safe Operating Area.

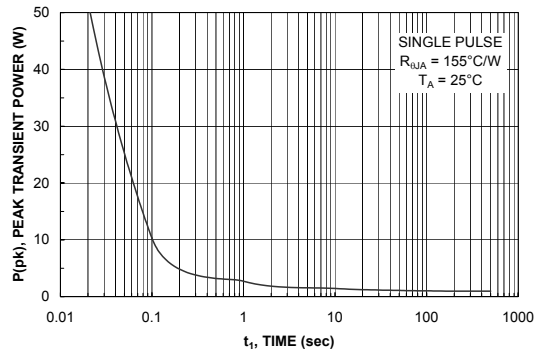


Figure 10. Single Pulse Maximum Power Dissipation.

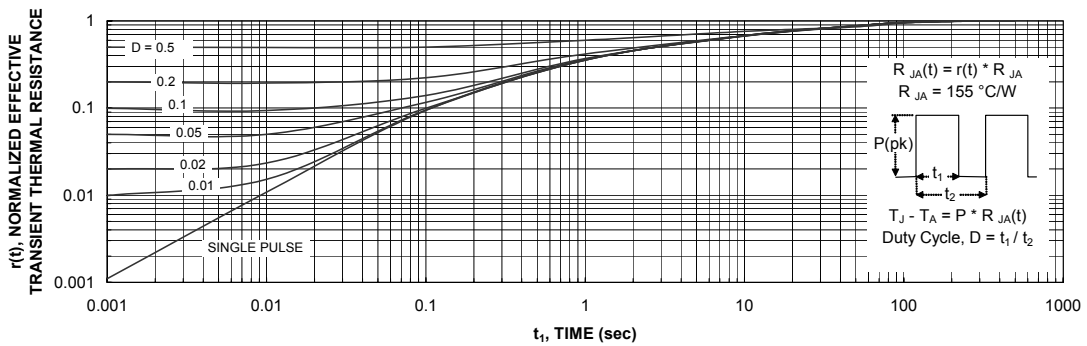


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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