

FDW2508PB

Dual P-Channel -1.8V Specified PowerTrench® MOSFET

-12V, -6A, 18mΩ

Features

- Max $r_{DS(on)}$ = 18mΩ at $V_{GS} = -4.5V$, $I_D = -6A$
- Max $r_{DS(on)}$ = 22mΩ at $V_{GS} = -2.5V$, $I_D = -5A$
- Max $r_{DS(on)}$ = 30mΩ at $V_{GS} = -1.8V$, $I_D = -4A$
- Low gate charge
- High performance trench technology for extremely low $r_{DS(on)}$
- Low profile TSSOP-8 package
- RoHS compliant

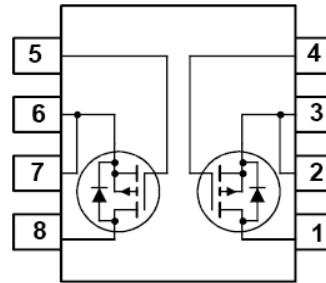
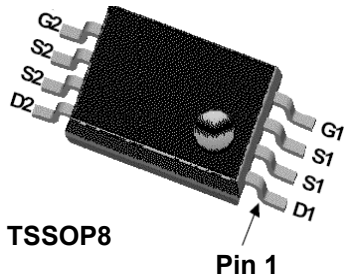


General Description

This P-Channel -1.8V specified MOSFET uses Fairchild Semiconductor's advanced low voltage PowerTrench®. It has been optimized for battery power management applications.

Application

- Power management
- Load switch
- Battery protection



MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Rated	Units
V_{DS}	Drain to Source Voltage	-12	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	Drain Current -Continuous (Note 1a)	-6	A
	-Pulsed	-30	
P_D	Power Dissipation-Dual Operation	2	W
	Power Dissipation-Single Operation (Note 1a)	1.6	
	(Note 1b)	1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	80	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	125	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
2508PB	FDW2508PB	TSSOP-8	13"	12mm	2500 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	-12			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$, referenced to 25°C		-12		$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -10\text{V}$ $V_{GS} = 0\text{V}$ $T_J = 125^\circ\text{C}$			-1 -100	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 8\text{V}, V_{DS} = 0\text{V}$			± 100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	-0.4	-0.6	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$, referenced to 25°C		3		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On-Resistance	$V_{GS} = -4.5\text{V}, I_D = -6\text{A}$		15	18	$\text{m}\Omega$
		$V_{GS} = -2.5\text{V}, I_D = -5\text{A}$		18	22	
		$V_{GS} = -1.8\text{V}, I_D = -4\text{A}$		22	30	
		$V_{GS} = -4.5\text{V}, I_D = -6\text{A}, T_J = 125^\circ\text{C}$		23	30	
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{V}, I_D = -6\text{A}$		35		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -6\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$		2835	3775	pF
C_{oss}	Output Capacitance			440	590	pF
C_{rss}	Reverse Transfer Capacitance			370	555	pF

Switching Characteristics

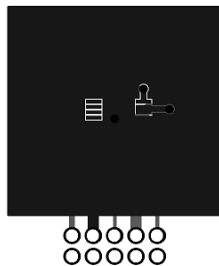
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -6\text{V}, I_D = -6\text{A}$ $V_{GS} = -4.5\text{V}, R_{GEN} = 6\Omega$		8	16	ns
t_r	Rise Time			16	29	ns
$t_{d(off)}$	Turn-Off Delay Time			254	407	ns
t_f	Fall Time			106	170	ns
Q_g	Total Gate Charge		$V_{GS} = -4.5\text{V}, V_{DD} = -6\text{V}$ $I_D = -6\text{A}$		32	45
Q_{gs}	Gate to Source Gate Charge			4.3		nC
Q_{gd}	Gate to Drain "Miller" Charge			7.1		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = -1.1\text{A}$ (Note 2)		-0.6	-1.2	V
t_{rr}	Reverse Recovery Time	$I_F = -6\text{A}, di/dt = 100\text{A}/\mu\text{s}$		106	159	ns
Q_{rr}	Reverse Recovery Charge			110	165	nC

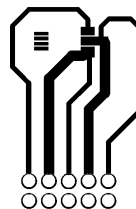
Notes:

1: $R_{\theta JA}$ is the sum of junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $R_{\theta JA}$ is $80^\circ\text{C}/\text{W}$ (steady state) when mounted on a 1 in^2 pad of 2 oz copper.

Scale 1 : 1 on letter size paper



b. $R_{\theta JA}$ is $125^\circ\text{C}/\text{W}$ (steady state) when mounted on a minimum pad.

2: Pulse Test: Pulse Width < $300\mu\text{s}$, Duty cycle < 2.0%.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

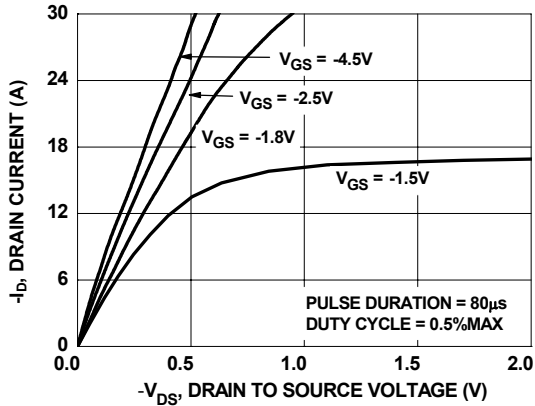


Figure 1. On Region Characteristics

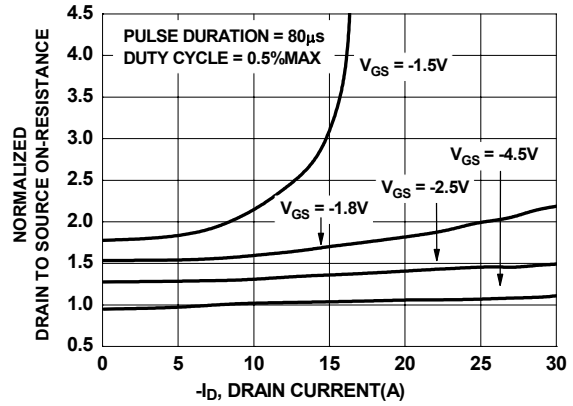


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

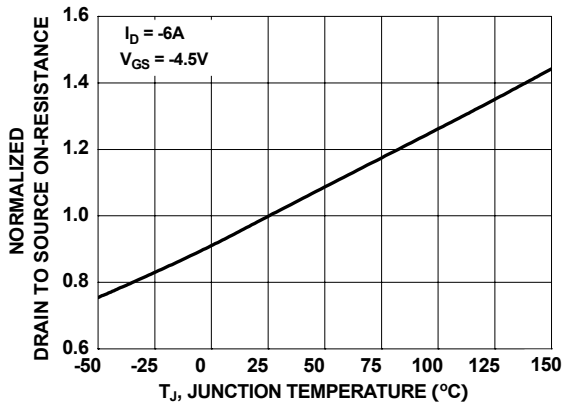


Figure 3. Normalized On Resistance vs Junction Temperature

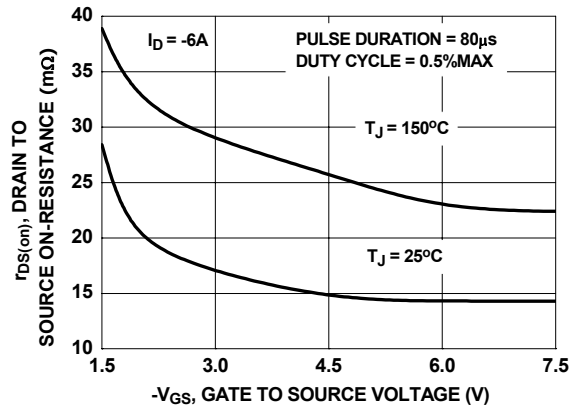


Figure 4. On-Resistance vs Gate to Source Voltage

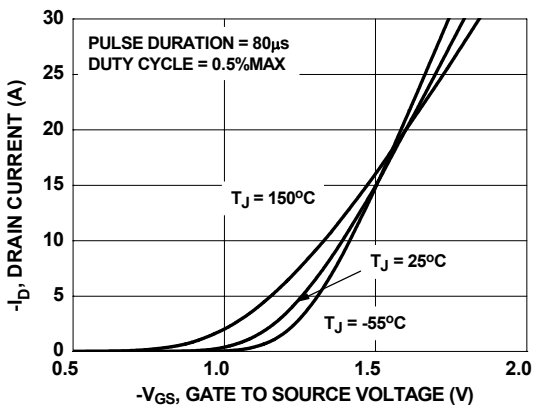


Figure 5. Transfer Characteristics

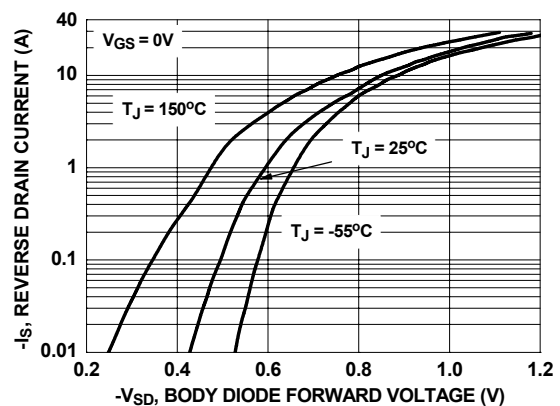


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

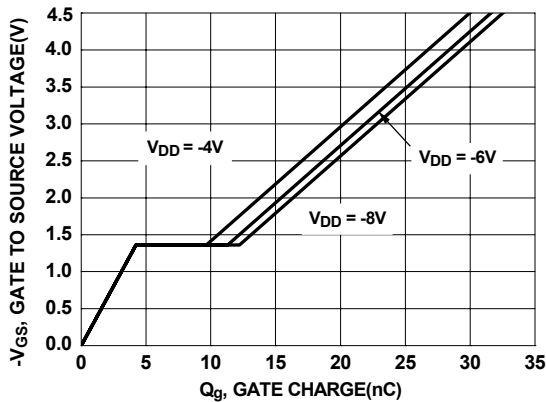


Figure 7. Gate Charge Characteristics

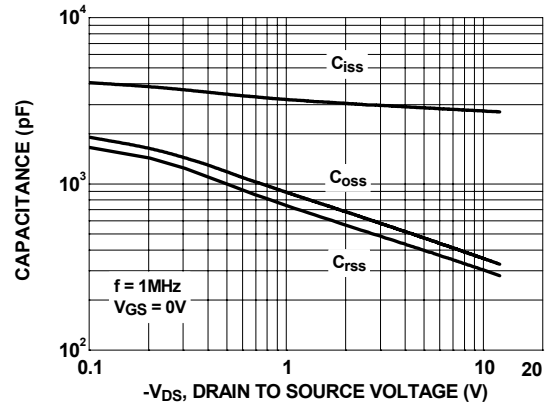


Figure 8. Capacitance vs Drain to Source Voltage

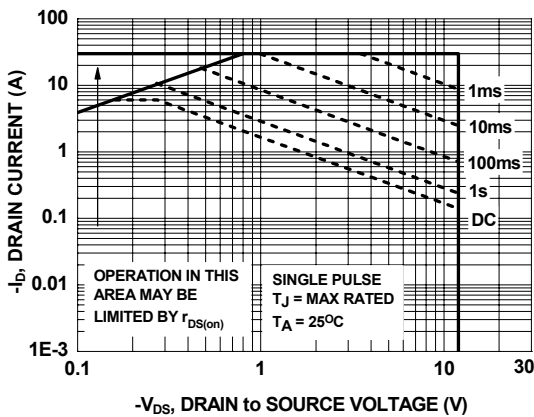


Figure 9. Forward Bias Safe Operating Area

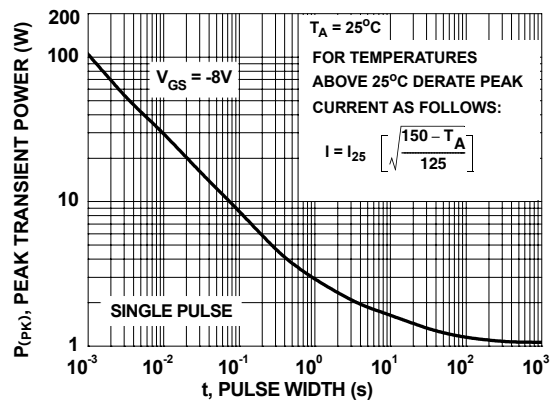


Figure 10. Single Pulse Maximum Power Dissipation

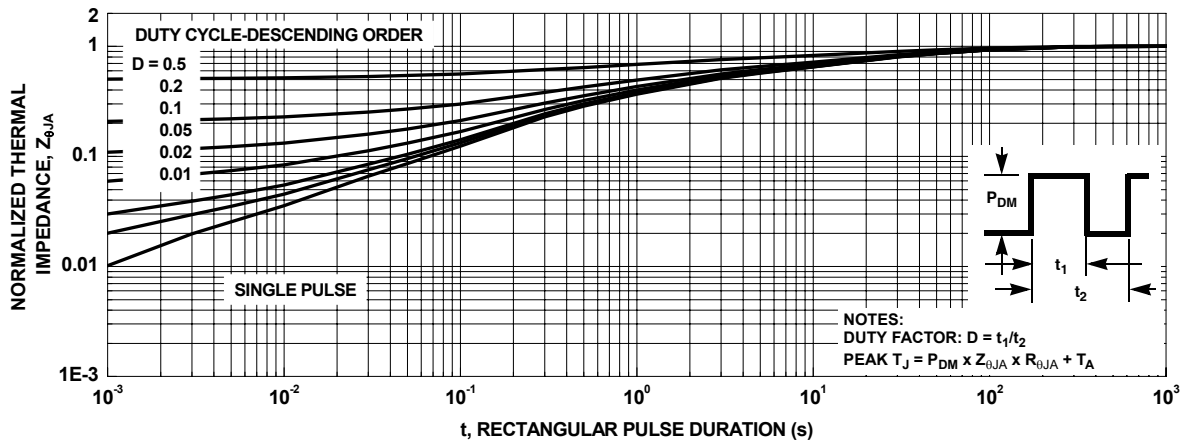
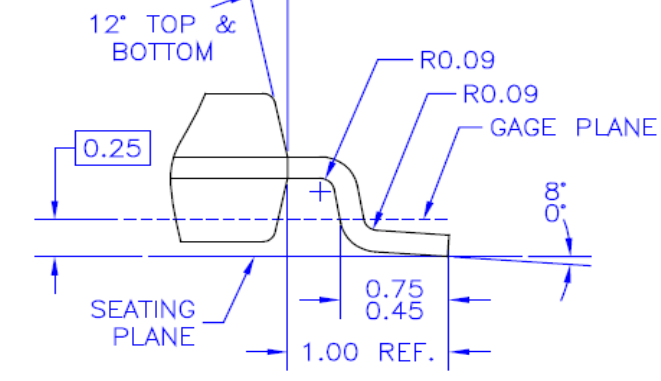
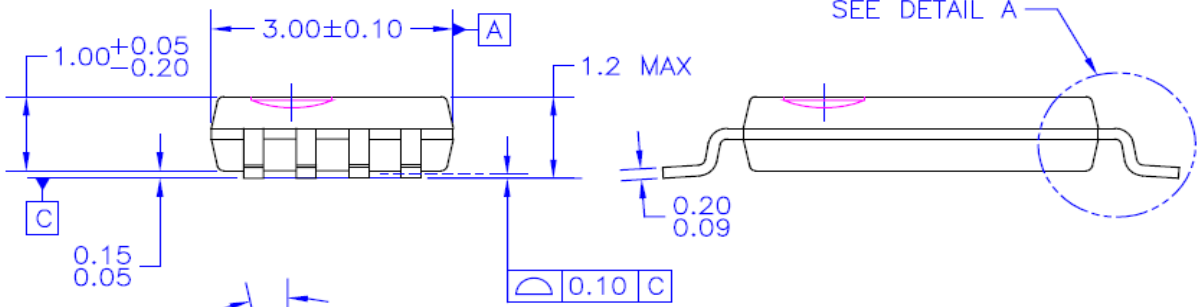
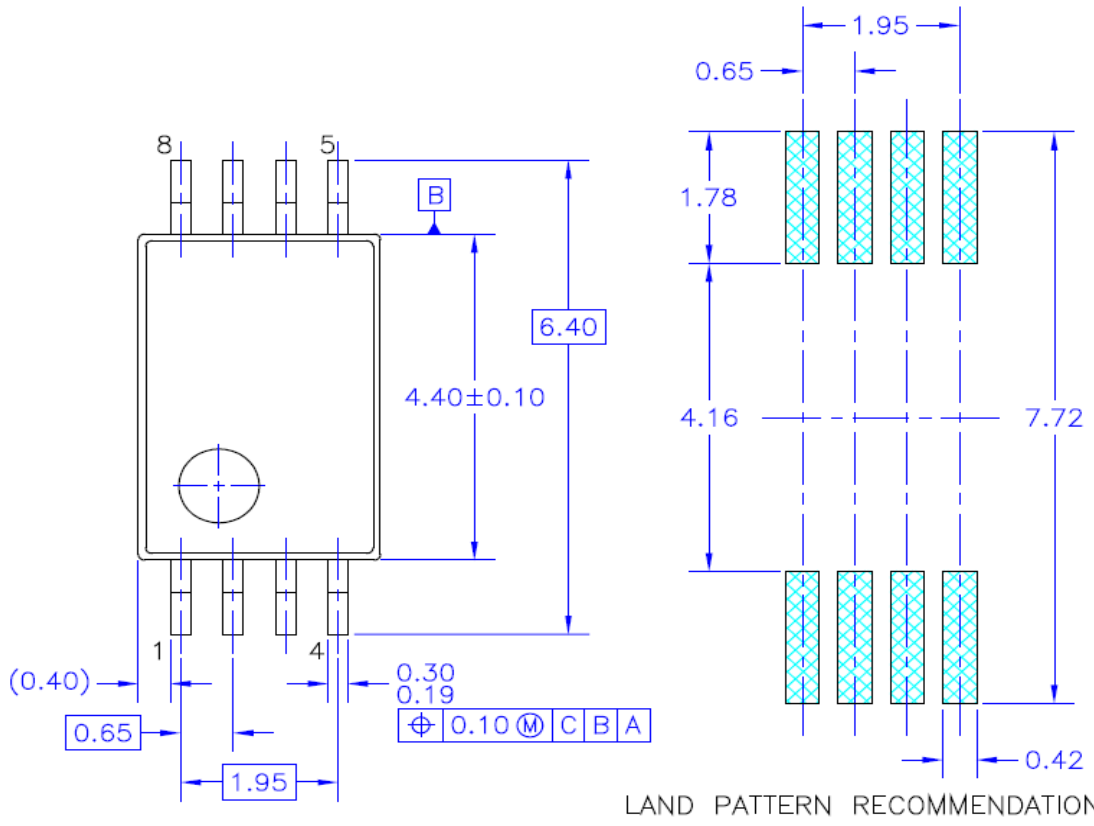


Figure 11. Transient Thermal Response Curve



- NOTES: UNLESS OTHERWISE SPECIFIED
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 - D) DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

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