

# FDS9412A

## N-Channel PowerTrench® MOSFET

30V, 8A, 21mΩ

### General Description

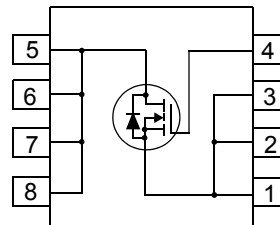
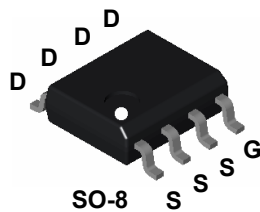
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $r_{DS(on)}$  and fast switching speed.

### Features

- Max  $r_{DS(on)}$  = 21mΩ at  $V_{GS} = 10V$ ,  $I_D = 8A$
- Max  $r_{DS(on)}$  = 25mΩ at  $V_{GS} = 4.5V$ ,  $I_D = 6.6A$
- Low gate charge
- RoHS Compliant

### Application

- DC/DC converters



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current		
	-Continuous ( $T_A = 25^\circ\text{C}$ , $V_{GS} = 10V$ , $R_{\theta JA} = 50^\circ\text{C/W}$ )	8	A
	-Continuous ( $T_A = 25^\circ\text{C}$ , $V_{GS} = 4.5V$ , $R_{\theta JA} = 50^\circ\text{C/W}$ )	6.6	A
	-Pulsed	30	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	54	mJ
$P_D$	Power dissipation	2.5	W
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to 150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	25	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	$^\circ\text{C/W}$

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS9412A	FDS9412A	SO-8	330mm	12mm	2500 units

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		22		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}, V_{GS} = 0\text{V}$ $T_J = 150^\circ\text{C}$			1 250	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$			$\pm 100$	$\mu\text{A}$

**On Characteristics (Note 2)**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1.2	1.9	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-5.8		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 8\text{A}$ $V_{GS} = 4.5\text{V}, I_D = 6.6\text{A}$ $V_{GS} = 10\text{V}, I_D = 8\text{A}$ $T_J = 150^\circ\text{C}$		14 18 20	21 25 30	$\text{m}\Omega$

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		740	985	pF
$C_{oss}$	Output Capacitance			150	200	pF
$C_{riss}$	Reverse Transfer Capacitance			95	145	pF
$R_G$	Gate Resistance		$f = 1\text{MHz}$	3		$\Omega$

**Switching Characteristics (Note 2)**

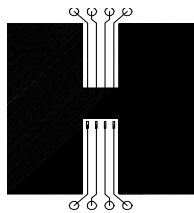
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{V}, I_D = 1\text{A}$ $V_{GS} = 10\text{V}, R_{GS} = 6\Omega$		5	10	ns	
$t_r$	Rise Time			13	23	ns	
$t_{d(off)}$	Turn-Off Delay Time			13	24	ns	
$t_f$	Fall Time			12	22	ns	
$Q_g$	Total Gate Charge at 10V		$V_{GS} = 0\text{V}$ to $10\text{V}$		14	20	nC
$Q_g$	Total Gate Charge at 5V	$V_{GS} = 0\text{V}$ to $5\text{V}$	$V_{DD} = 15\text{V}$ $I_D = 8\text{A}$ $I_G = 1.0\text{mA}$		8	12	nC
$Q_{gs}$	Gate to Source Gate Charge				2.3		nC
$Q_{gd}$	Gate to Drain "Miller" Charge				3.0		nC

**Drain-Source Diode Characteristics**

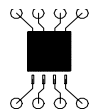
$V_{SD}$	Source to Drain Diode Voltage	$V_{GS} = 0\text{V}, I_S = 8\text{A}$ $V_{GS} = 0\text{V}, I_S = 2.1\text{A}$		0.85 0.76	1.25 1.0	V
$t_{rr}$	Reverse Recovery Time	$I_F = 8\text{A}, di/dt = 100\text{A}/\mu\text{s}$		18	27	ns
$Q_{rr}$	Reverse Recovery Charge	$I_F = 8\text{A}, di/dt = 100\text{A}/\mu\text{s}$		9.6	14	nC

**Notes:**

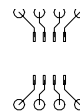
1:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $50^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b)  $105^\circ\text{C}/\text{W}$  when mounted on a  $.04\text{ in}^2$  pad of 2 oz copper



c)  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad

Scale 1 : 1 on letter size paper

2: Pulse Test: Pulse Width  $< 300\mu\text{s}$ , Duty Cycle  $< 2.0\%$ .  
3: Starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\text{mH}$ ,  $I_{AS} = 6\text{A}$ ,  $V_{DD} = 30\text{V}$ ,  $V_{GS} = 10\text{V}$ .

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

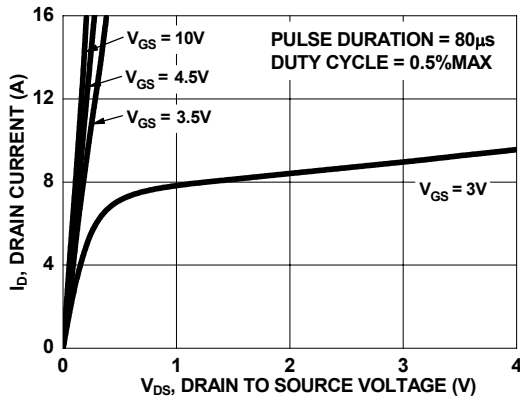


Figure 1. On Region Characteristics

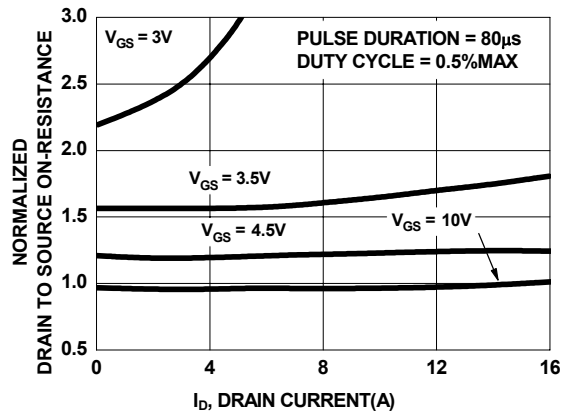


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

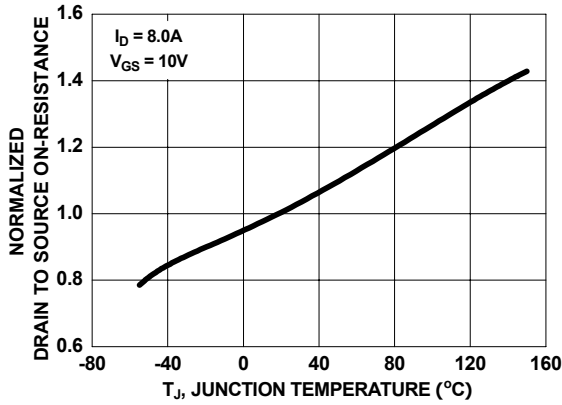


Figure 3. Normalized On Resistance vs Junction Temperature

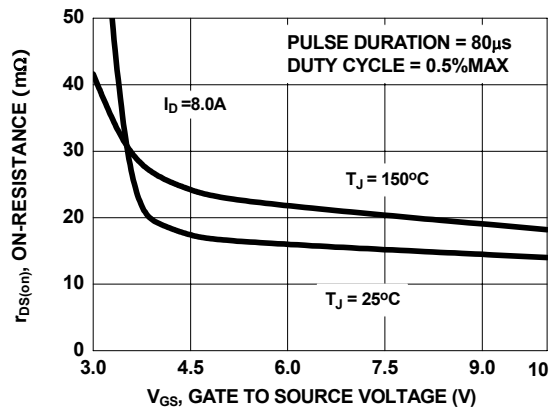


Figure 4. On-Resistance vs Gate to Source Voltage

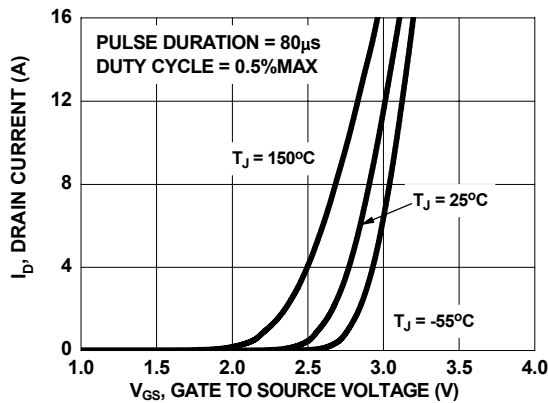


Figure 5. Transfer Characteristics

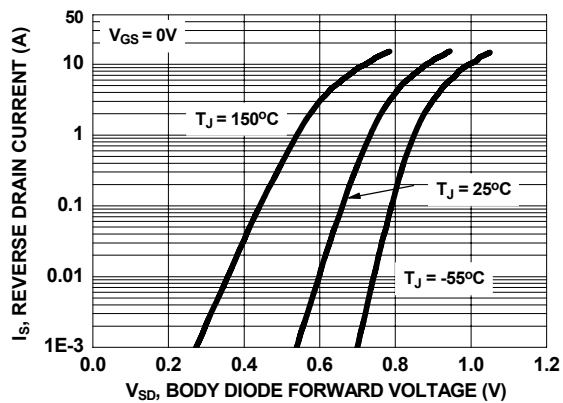


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

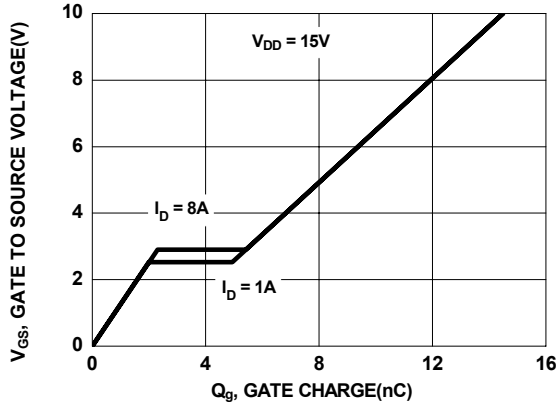


Figure 7. Gate Charge Characteristics

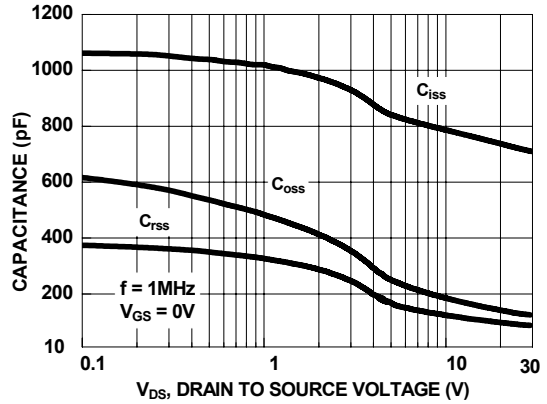


Figure 8. Capacitance vs Drain to Source Voltage

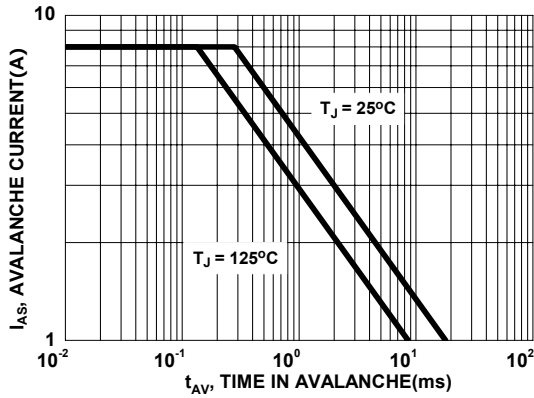


Figure 9. Unclamped Inductive Switching Capability

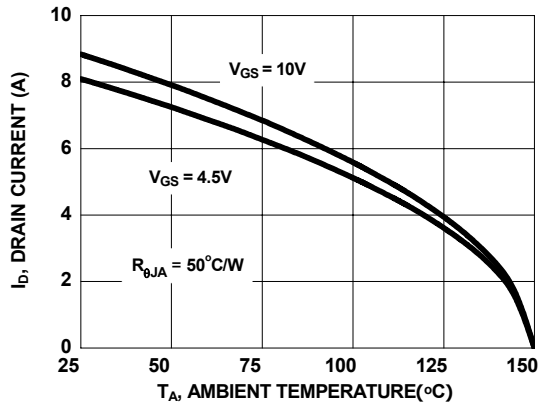


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

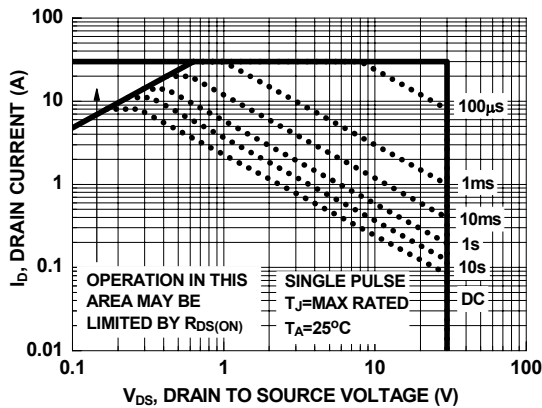


Figure 11. Forward Bias Safe Operating Area

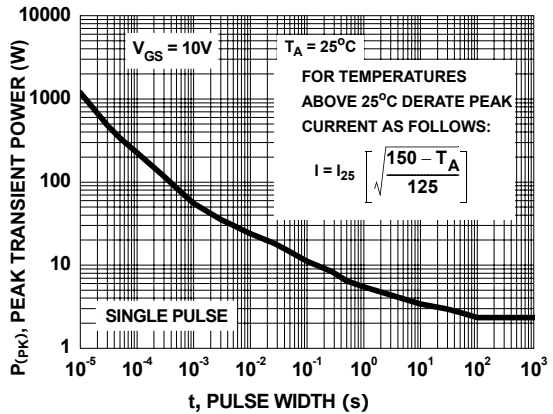


Figure 12. Single Pulse Maximum Power Dissipation

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

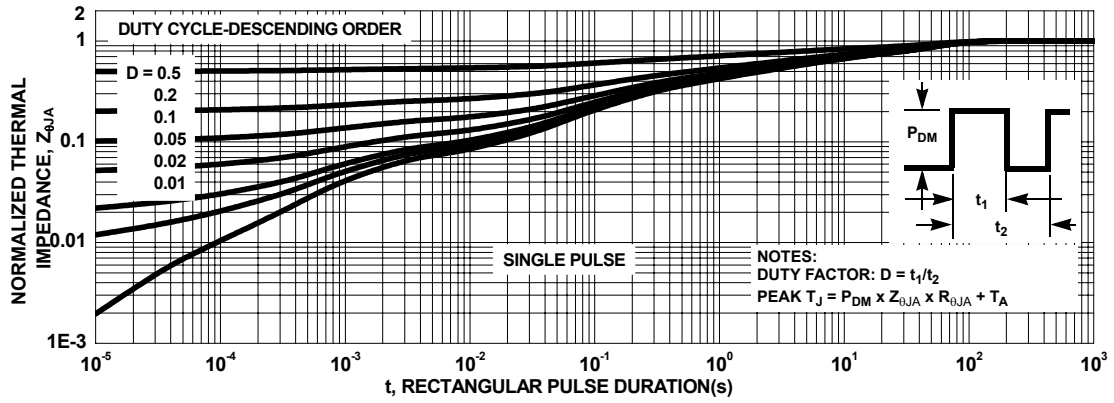


Figure 13. Transient Thermal Response Curve

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