



FDS8670 30V N-Channel PowerTrench<sup>®</sup> MOSFET

# FDS8670

## 30V N-Channel PowerTrench<sup>®</sup> MOSFET

### General Description

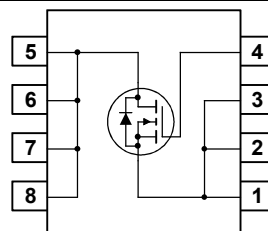
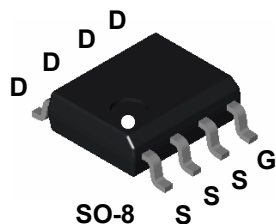
This device has been designed specifically to improve the efficiency of DC-DC converters. Using new techniques in MOSFET construction, the various components of gate charge and capacitance have been optimized to reduce switching losses. Low gate resistance and very low Miller charge enable excellent performance with both adaptive and fixed dead time gate drive circuits. Very low R<sub>ds(on)</sub> has been maintained to provide an extremely versatile device.

### Applications

- High Efficiency DC-DC Converters:
  - Notebook Vcore Power Supply
  - Telecom Brick Synchronous Rectifier
  - Multi purpose Point Of Load

### Features

- 21 A, 30 V      Max R<sub>DS(ON)</sub> = 3.7 mΩ @ V<sub>GS</sub> = 10 V  
                                  Max R<sub>DS(ON)</sub> = 5.0 mΩ @ V<sub>GS</sub> = 4.5 V
- High performance trench technology for extremely low R<sub>DS(ON)</sub> and gate charge
- Minimal Qgd (5.5 nC typical)
- 100% R<sub>θ</sub> tested (0.9 Ω typical)
- 100% UIL tested
- RoHS Compliant



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage	30	V
V <sub>GSS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Drain Current – Continuous (Note 1a)	21	A
	– Pulsed	105	
P <sub>D</sub>	Power Dissipation (Note 1a)	2.5	W
	(Note 1b)	1.2	
	(Note 1c)	1	
E <sub>AS</sub>	Single Pulse Avalanche Energy (Note 3)	433	mJ
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	25	

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS8670	FDS8670	13"	12mm	2500 units

## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

### Off Characteristics

$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		39		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate–Body Leakage	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	1.4	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-5		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10\text{ V}, I_D = 21\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 18\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 21\text{ A}, T_J = 125^\circ\text{C}$		3.3 4.2 4.4	3.7 5.0 5.5	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 21\text{ A}$		118		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		4040		pF
$C_{oss}$	Output Capacitance			1730		pF
$C_{riss}$	Reverse Transfer Capacitance			160		pF
$R_G$	Gate Resistance	$f = 1.0\text{ MHz}$	0.2	0.9	1.5	$\Omega$

### Switching Characteristics (Note 2)

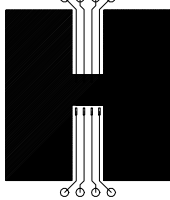
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		12	21	ns
$t_r$	Turn–On Rise Time			11	20	ns
$t_{d(off)}$	Turn–Off Delay Time			56	90	ns
$t_f$	Turn–Off Fall Time			68	108	ns
$Q_{g(TOT)}$	Total Gate Charge at $V_{GS} = 10\text{ V}$	$V_{DD} = 15\text{ V}, I_D = 21\text{ A}$		58.5	82	nC
$Q_{g(TOT)}$	Total Gate Charge at $V_{GS} = 5\text{ V}$			30	42	nC
$Q_{gs}$	Gate–Source Charge			9.5		nC
$Q_{gd}$	Gate–Drain Charge			5.5		nC

### Drain–Source Diode Characteristics and Maximum Ratings

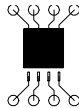
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.1\text{ A}$ (Note 2)		0.7	1.2	V
$t_{rr}$	Diode Reverse Recovery Time	$I_F = 21\text{ A},$ $di_F/dt = 100\text{ A}/\mu\text{s}$		51		ns
$I_{RM}$	Diode Reverse Recovery Current			1.5		A
$Q_{rr}$	Diode Reverse Recovery Charge			37		nC

#### Notes:

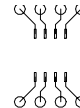
1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 50°/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b) 105°/W when mounted on a .04 in<sup>2</sup> pad of 2 oz copper



c) 125°/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

3. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 17\text{ A}$ ,  $V_{DD} = 30\text{ V}$ ,  $V_{GS} = 10\text{ V}$

## Typical Characteristics

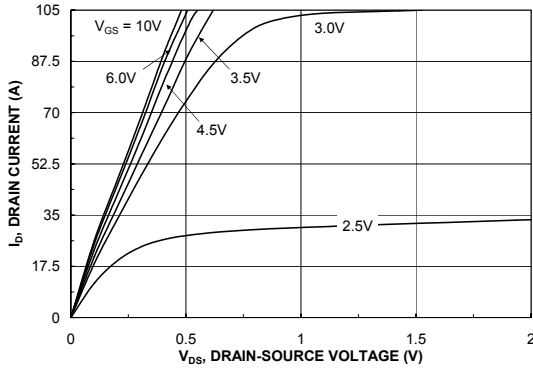


Figure 1. On-Region Characteristics.

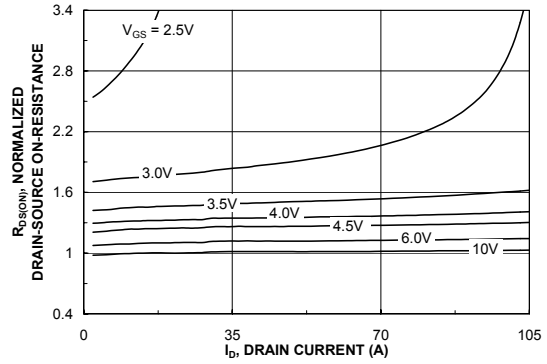


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

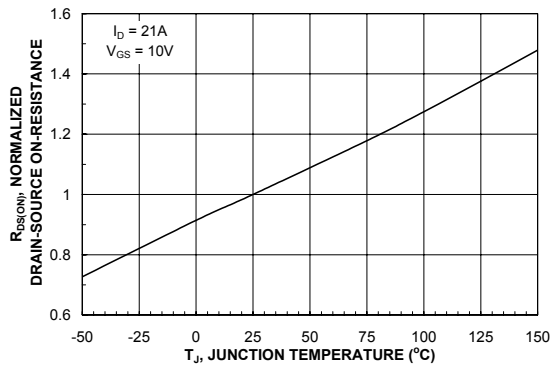


Figure 3. On-Resistance Variation with Temperature.

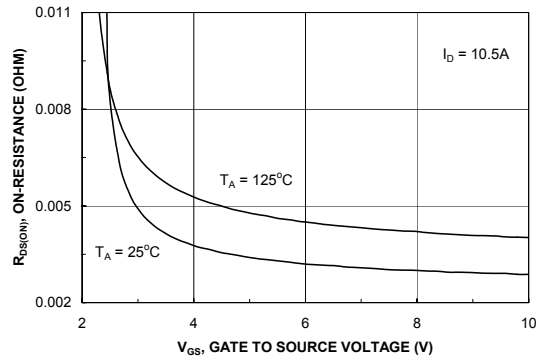


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

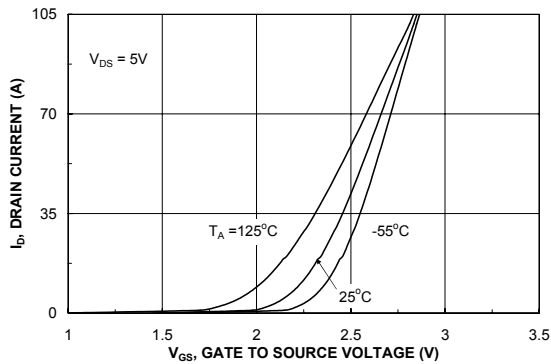


Figure 5. Transfer Characteristics.

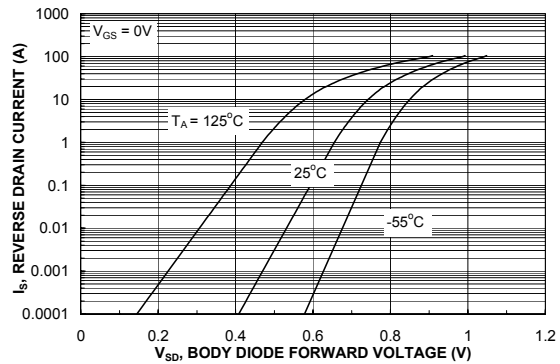
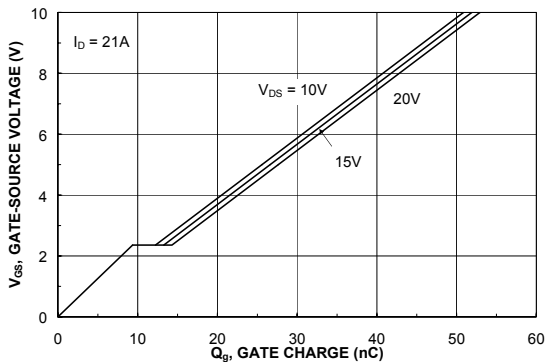
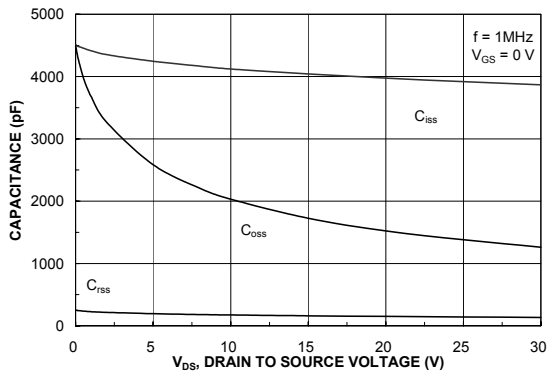


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

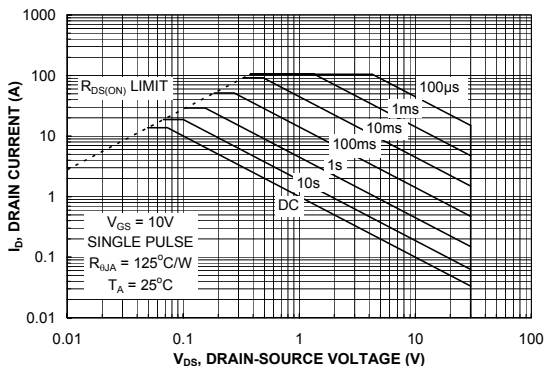
**Typical Characteristics** (continued)



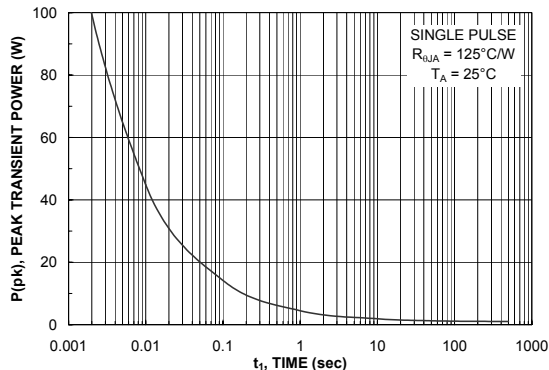
**Figure 7. Gate Charge Characteristics.**



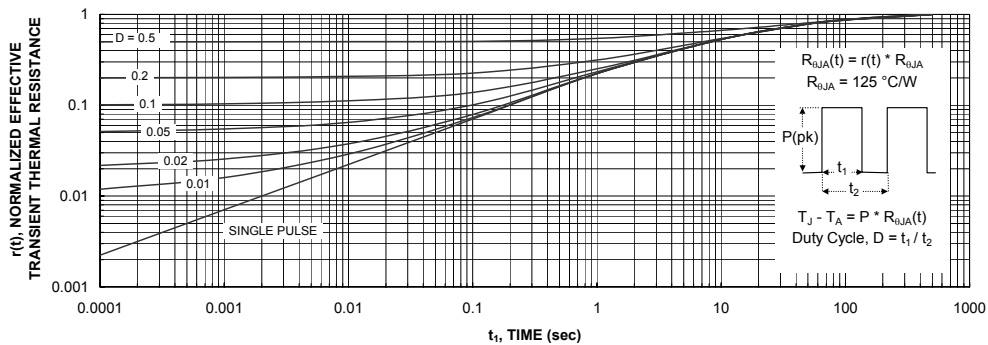
**Figure 8. Capacitance Characteristics.**



**Figure 9. Maximum Safe Operating Area.**



**Figure 10. Single Pulse Maximum Power Dissipation.**



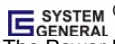


**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.



## TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

ACEx®	FPS™	PDP-SPM™	SupreMOS™
Build it Now™	FRFET®	Power220®	SyncFET™
CorePLUS™	Global Power Resource <sup>SM</sup>	POWEREDGE®	 SYSTEM GENERAL®
CROSSVOLT™	Green FPS™	Power-SPM™	The Power Franchise®
CTL™	Green FPS™ e-Series™	PowerTrench®	the <b>power</b> franchise
Current Transfer Logic™	GTO™	Programmable Active Droop™	TinyBoost™
EcoSPARK®	<i>i-Lo</i> ™	QFET®	TinyBuck™
EZSWITCH™ *	IntelliMAX™	QS™	TinyLogic®
 ™	ISOPLANAR™	QT Optoelectronics™	TINYOPTO™
<b>F</b> ™	MegaBuck™	Quiet Series™	TinyPower™
Fairchild®	MICROCOUPLER™	RapidConfigure™	TinyPWM™
Fairchild Semiconductor®	MicroFET™	SMART START™	TinyWire™
FACT Quiet Series™	MicroPak™	SPM®	µSerDes™
FACT®	MillerDrive™	STEALTH™	UHC®
FAST®	Motion-SPM™	SuperFET™	Ultra FRFET™
FastvCore™	OPTOLOGIC®	SuperSOT™-3	UniFET™
FlashWriter® *	OPTOPLANAR®	SuperSOT™-6	VCX™
	 ®	SuperSOT™-8	

\* EZSWITCH™ and FlashWriter® are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component in any component of a life support, device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.