FAIRCHILD

SEMICONDUCTOR®

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FDS7098N3

## 30V N-Channel PowerTrench® MOSFET

General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

Applications

- DC/DC converter
- Power management
- Load switch

Features

- 14 A, 30 V $R_{DS(ON)}$ = 9 mΩ @ V_{GS} = 10 V
  $R_{DS(ON)}$ = 12 mΩ @ V_{GS} = 4.5 V

- High performance trench technology for extremely low $R_{DS(ON)}$

- High power and current handling capability

- Fast switching

- FLMP SO-8 package: Enhanced thermal performance in industry-standard package size

FLMP SO-8

Pin 1

Bottom-side Drain Contact
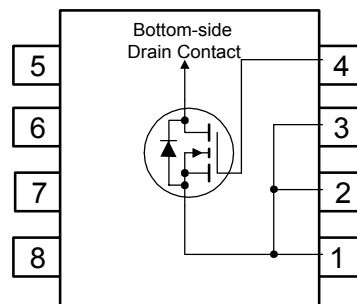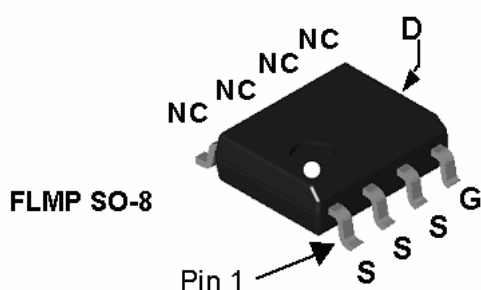
Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current – Continuous	(Note 1a)	14	A
	– Pulsed		60	
P_D	Power Dissipation for Single Operation	(Note 1a)	3.0	W
		(Note 1b)	1.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	40	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	0.5	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS7098N3	FDS7098N3	13''	12mm	2500 units

FDS7098N3 Rev C (W)

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		27		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			10	μA
I_{GSS}	Gate–Body Leakage	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		–6		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 10 V, I_D = 14 A V_{GS} = 4.5 V, I_D = 13 A V_{GS} = 10 V, I_D = 14 A,T_J = 125°C		7.5 9.5 11	9 12 14	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 14 A		62		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V,		1587		pF
C_{oss}	Output Capacitance	f = 1.0 MHz		385		pF
C_{rss}	Reverse Transfer Capacitance			154		pF
R_G	Gate Resistance	V_{GS} = 15 mV, f = 1.0 MHz		1.4		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 15 V, I_D = 1 A,		11	20	ns
t_r	Turn–On Rise Time	V_{GS} = 10 V, R_{GEN} = 6 Ω		13	23	ns
$t_{d(off)}$	Turn–Off Delay Time			27	43	ns
t_f	Turn–Off Fall Time			15	27	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 14 A,		16	22	nC
Q_{gs}	Gate–Source Charge	V_{GS} = 5.0 V		5		nC
Q_{gd}	Gate–Drain Charge			6		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				2.5	A
t_{RR}	Reverse Recovery Time	I_F = 14 A,		16		ns
Q_{RR}	Reverse Recovery Charge	d_{iF}/d_t = 100 A/μs (Note 2)		26		nC
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.5 A (Note 2)		0.7	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
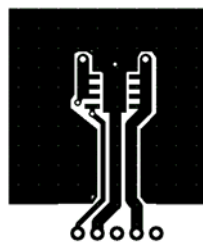
a) 40°C/W when mounted on a 1in² pad of 2 oz copper

b) 85°C/W when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%
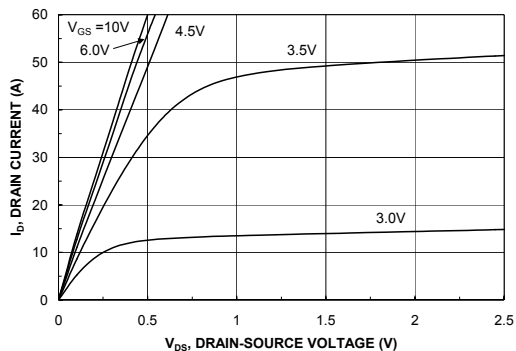
Typical Characteristics
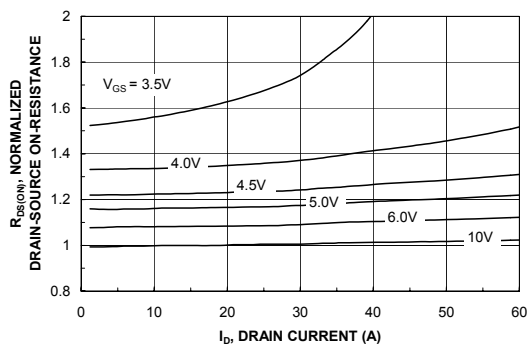

Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with
Drain Current and Gate Voltage.

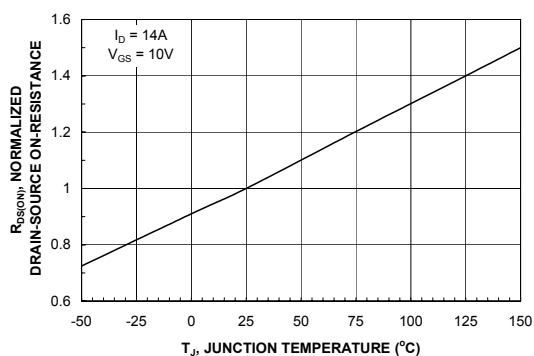Figure 3. On-Resistance Variation
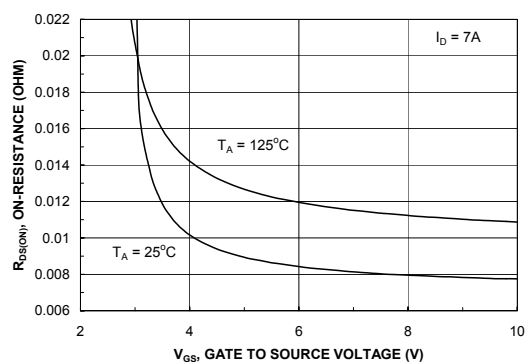withTemperature.

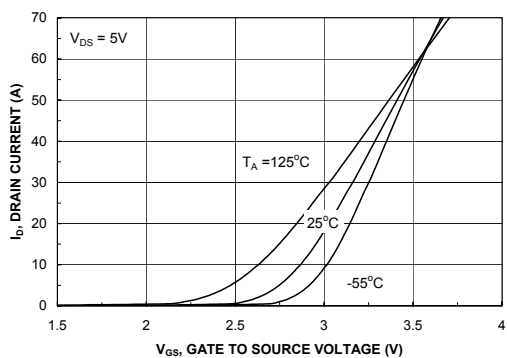Figure 4. On-Resistance Variation with
Gate-to-Source Voltage.

Figure 5. Transfer Characteristics.
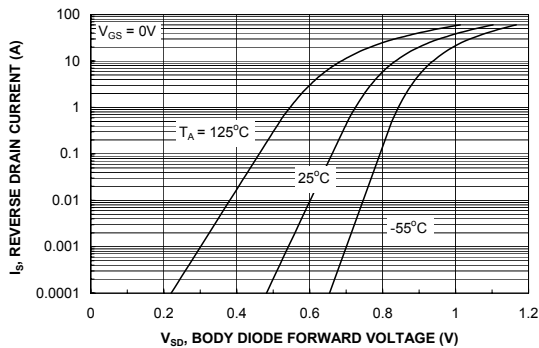

Figure 6. Body Diode Forward Voltage Variation
with Source Current and Temperature.
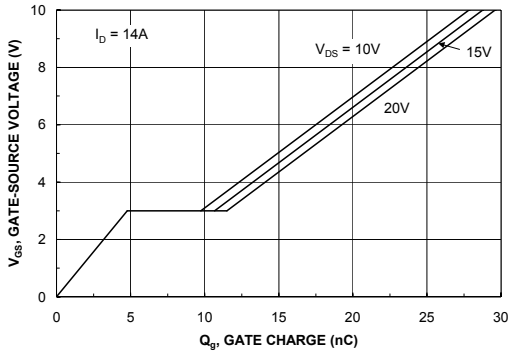
Typical Characteristics
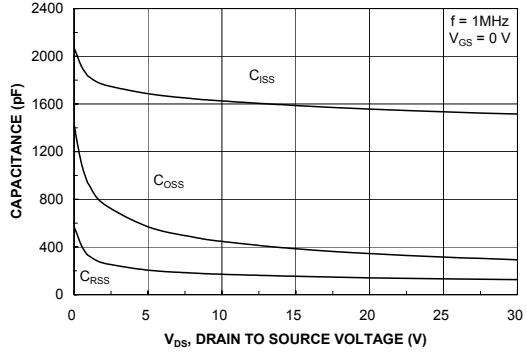

Figure 7. Gate Charge Characteristics.

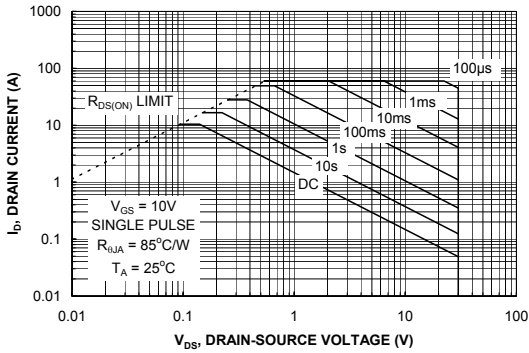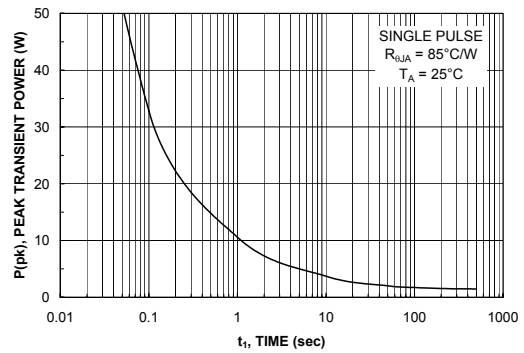Figure 8. Capacitance Characteristics.

Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum
Power Dissipation.

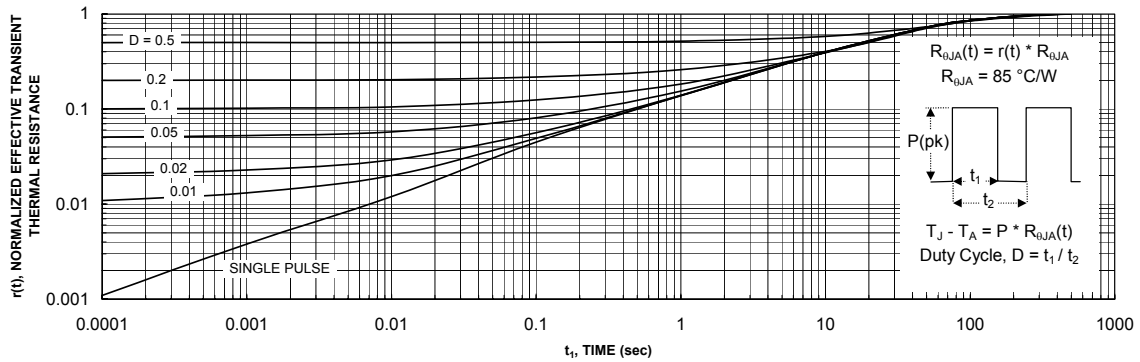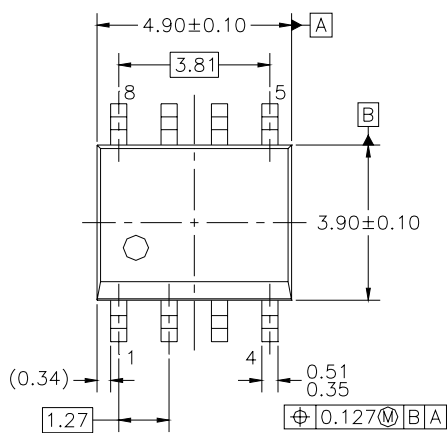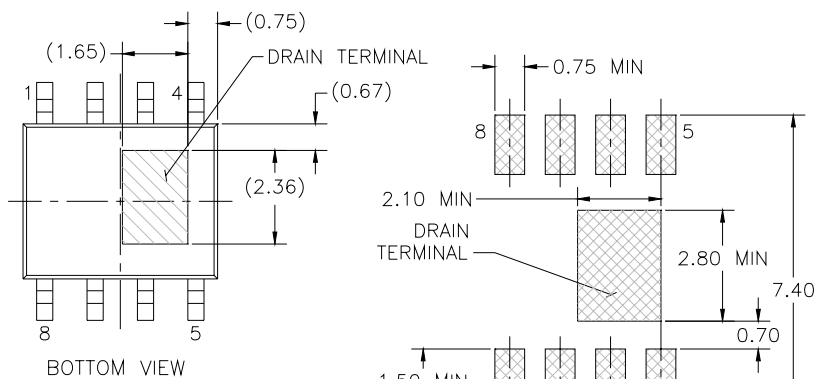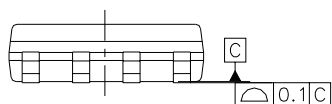Figure 11. Transient Thermal Response Curve.

**Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.**

Dimensional Outline and Pad Layout

(0.75)

(1.65)

DRAIN TERMINAL

1   4

(0.67)

(2.36)

8   5

BOTTOM VIEW

0.75 MIN

8   5

2.10 MIN

DRAIN
TERMINAL

2.80 MIN

7.40

0.70

1.50 MIN

1   4

1.27

3.81

LAND PATTERN RECOMMENDATION

4.90±0.10   ▶ A

3.81

8   5

B

3.90±0.10

1   4

(0.34)

0.51
0.35

1.27

⊕ 0.127 Ⓜ B A

C

⌒ 0.1 C

SEE DETAIL A

0.25
0.19

6.00±0.20

GAGE PLANE

0.50
0.25 X 45°

1.45 +0.05
     −0.20

0.36

1.60 MAX

0.10
0.00

8°
0°

0.90
0.50

SEATING PLANE

(1.04)
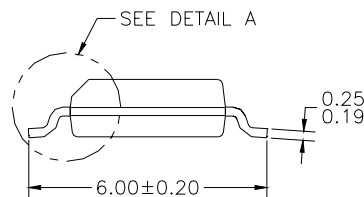
DETAIL A
SCALE: 24:1

NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) STANDARD LEAD FINISH:
     20−80 MICROINCHES NICKEL/
     6 MICROINCHES MAX. PALLADIUM
     AND GOLD FLASH.
C) NO JEDEC REGISTERED REFERENCE
     AS OF MARCH 2, 2000.

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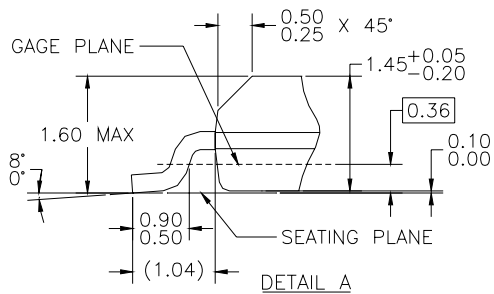The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

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EcoSPARK™	HiSeC™	MSX™	Quiet Series™	TINYOPTO™
E²CMOS™	I²C™	MSXPro™	RapidConfigure™	TruTranslation™
EnSigna™	i-Lo™	OCX™	RapidConnect™	UHC™
FACT™	ImpliedDisconnect™	OCXPro™	μSerDes™	UltraFET®
FACT Quiet Series™		OPTOLOGIC®	SILENT SWITCHER®	VCX™
Across the board. Around the world.™		OPTOPLANAR™	SMART START™	
The Power Franchise®		PACMAN™	SPM™	
Programmable Active Droop™		POP™	Stealth™	

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