FAIRCHILD SEMICONDUCTOR®

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FDS5692Z

N-Channel UltraFET Trench® MOSFET

50V, 5.8A, 24mΩ

General Description

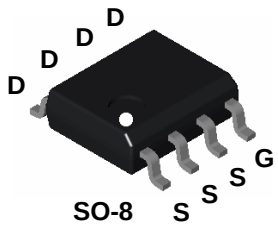
This N-Channel UltraFET device has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$ and fast switching speed.

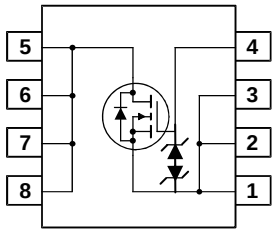
Applications

- DC/DC converter

Features

- Max $r_{DS(on)}$ = 24mΩ at V_{GS} = 10V, I_D = 5.8A
- Max $r_{DS(on)}$ = 33mΩ at V_{GS} = 4.5V, I_D = 5.6A
- ESD protection diode (note 3)
- Low Qgd
- Fast switching speed





MOSFET Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DS}	Drain-Source Voltage		50	V
V_{GS}	Gate-Source Voltage		± 20	V
I_D	Drain Current – Continuous	(Note 1a)	5.8	A
	– Pulsed		40	
E_{AS}	Single Pulse Avalanche Energy		72	mJ
P_D	UltraFET Dissipation for Single Operation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1.1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to 150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1c)	125	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape width	Quantity
FDS5692Z	FDS5692Z	SO-8	13”	12mm	2500units

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Ratings						
E_{AS}	Drain-Source Avalanche Energy (Single Pulse)	V_{DD} = 50 V, I_D= 12 A, L=1mH			72	mJ
I_{AS}	Drain-Source Avalanche Current			12		A
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	50			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		48		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 40 V V_{GS} = 0 V			1	μA
I_{GSS}	Gate–Body Leakage	V_{GS} = ± 20V, V_{DS} = 0 V			± 10	μA
On Characteristics (Note 4)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	1	1.6	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		–6		mV/°C
$r_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 10 V, I_D = 5.8 A V_{GS} = 4.5 V, I_D = 5.6 A V_{GS} = 10 V, I_D = 5.8A, T_J = 125°C		20 26 32	24 33 41	mΩ
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		1025		pF
C_{oss}	Output Capacitance			150		pF
C_{rss}	Reverse Transfer Capacitance			50		pF
R_G	Gate Resistance	f = 1.0 MHz		0.79		Ω
$Q_{g(TOT)}$	Total Gate Charge, V_{GS} = 10V	V_{DS} = 25V, I_D = 5.8A		18	25	nC
$Q_{g(TOT)}$	Total Gate Charge, V_{GS} = 5V			10	14	nC
Q_{gs}	Gate–Source Gate Charge			2.8		nC
Q_{gd}	Gate–Drain Gate Charge			3.0		nC
Switching Characteristics (Note 4)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 25 V, I_D = 5.8A, V_{GS} = 10 V, R_{GEN} = 6 Ω		9	18	ns
t_r	Rise Time			5	10	ns
$t_{d(off)}$	Turn–Off Delay Time			27	43	ns
t_f	Fall Time			6	12	ns

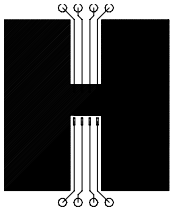
Electrical Characteristics

T_A = 25°C unless otherwise noted

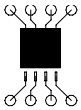
Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
Drain–Source Diode Characteristics							
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V,	I_S = 5.8 A		0.79	1.25	V
			I_S = 2.9 A		0.75	1.0	V
t_{rr}	Reverse Recovery Time	I_F = 6A, dI_F/dt = 100A/µs			24		ns
Q_{rr}	Reverse Recovery Charge				16		nC

Notes:

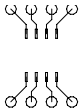
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1in^2 pad of 2 oz copper



b) 105°C/W when mounted on a .04 in^2 pad of 2 oz copper



c) 125°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics

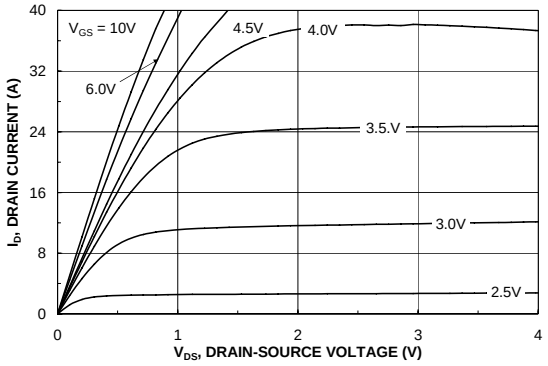


Figure 1. On-Region Characteristics.

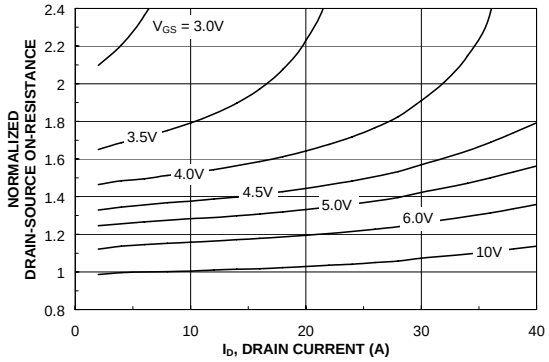


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

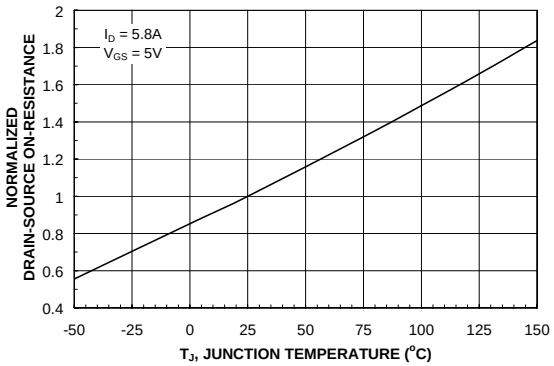


Figure 3. On-Resistance Variation with Temperature.

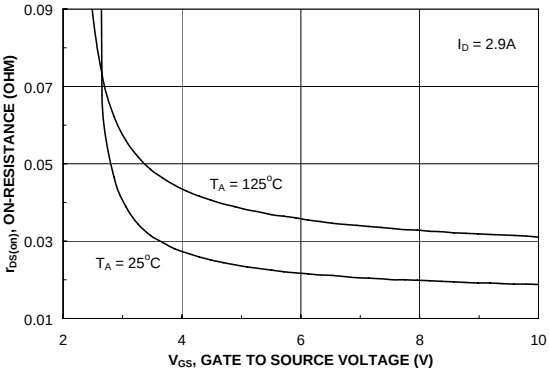


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

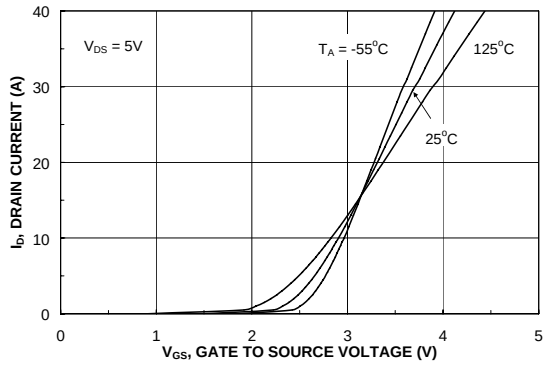


Figure 5. Transfer Characteristics.

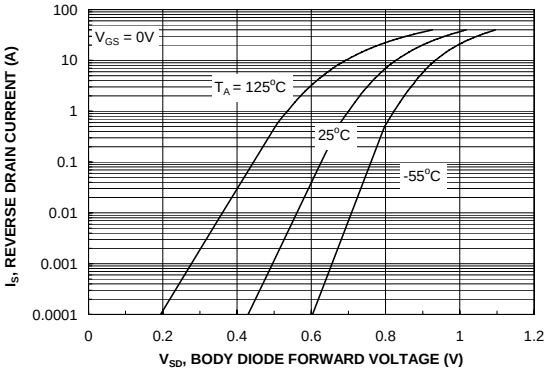


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

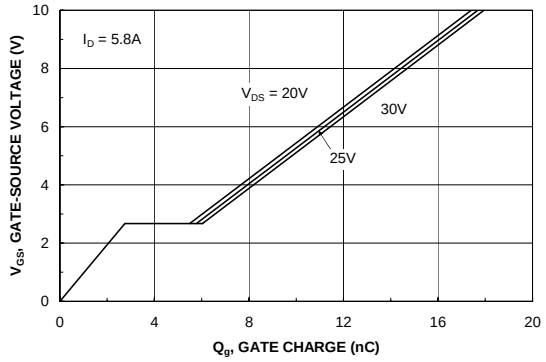


Figure 7. Gate Charge Characteristics.

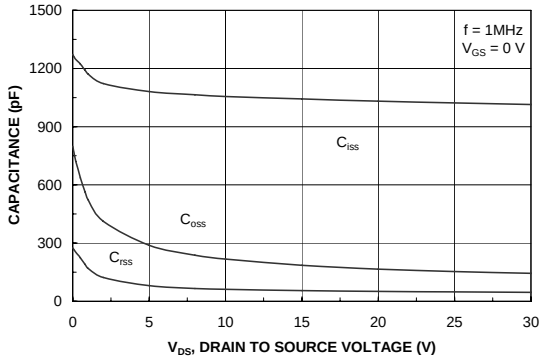


Figure 8. Capacitance Characteristics.

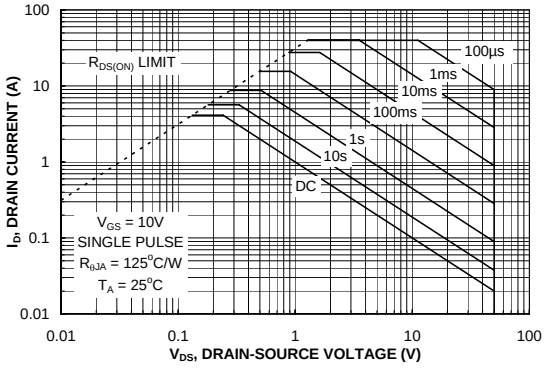


Figure 9. Maximum Safe Operating Area.

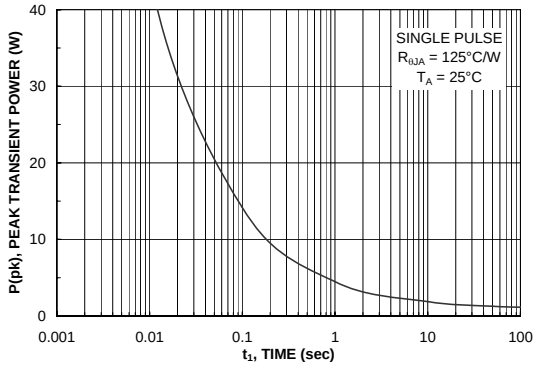


Figure 10. Single Pulse Maximum UltraFET Dissipation.

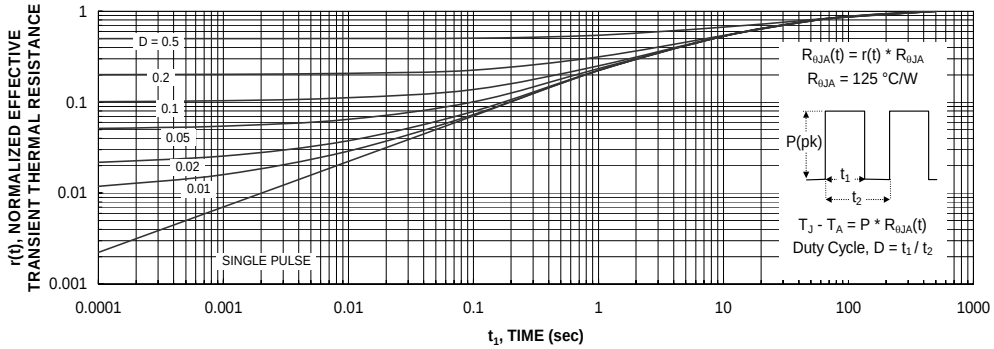


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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