

FDR858P

Single P-Channel, Logic Level, PowerTrench™ MOSFET

General Description

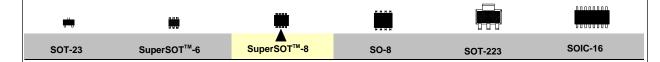
The SuperSOT-8 family of P-Channel Logic Level MOSFETs have been designed to provide a low profile, small footprint alternative to industry standard SO-8 little foot type product.

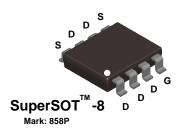
This P-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

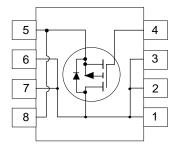
These devices are well suited for notebook computer applications: load switching and power management, battery charging circuits, and DC/DC conversion.

Features

- -8 A, -30 V. $R_{DS(ON)}$ = 0.019 Ω @ V_{GS} = -10 V, $R_{DS(ON)}$ = 0.028 Ω @ V_{GS} = -4.5 V.
- Low gate charge (21nC typical).
- High performance trench technology for extremely low R_{DS/ONI}.
- SuperSOTTM-8 package: small footprint (40%) less than SO-8); low profile (1mm thick); maximum power comperable to SO-8.







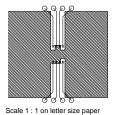
Absolute Maximum Ratings T_a = 25°C unless otherwise noted

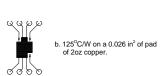
Symbol	Parameter	Ra	atings Units
V _{DSS}	Drain-Source Voltage		-30 V
V_{GSS}	Gate-Source Voltage		±20 V
I _D	Draint Current - Continuous (Not	÷ 1)	-8 A
	- Pulsed		-50
P _D	Maximum Power Dissipation (Note	1a)	1.8 W
	(Note	1b)	1
	(Note	1c)	0.9
T_J , T_{STG}	Operating and Storage Temperature Range	-55	to 150 °C
THERMA	L CHARACTERISTICS		
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (No	e 1a)	70 °C/W
R _{eJC}	Thermal Resistance, Junction-to-Case (Not	e 1)	20 °C/W

Symbol	Parameter	Min	Тур	Max	Units	
OFF CHAR	ACTERISTICS					
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$	-30			V
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient	I _D =-50 μA, Referenced to 25 °C		-22		mV /°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24 \text{ V}, \ V_{GS} = 0 \text{ V}$			-1	μA
		T _J = 55°C			-10	μA
I _{GSS}	Gate - Body Leakage Current	$V_{GS} = 20 \text{ V}, \ V_{DS} = 0 \text{ V}$			100	nA
I _{GSS}	Gate - Body Leakage, Reverse	$V_{GS} = -20 \text{ V}, \ V_{DS} = 0 \text{ V}$			-100	nA
ON CHARAC	CTERISTICS (Note 2)	<u> </u>	•		·	
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$	-1	-1.7	-3	V
$\Delta V_{GS(th)}/\Delta T_{J}$	Gate Threshold Voltage Temp.Coefficient	I _D =-50 μA, Referenced to 25 °C		4		mV /°C
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = -10 \text{ V}, I_{D} = -8 \text{ A}$		0.0155	0.019	Ω
. ,		T _J = 125°C		0.021	0.03	1
		$V_{GS} = -4.5 \text{ V}, I_{D} = -6.3 \text{ A}$		0.022	0.028	1
I _{D(ON)}	On-State Drain Current	$V_{GS} = -10 \text{ V}, \ V_{DS} = -5 \text{ V}$	-50			Α
g _{FS}	Forward Transconductance	$V_{DS} = -10 \text{ V}, I_{D} = -3.2 \text{ A}$		25		S
DYNAMIC C	HARACTERISTICS					
C _{iss}	Input Capacitance	$V_{DS} = -15 \text{ V}, \ V_{GS} = 0 \text{ V},$ f = 1.0 MHz		2010		pF
C _{oss}	Output Capacitance	f = 1.0 MHz		590		pF
C _{rss}	Reverse Transfer Capacitance	se Transfer Capacitance				
SWITCHING	CHARACTERISTICS (Note 2)					
t _{D(on)}	Turn - On Delay Time	$V_{DD} = -15 \text{ V}, \ I_{D} = -1 \text{ A},$		12	22	ns
t,	Turn - On Rise Time		15	27	ns	
t _{D(off)}	Turn - Off Delay Time			100	140	ns
t _r	Turn - Off Fall Time			55	80	ns
Q_g	Total Gate Charge	$V_{DS} = -15 \text{ V}, I_{D} = -8 \text{ A},$		21	30	nC
Q_{gs}	Gate-Source Charge	$V_{GS} = 5 V$		6		nC
Q_{gd}	Gate-Drain Charge			8		nC
DRAIN-SO	URCE DIODE CHARACTERISTICS AND N	IAXIMUM RATINGS				
l _s	Maximum Continuous Drain-Source Diode F	Forward Current			-0.67	А
V _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -0.67 \text{ A} \text{ (Note 2)}$		-0.7	-1.2	V

Notes:

^{1.} R_{gas} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{gas} is guaranteed by design while $\boldsymbol{R}_{\text{\tiny BCA}}$ is determined by the user's board design.







2. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%.

Typical Electrical Characteristics

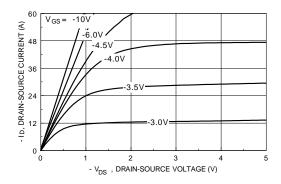


Figure 1. On-Region Characteristics.

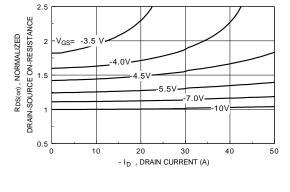


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

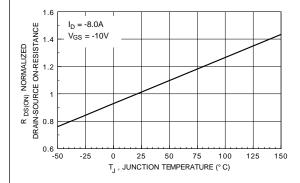


Figure 3. On-Resistance Variation with Temperature.

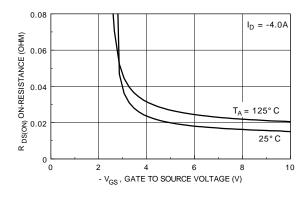


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

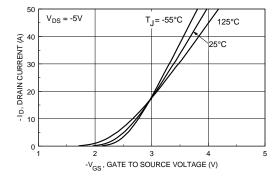


Figure 5. Transfer Characteristics.

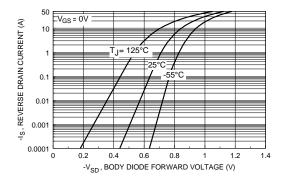


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics (continued)

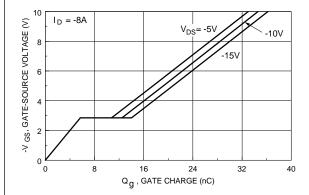


Figure 7. Gate Charge Characteristics.

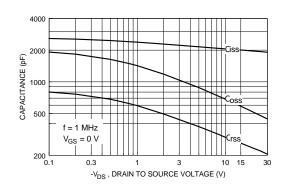


Figure 8. Capacitance Characteristics.

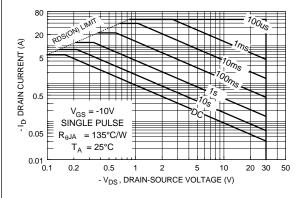


Figure 9. Maximum Safe Operating Area.

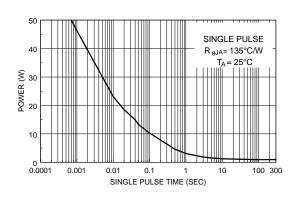


Figure 10. Single Pulse Maximum Power Dissipation.

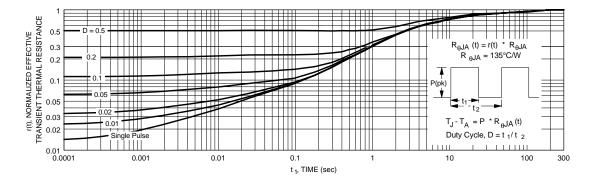
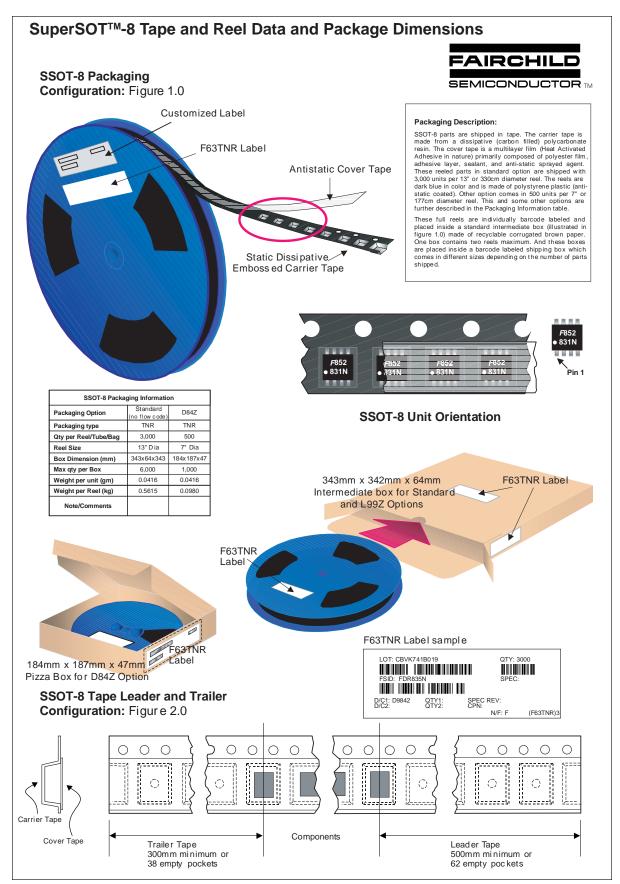
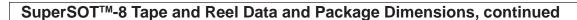


Figure 11. Transient Thermal Response Curve.

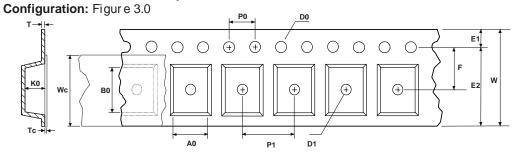
Thermal characterization performed using the conditions described in note 1c.

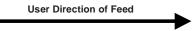
Transient thermal response will change depending on the circuit board design.





SSOT-8 Embossed Carrier Tape



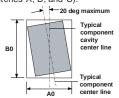


Dimensions are in millimeter														
Pkg type	A0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	Т	Wc	Тс
SSOT-8 (12mm)	4.47 +/-0.10	5.00 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.50 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	1.37 +/-0.10	0.280 +/-0.150	9.5 +/-0.025	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation

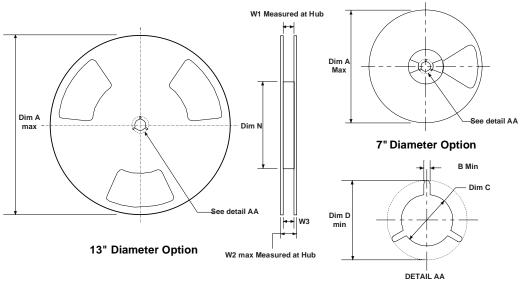


Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

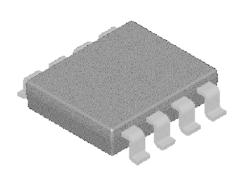
SSOT-8 Reel Configuration: Figur e 4.0

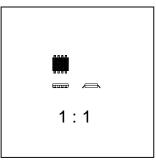


	Dimensions are in inches and millimeters								
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	5.906 150	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4

SuperSOT™-8 Tape and Reel Data and Package Dimensions, continued

SuperSOT™-8 (FS PKG Code 34, 35)

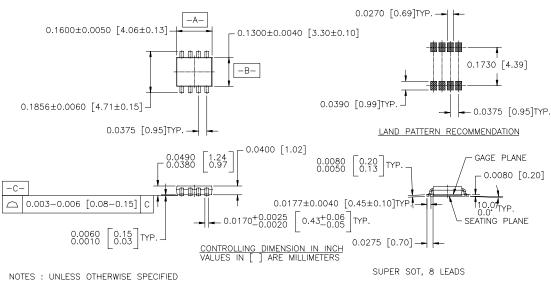




Scale 1:1 on letter size paper

Dimensions shown below are in: inches [millimeters]

Part Weight per unit (gram): 0.0416



STANDARD LEAD FINISH TI BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM TIN/LEAD (SOLDER) ON COPPER.

2. NO JEDEC REGISTRATION AS JAN. 1996

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 E^2CMOS^{TM} PowerTrenchTM

FACT™ QFET™ FACT Quiet Series™ QS™

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