

# FDP15N65 / FDPF15N65

## 650V N-Channel MOSFET

### Features

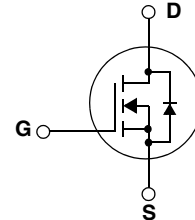
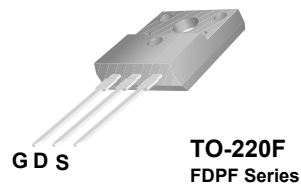
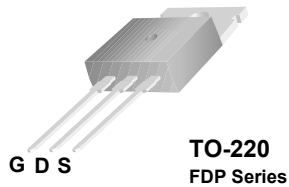
- 15A, 650V,  $R_{DS(on)} = 0.44\Omega @ V_{GS} = 10V$
- Low gate charge ( typical 48.5 nC)
- Low  $C_{rss}$  ( typical 23.6 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



### Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.



### Absolute Maximum Ratings

Symbol	Parameter	FDP15N65	FDPF15N65	Unit
$V_{DSS}$	Drain-Source Voltage	650		V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	15	15*
		- Continuous ( $T_C = 100^\circ\text{C}$ )	9.5	9.5*
$I_{DM}$	Drain Current - Pulsed (Note 1)	60	60*	A
$V_{GSS}$	Gate-Source voltage	$\pm 30$		V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	637		mJ
$I_{AR}$	Avalanche Current (Note 1)	15		A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	25.0		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	250	38.5	W
		2.0	0.3	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300		$^\circ\text{C}$

\* Drain current limited by maximum junction temperature.

### Thermal Characteristics

Symbol	Parameter	FDP15N65	FDPF15N65	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.5	3.3	$^\circ\text{C/W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink	0.5	--	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	$^\circ\text{C/W}$

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP15N65	FDP15N65	TO-220	--	--	50
FDPF15N65	FDPF15N65	TO-220F	--	--	50

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted

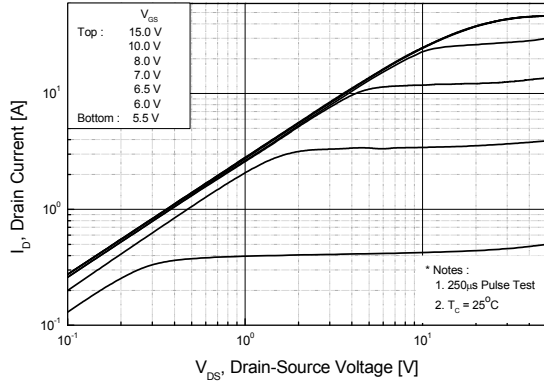
Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA, T <sub>J</sub> = 25°C	650	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, Referenced to 25°C	--	0.65	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 650V, V <sub>GS</sub> = 0V V <sub>DS</sub> = 520V, T <sub>C</sub> = 125°C	--	--	1 10	μA μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30V, V <sub>DS</sub> = 0V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30V, V <sub>DS</sub> = 0V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	3.0	--	5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 7.5A	--	0.36	0.44	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40V, I <sub>D</sub> = 7.5A (Note 4)	--	19.2	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1.0MHz	--	2380	3095	pF
C <sub>oss</sub>	Output Capacitance		--	295	385	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	23.6	35.5	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 325V, I <sub>D</sub> = 15A R <sub>G</sub> = 21.7Ω  (Note 4, 5)	--	65	140	ns
t <sub>r</sub>	Turn-On Rise Time		--	125	260	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	105	220	ns
t <sub>f</sub>	Turn-Off Fall Time		--	65	140	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 520V, I <sub>D</sub> = 15A V <sub>GS</sub> = 10V  (Note 4, 5)	--	48.5	63.0	nC
Q <sub>gs</sub>	Gate-Source Charge		--	14.0	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	21.2	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	15	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	60	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = 15A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>S</sub> = 15A di/dt = 100A/μs (Note 4)	--	496	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	5.69	--	μC

### NOTES:

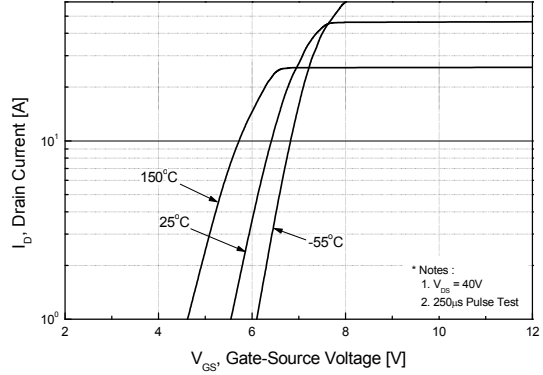
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 5.23mH, I<sub>AS</sub> = 15A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25Ω, Starting T<sub>J</sub> = 25°C
3. I<sub>SD</sub> ≤ 15A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25°C
4. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

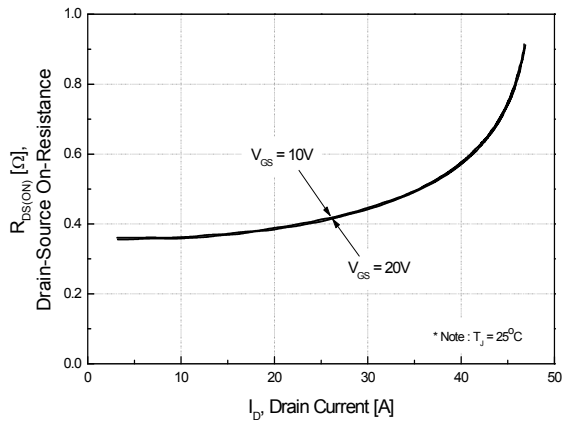
**Figure 1. On-Region Characteristics**



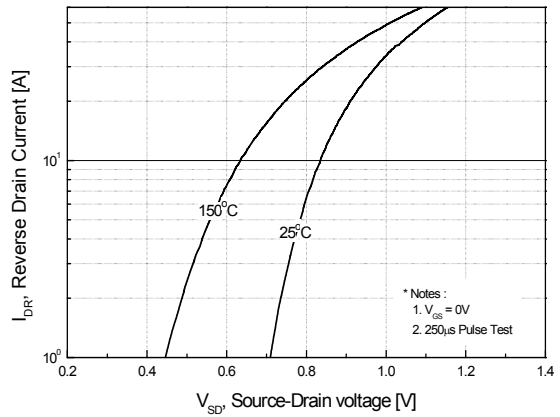
**Figure 2. Transfer Characteristics**



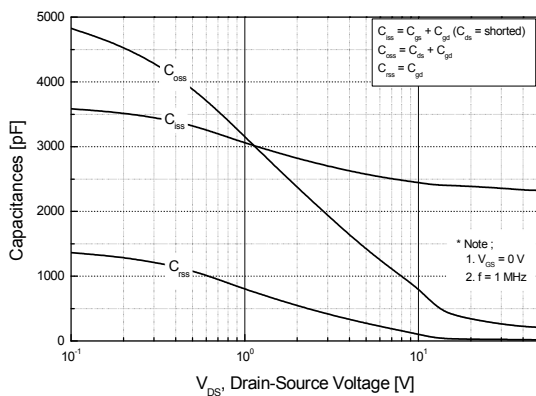
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



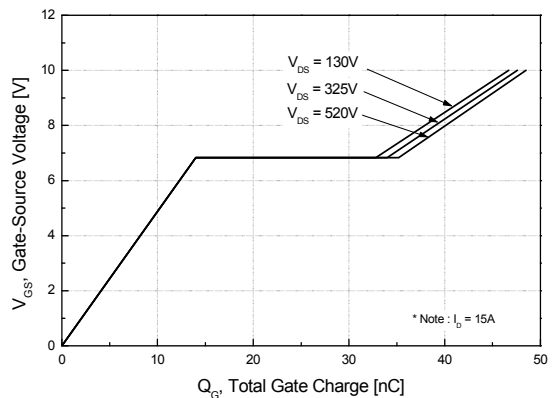
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

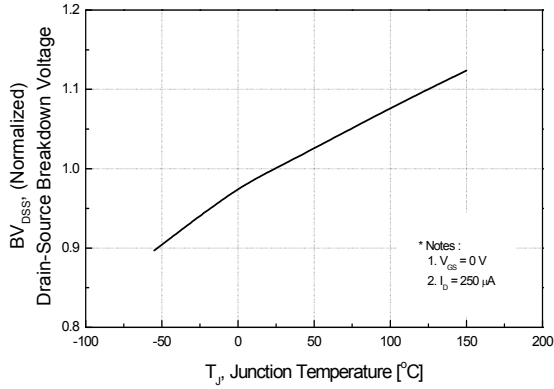


**Figure 6. Gate Charge Characteristics**

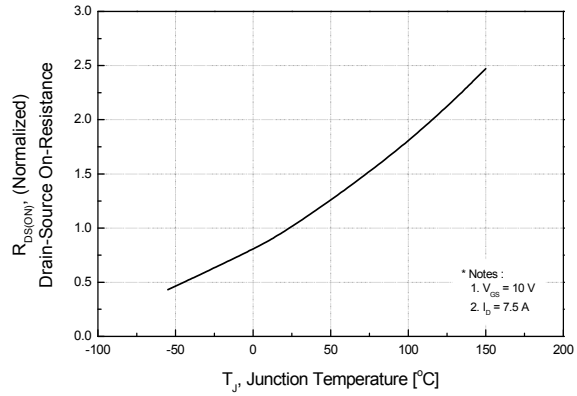


**Typical Performance Characteristics (Continued)**

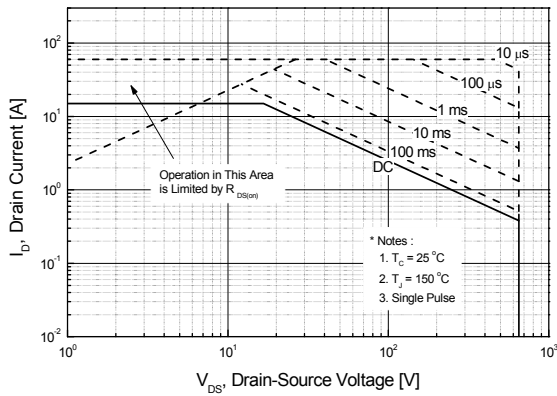
**Figure 7. Breakdown Voltage Variation vs. Temperature**



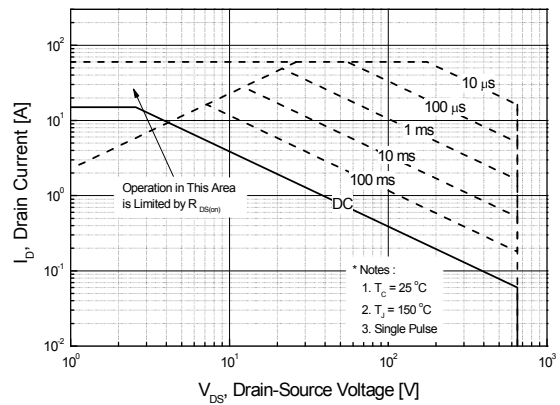
**Figure 8. On-Resistance Variation vs. Temperature**



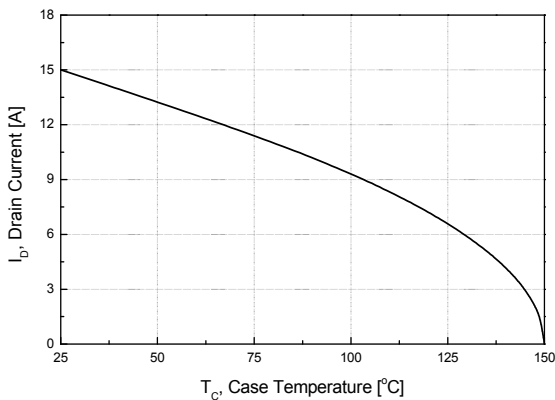
**Figure 9-1. Safe Operating Area for FDP15N65**



**Figure 9-2. Safe Operating Area for FDPF15N65**

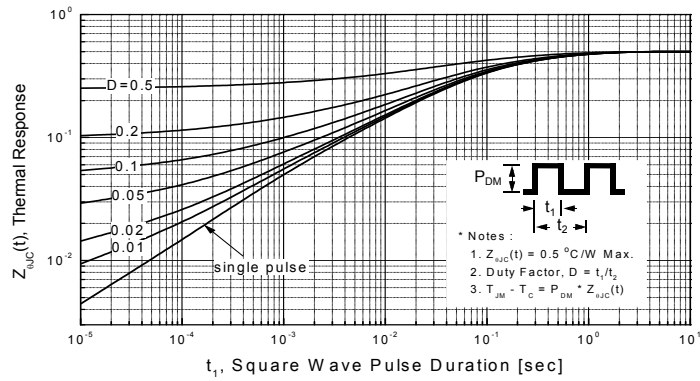


**Figure 10. Maximum Drain Current vs. Case Temperature**

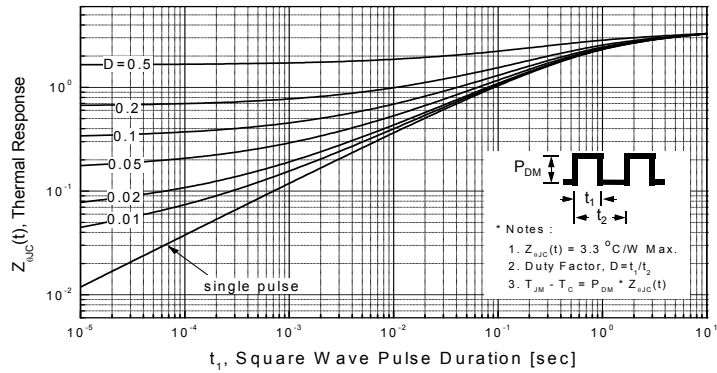


**Typical Performance Characteristics (Continued)**

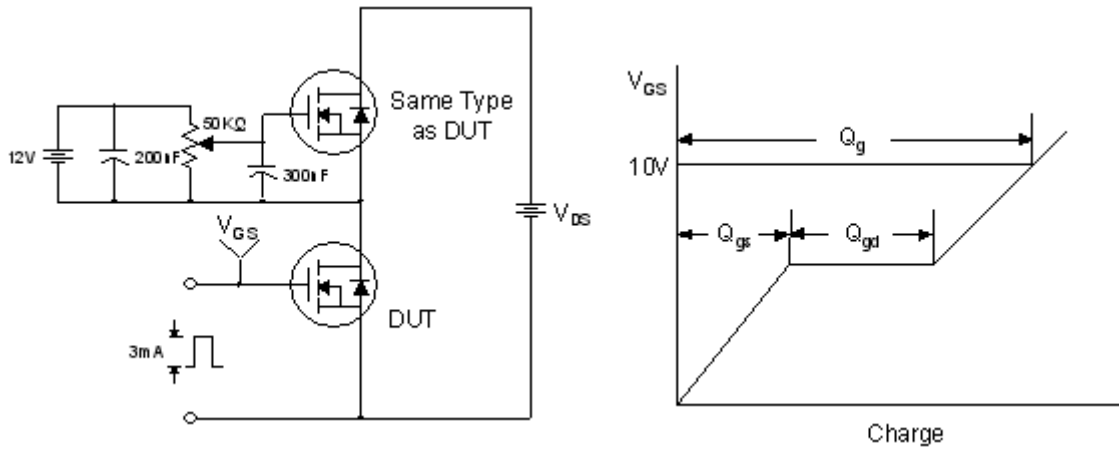
**Figure 11-1. Transient Thermal Response Curve for FDP15N65**



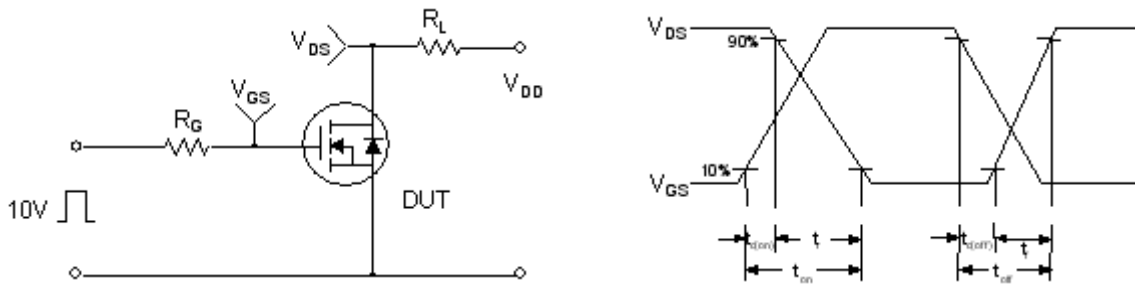
**Figure 11-2. Transient Thermal Response Curve for FDPF15N65**



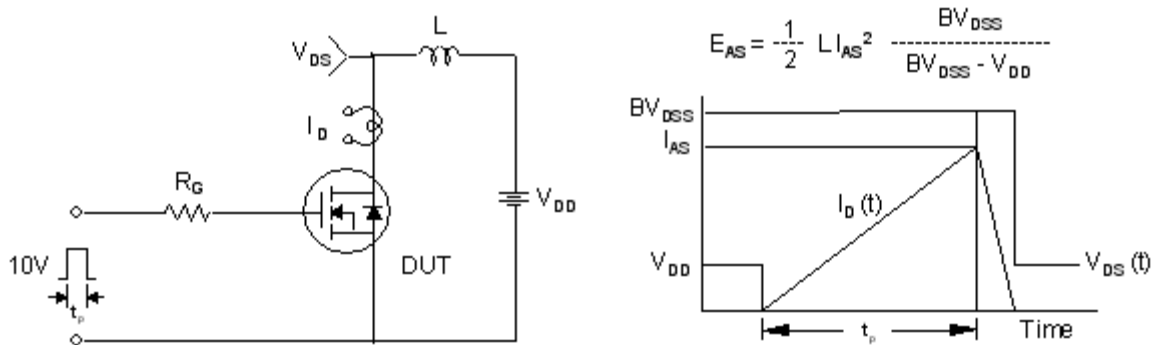
**Gate Charge Test Circuit & Waveform**



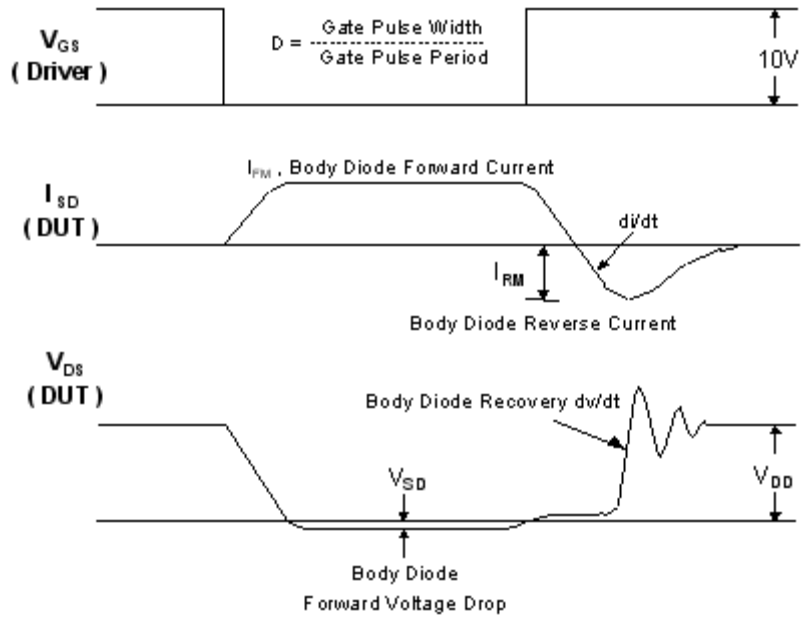
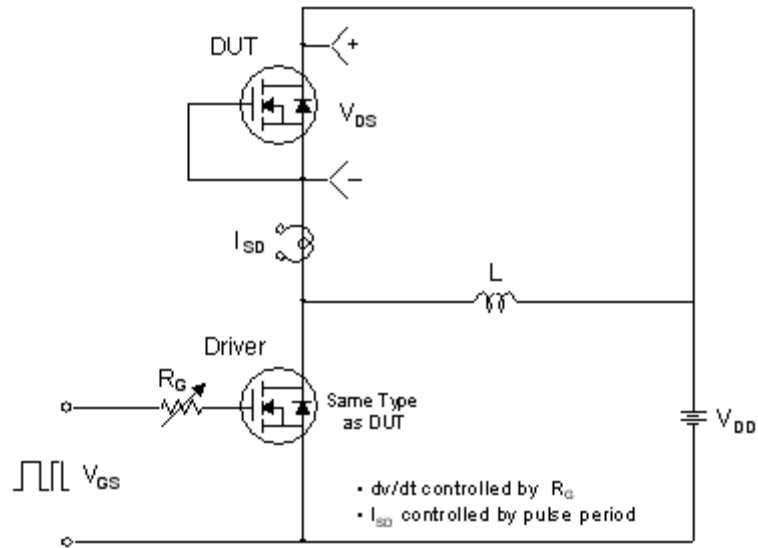
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

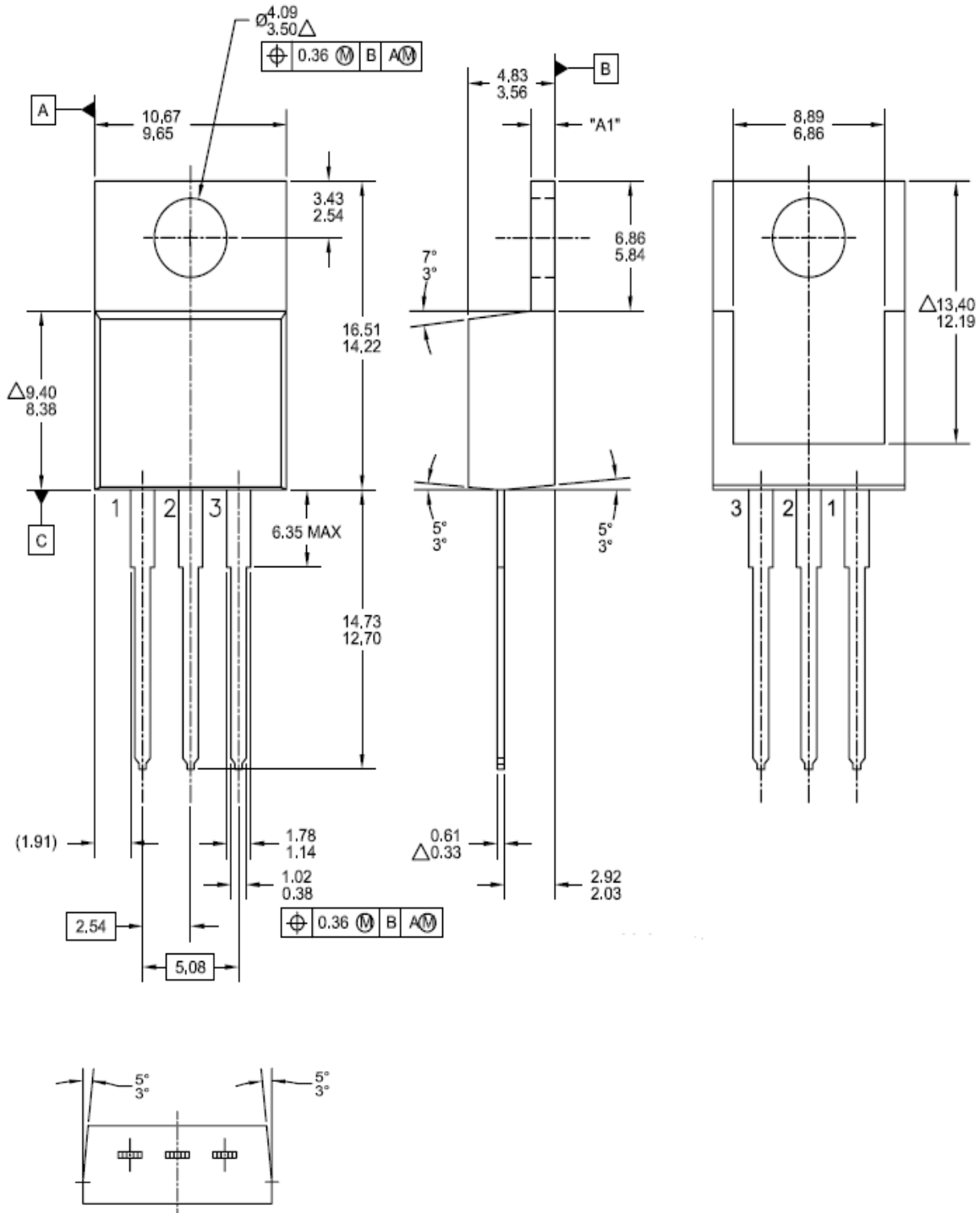


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

TO - 220

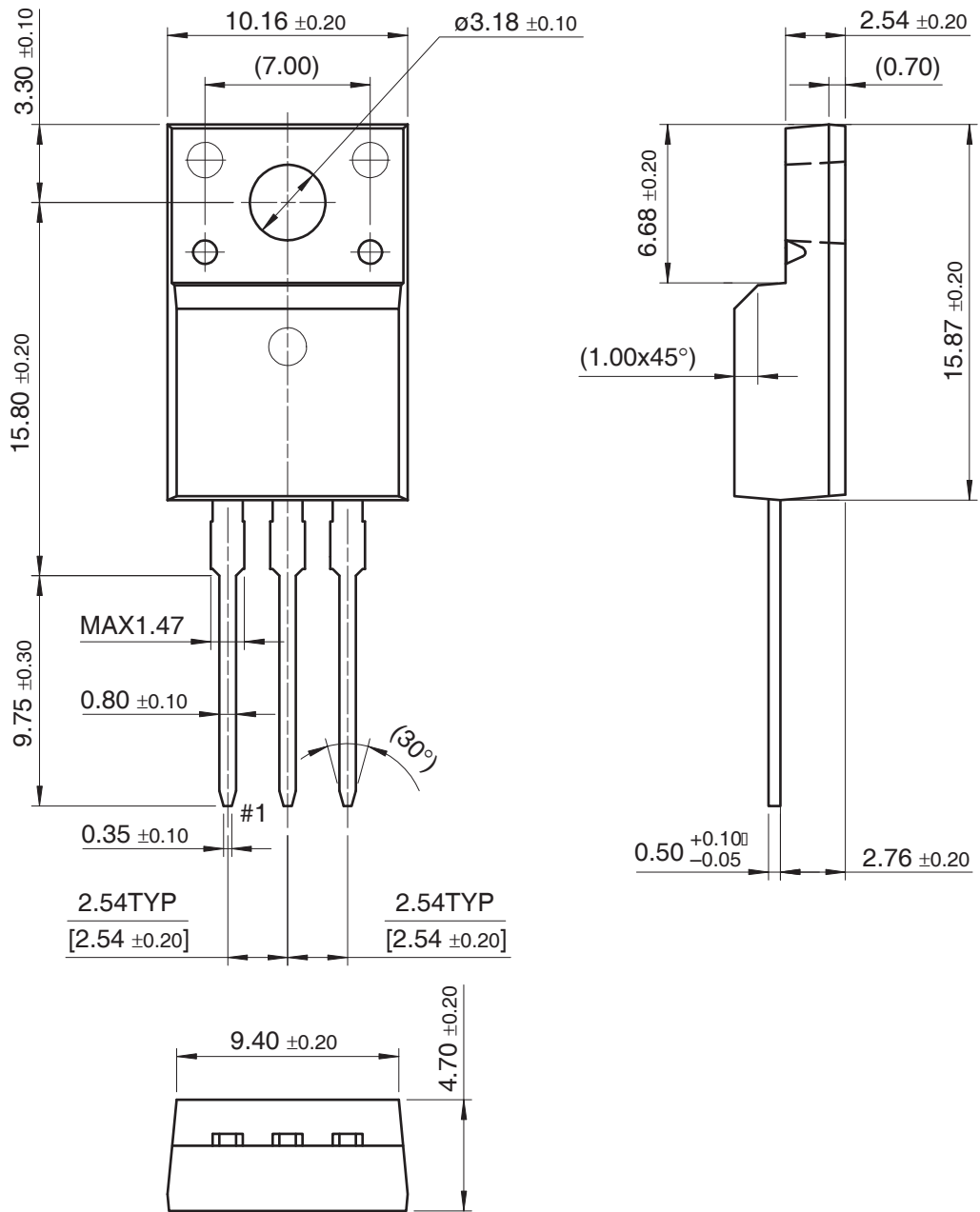


Dimensions in Millimeters



Mechanical Dimensions (Continued)

TO-220F




Dimensions in Millimeters



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