

FDMS8672S

N-Channel PowerTrench® SyncFET™

30V, 35A, 5mΩ

Features

- Max $r_{DS(on)}$ = 5.0mΩ at $V_{GS} = 10V, I_D = 17A$
- Max $r_{DS(on)}$ = 7.0mΩ at $V_{GS} = 4.5V, I_D = 15A$
- Advanced Package and Silicon combination for low $r_{DS(on)}$ and high efficiency
- SyncFET Schottky Body Diode
- MSL1 robust package design
- RoHS Compliant

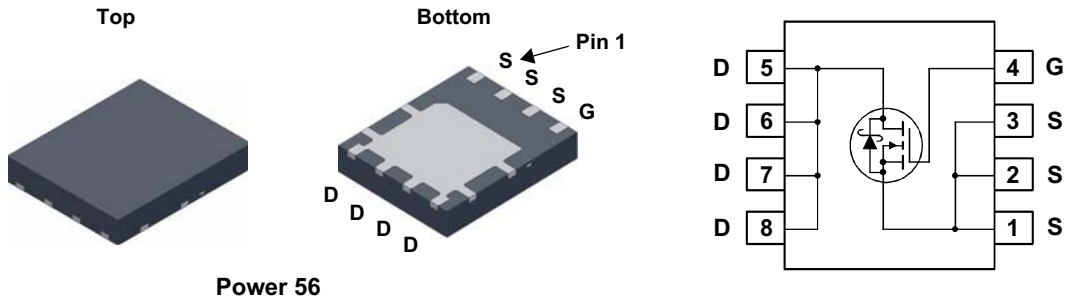


General Description

The FDMS8672S has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance. This device has the added benefit of an efficient monolithic Schottky body diode.

Application

- Synchronous Rectifier for DC/DC Converters
- Notebook Vcore/ GPU low side switch
- Networking Point of Load low side switch
- Telecom secondary side rectification



MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous (Package limited) $T_C = 25^\circ C$	35	A
	-Continuous (Silicon limited) $T_C = 25^\circ C$	90	
	-Continuous $T_A = 25^\circ C$	17	
	-Pulsed	200	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	337	mJ
P_D	Power Dissipation $T_C = 25^\circ C$	50	W
	Power Dissipation $T_A = 25^\circ C$ (Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ C$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.5	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS8672S	FDMS8672S	Power 56	13"	12mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 1\text{mA}, V_{GS} = 0\text{V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 50\text{mA}$, referenced to 25°C		23		$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}, V_{GS} = 0\text{V}$			500	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 1\text{mA}$	1	1.5	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 50\text{mA}$, referenced to 25°C		-5.4		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 17\text{A}$		4.0	5.0	m Ω
		$V_{GS} = 4.5\text{V}, I_D = 15\text{A}$		5.2	7.0	
		$V_{GS} = 10\text{V}, I_D = 17\text{A}, T_J = 125^\circ\text{C}$		6.1	7.8	
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{V}, I_D = 17\text{A}$		72		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$		1890	2515	pF
C_{oss}	Output Capacitance			555	740	pF
C_{rss}	Reverse Transfer Capacitance			205	380	pF
R_g	Gate Resistance	$f = 1\text{MHz}$		1.1		Ω

Switching Characteristics

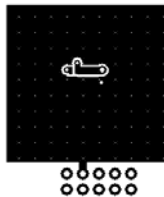
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{V}, I_D = 17\text{A}$ $V_{GS} = 10\text{V}, R_{GEN} = 7\Omega$		11	20	ns	
t_r	Rise Time			17	31	ns	
$t_{d(off)}$	Turn-Off Delay Time			27	44	ns	
t_f	Fall Time			7	14	ns	
$Q_{g(TOT)}$	Total Gate Charge at 10V		$V_{GS} = 0\text{V}$ to 10V		33	47	nC
$Q_{g(4.5V)}$	Total Gate Charge at 4.5V	$V_{GS} = 0\text{V}$ to 4.5V	$V_{DD} = 15\text{V},$ $I_D = 17\text{A}$		16	23	nC
Q_{gs}	Gate to Source Gate Charge				5		nC
Q_{gd}	Gate to Drain "Miller" Charge				6		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 1.7\text{A}$		0.4	0.7	V
t_{rr}	Reverse Recovery Time	$I_F = 17\text{A}, di/dt = 300\text{A}/\mu\text{s}$		20	32	ns
Q_{rr}	Reverse Recovery Charge			16	28	nC

Notes:

1: $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $50^\circ\text{C}/\text{W}$ when mounted on a 1in^2 pad of 2 oz copper



b. $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

2: Pulse time $< 300\mu\text{s}$, Duty cycle $< 2.0\%$.

3: Starting $T_J = 25^\circ\text{C}$, $L = 3\text{mH}$, $I_{AS} = 15\text{A}$, $V_{DD} = 30\text{V}$, $V_{GS} = 10\text{V}$.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

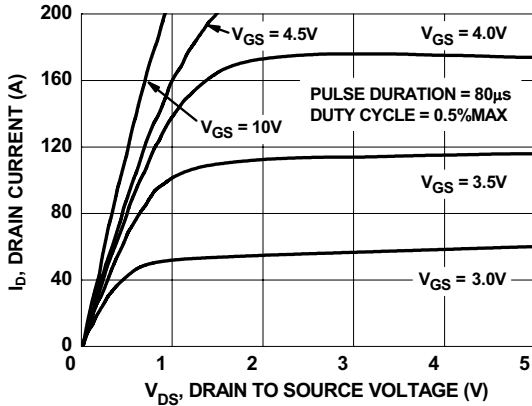


Figure 1. On Region Characteristics

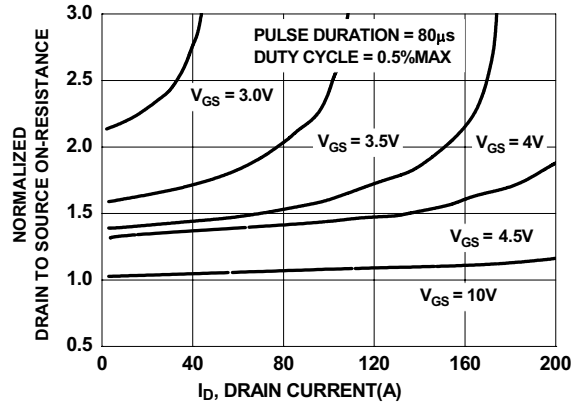


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

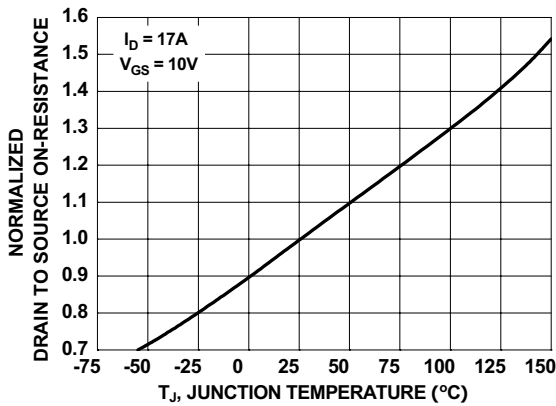


Figure 3. Normalized On Resistance vs Junction Temperature

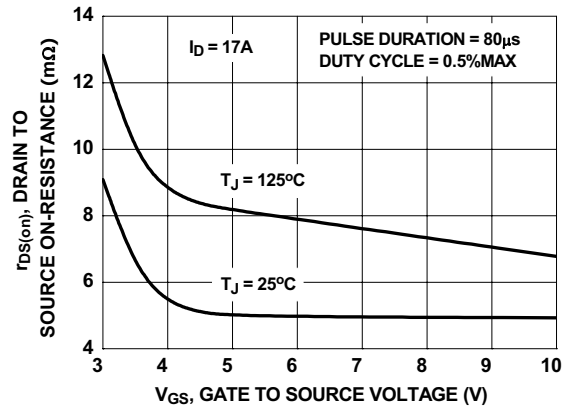


Figure 4. On-Resistance vs Gate to Source Voltage

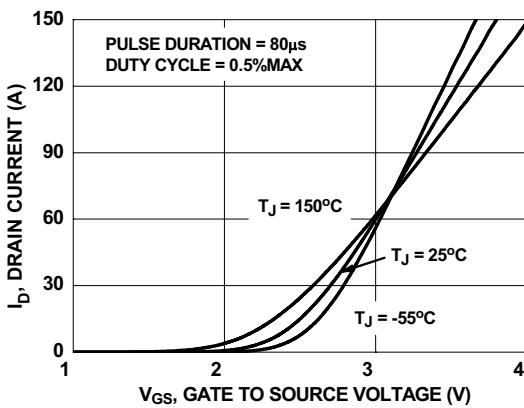


Figure 5. Transfer Characteristics

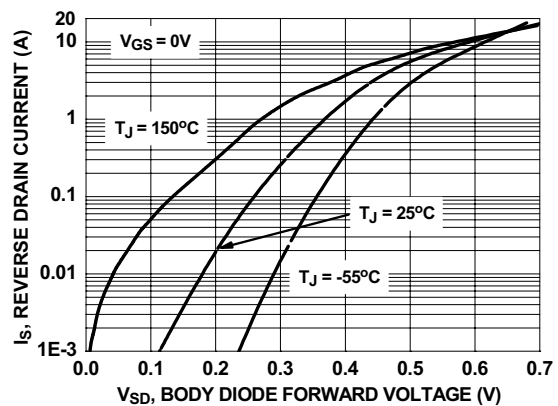


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

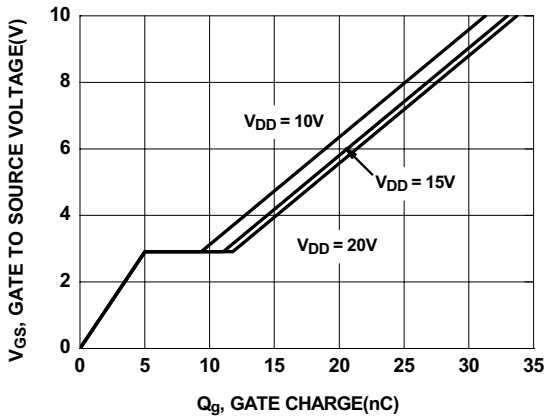


Figure 7. Gate Charge Characteristics

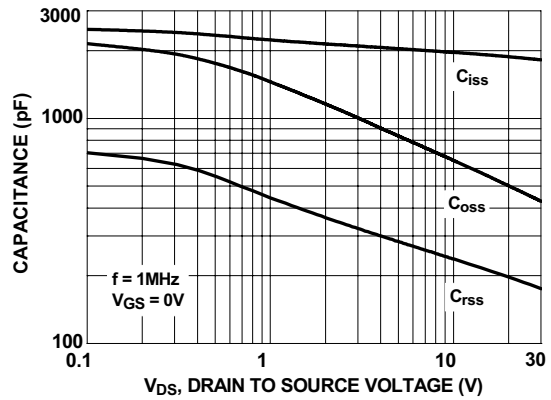


Figure 8. Capacitance vs Drain to Source Voltage

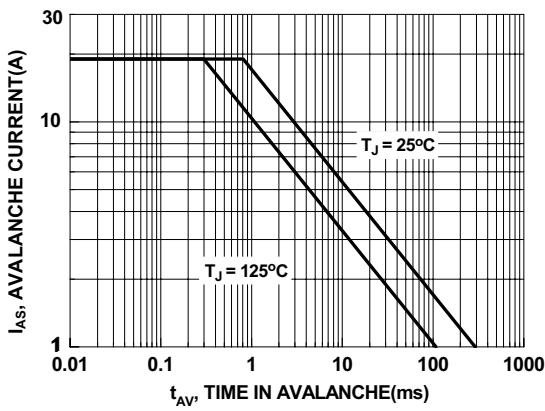


Figure 9. Unclamped Inductive Switching Capability

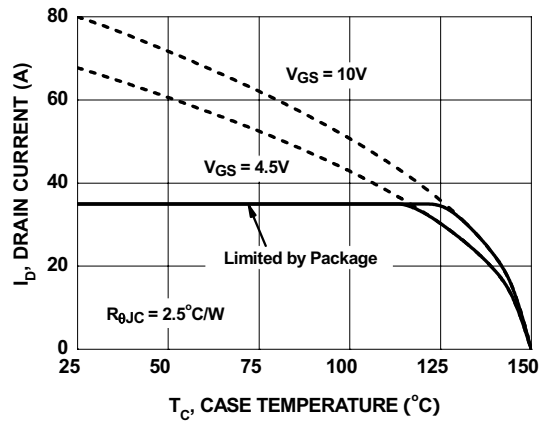


Figure 10. Maximum Continuous Drain Current vs Case Temperature

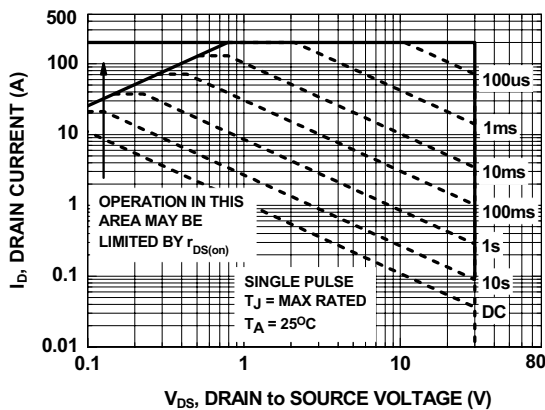


Figure 11. Forward Bias Safe Operating Area

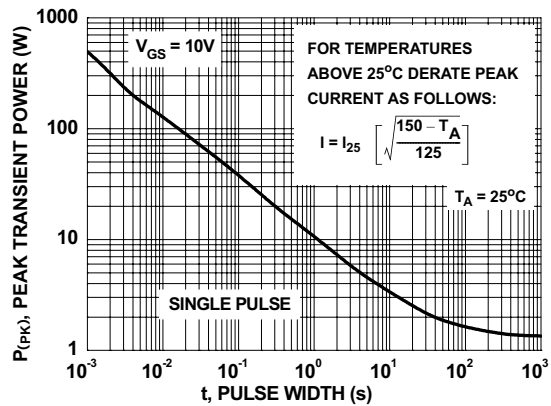
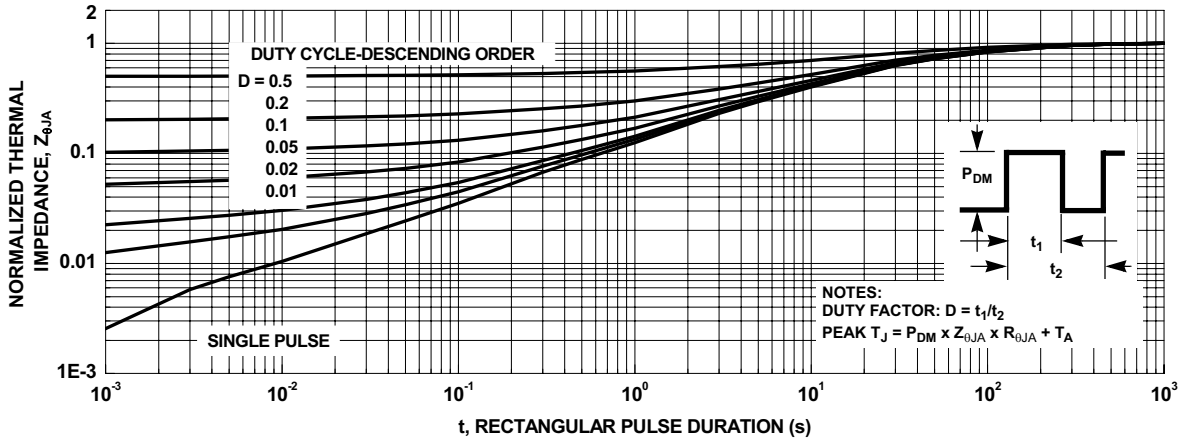


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted



Typical Characteristics (continued)

SyncFET Schottky body diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MoSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverse recovery characteristic of the FDMS8672S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

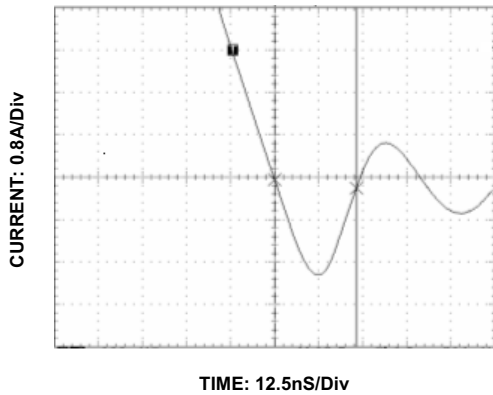


Figure 14. FDMS8672S SyncFET Body Diode Reverse Recovery Characteristics

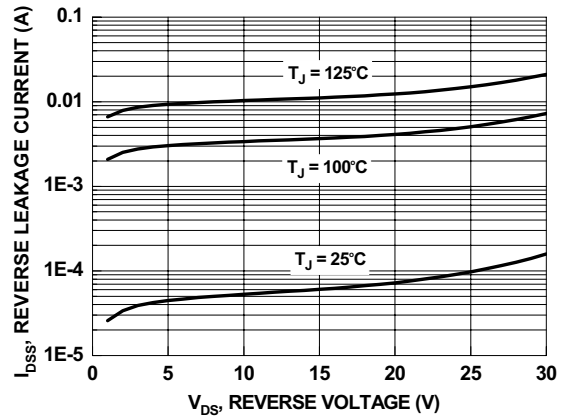
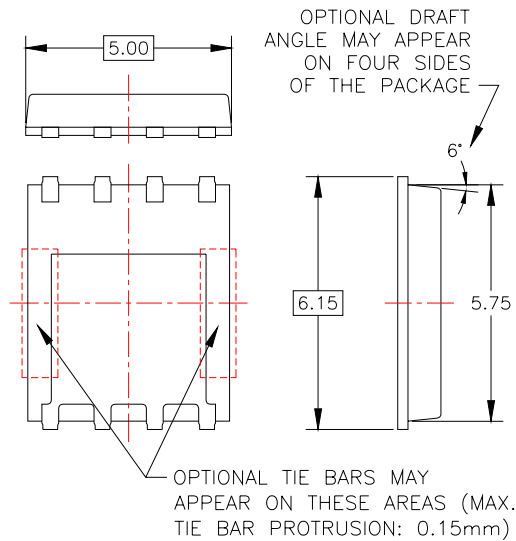
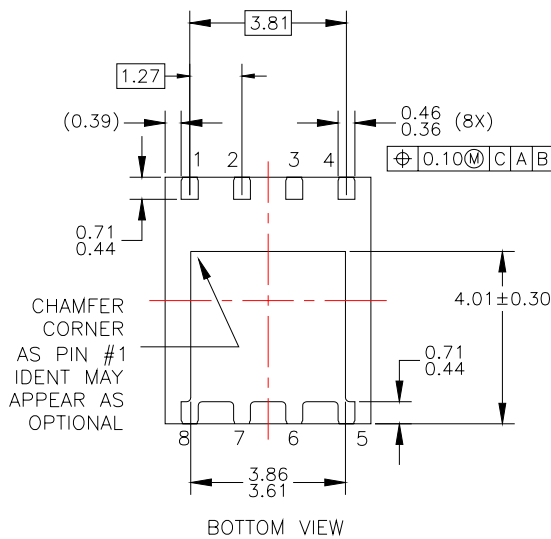
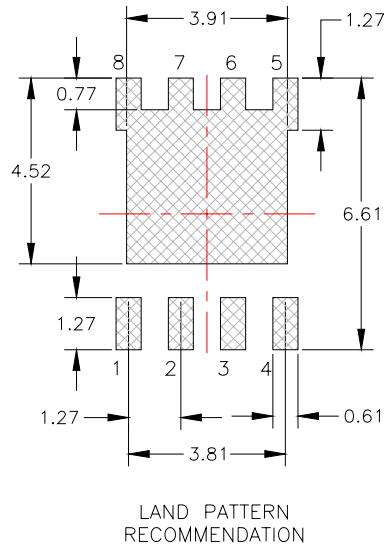
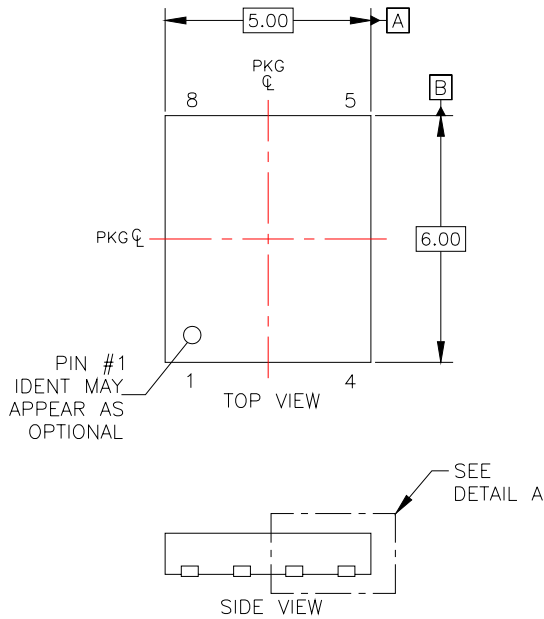


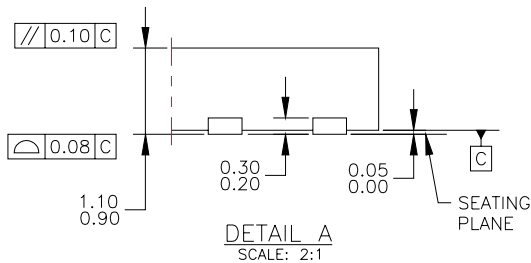
Figure 15. SyncFET Body Diode Reverse Leakage vs Drain to Source Voltage

Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED






- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- E) DRAWING FILE NAME: PQFN08AREV4





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