FAIRCHILD SEMICONDUCTOR®

August 2007

# FDMS2380

## Dual Integrated Solenoid Driver

## Features

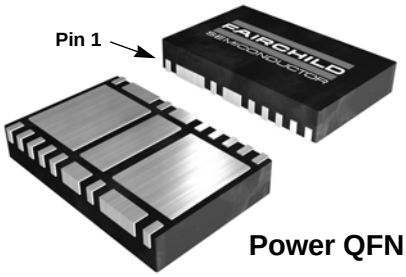
- 5A, 60V Load Clamp
- $r_{DS(ON)}$ = 30mΩ (Typ.) Excitation path
- 6V to 26V Operation
- CMOS Compatible
- Soft Short Detection
- Thermal Shutdown
- Diagnostic Output
- Integrated Clamps
- Over-current Protection
- Open Load Detection
- Over-voltage Protection

## Applications

- Transmission Solenoid Driver
- Inductive Load Management

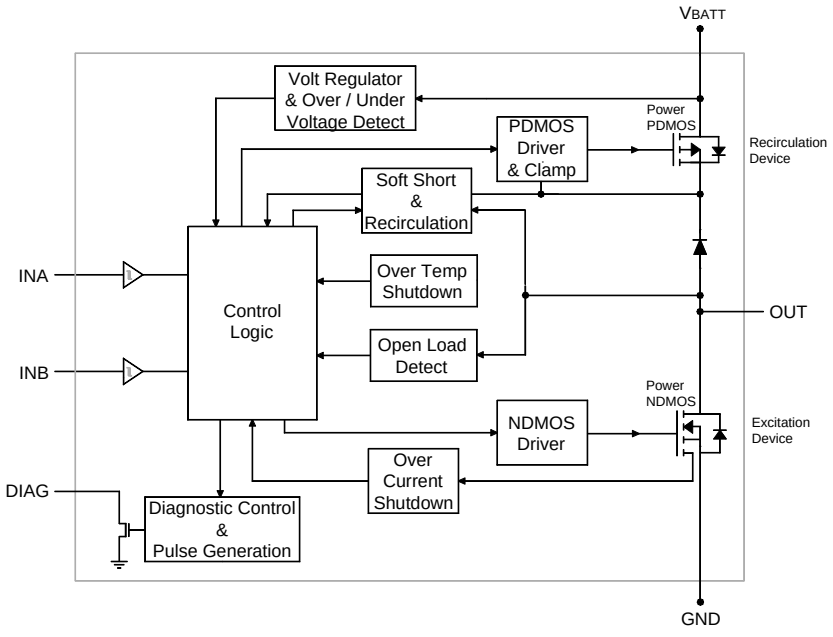
## General Description

The FDMS2380 is an intelligent low side driver with built in recirculation and demagnetization circuits designed specifically for driving inductive loads. The inputs are CMOS compatible. A separate diagnostic signal for each channel provides the system with an indication of the operation of the solenoid or the presence of a protection fault condition. Built-in Over-voltage, Over-current, Over-temperature circuits protect the device from these conditions. Additional diagnostic circuitry is included for detecting Open Load, Under-voltage and output ground fault conditions. The FDMS2380 contains two independent intelligent low side solenoid drivers.

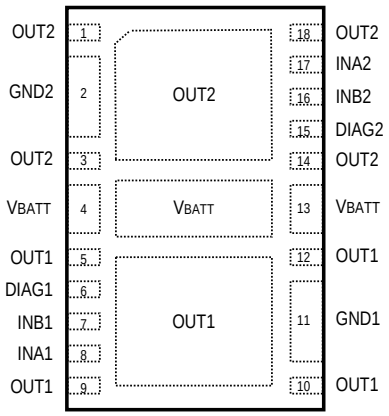



**Power QFN**

**Internal Logical Block Diagram (One of two Identical Channels)**



## Pin Assignment




TOP VIEW

## Pin Description

| QFN Pin | Pin Name | Pin Description |
|---|---|---|
| 1, 3, 14, 18, pad OUT2 | OUT2 | Power Driver Output (Ch2) |
| 2 | GND2 | Ground (Ch2) |
| 4, 13, pad $V_{BATT}$ | $V_{BATT}$ | Battery Supply Voltage. Battery supply is common to both channels |
| 5, 9, 10, 12, pad OUT1 | OUT1 | Power Driver Output (Ch1) |
| 6 | DIAG1 | Diagnostic Flag (Ch1). Open drain output. |
| 7 | INB1 | Input Control Signal B (Ch1) |
| 8 | INA1 | Input Control Signal A (Ch1) |
| 11 | GND1 | Ground (Ch1) |
| 15 | DIAG2 | Diagnostic Flag (Ch2). Open drain output. |
| 16 | INB2 | Input Control Signal B (Ch2) |
| 17 | INA2 | Input Control Signal A (Ch2) |

## Maximum Ratings $T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | Ratings | Units |
|---|---|---|---|
| $I_{OUT(rev)}$ | Maximum Reverse Output Current | -4 | A |
| $V_{BATT(max)}$ | Maximum DC Supply Voltage (Note 2) | 60 | V |
| $I_{IN}$ | Input Currents | 10 | mA |
| $V_{IN(max)}$ | Maximum Input Voltage | 8 | V |
| $I_{DIAG}$ | Diagnostic Output Current | 10 | mA |
| $V_{DIAG(max)}$ | Maximum Diagnostic Output Voltage | 8 | V |
| $P_D$ | Total Power dissipation | 7 | W |
| | Power dissipation $V_{BATT}$ pad | 2.3 | W |
| | Power dissipation OUT pads: $P_{D(OUT)} = P_{D(OUT1)} + P_{D(OUT2)}$ | 4.6 | W |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature | -40 to 160 | °C |

## Thermal Characteristics

| | | | |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance Junction to Case: OUT pad | 3.5 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance Junction to Case: $V_{BATT}$ pad | 4.0 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance Junction to Ambient: OUT pad (Note 1) | 60 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance Junction to Ambient: $V_{BATT}$ pad (Note 1) | 60 | °C/W |

## Ordering Information

| Part Number | Package | Packing Method | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| FDMS2380 | 18 pin QFN | Tape & Reel | 330mm | 24mm | 2000 |

**Notes:**

**1.** $R_{\theta JA}$ is measured with 1.0 $in^2$ copper on FR-4 board. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

**2.** The FDMS2380 requires one or more high quality local bypass capacitors (i.e., low ESL, low ESR and located physically close to the VBATT/Ground terminals of the device) to prevent fast transients on the $V_{BATT}$ line from affecting the operation of the device. More specifically, the bypass scheme must reduce transients with an amplitude passing through $V_{BATT(ov)}$ to have a rise time of less than 2.2V/µs.

## Electrical Characteristics $T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $V_{BATT(Oper)}$ | Operating Supply Voltage | --- | 6.0 | 14.0 | 26.0 | V |
| $I_{SQ}$ | Supply Quiescent Current | $V_{BATT}$ = 13V, $V_{INA}$ = $V_{INB}$ = 5V | - | 9.3 | 15 | mA |
| $I_{LK}$ | Output Leakage Current | $V_{BATT}$ = 18V, $V_{INA}$ = $V_{INB}$ = 1.5V | - | 0.2 | 5 | mA |
| **On Characteristics** | | | | | | |
| $r_{DS(ON)}$ | On Resistance - Excitation Path | $V_{BATT}$ = 13V, $V_{INA}$ = $V_{INB}$ = 5V, | - | 0.030 | 0.080 | Ω |
| | | $I_{OUT}$ = 5A, $T_C$ = 150°C | - | 0.050 | 0.100 | Ω |
| $V_{Recir(sat)}$ | Saturation Voltage - Recirculation Path | $V_{BATT}$ = 13V, $V_{INA}$ = 5V, $V_{INB}$ = 0V, $I_{OUT}$ = 10A | - | 1.4 | 1.8 | V |
| **Switching Characteristics** (Excitation Path) | | | | | | |
| $t_{d(ON)}$ | Output Turn-On Delay Time | $V_{BATT}$ = 14V, $R_{Load}$ = 2.5Ω | - | 7.0 | 30 | µs |
| $t_{d(OFF)}$ | Output Turn-Off Delay Time | | - | 8.3 | 30 | µs |
| $t_r$ | Rise Time | | - | 6.5 | 10 | µs |
| $t_f$ | Fall Time | | - | 3.0 | 10 | µs |
| **Logic Input Characteristics** | | | | | | |
| $V_{IL}$ | Input Low Level Voltage | --- | - | - | 1.5 | V |
| $V_{IH}$ | Input High Level Voltage | --- | 3.5 | - | - | V |
| $V_{CL}$ | Input Clamp Voltage | $I_{IN}$ <=10mA | 5.5 | - | - | V |
| $I_{IN}$ | Input Current (each input) | $V_{INA}$ = $V_{INB}$ = 5V | - | 90 | 160 | µA |
| | | $V_{INA}$ = $V_{INB}$ = 1.5V | 20 | 60 | - | µA |
| **Protection and Diagnostics Characteristics** (Note 1) | | | | | | |
| $T_{J(tsd)}$ | Thermal Shut-down Junction Temperature | --- | 160 | 172 | 185 | °C |
| $I_{OUT(trip)}$ | Output Current Trip | --- | 15 | 20 | 30 | A |
| $V_{BATT(ov)}$ | Over-voltage Threshold | --- | 27 | 29 | 32 | V |
| $V_{BATT(uv)}$ | Under-voltage Threshold | --- | - | 5.1 | 5.5 | V |
| $I_{OUT(ol)}$ | Open Load Detect Current | $V_{INA}$ = 5V, $V_{INB}$ = falling edge | 300 | 450 | 800 | mA |
| $V_{OUT(SS)}$ | Soft Short Detect Voltage | INA=0, INB=1, $V_{BATT}$ − $V_{OUT}$ | 0.3 | 0.43 | 0.6 | V |
| $R_{SS}$ | Soft Short Resistance | INA=0, INB=1, from $V_{OUT}$ to $V_{BATT}$ | 50 | 75 | 140 | Ω |
| $T_{SS}$ | Soft Short Active Time | INA=0, INB=1, time $R_{SS}$ is active | 1 | - | 3 | ms |
| $V_{OUT(cl1)}$ | NDMOS Over-voltage Clamp | Ref to GND; $I_{OUT}$ = 5A | 60 | 73 | 85 | V |
| $V_{OUT(cl2)}$ | Output Inductive Clamp Voltage | $V_{OUT}$ − $V_{BATT}$; $I_{OUT}$ = 5A | 27 | 30 | 33 | V |
| $V_{FB}$ | Flyback Diagnostic Threshold Voltage ($V_{OUT}$ − $V_{BATT}$ ) | Threshold where DIAG goes low during Fast turn-off Mode | 22 | 23 | 33 | V |
| $td_{(DIAG)}$ | Diagnostic Propagation Delay Time | Fast turn-off Mode; $V_{DIAG}$ = 1V | - | 3 | 10 | µs |
| $t_{DAIGFB(min)}$ | Minimum Diagnostic Flyback Time | --- | 26 | 42 | 50 | µs |
| $t_{DIAG(prot)}$ | Protection Diagnostic Pulse Width | Over-voltage, Under-voltage, Over-current, Over-temperature | 2 | 7 | 10 | µs |
| $V_{DIAG(low)}$ | Diagnostic Voltage Low | $I_{DIAG}$ <= 1mA, Diagnostic output active | - | - | 0.9 | V |
| $V_{DIAG(cl)}$ | Diagnostic Output Clamp Voltage | $I_{DIAG}$ <= 10mA | 5.5 | - | - | V |

**Notes:**

**1.** Integrated protection functions, as described in this data sheet, are designed to prevent the destruction of the IC and these fault conditions are considered 'outside' the normal operating ranges. It is important to note that the protection functions integrated into this device are NOT designed for continuous repetitive operation.

## Normal operation (see figure 1)

**STANDBY MODE, INA = INB = 0** In the Standby mode, INA and INB are in the logic low state and there is no output current flow through solenoid coil. Both the PDMOS and NDMOS output power transistors are in their off state. This is the condition either at the start of a cycle to activate the solenoid or after a flyback signal has been generated.

**EXCITATION MODE, INA = INB = 1** In the Excitation mode, INA and INB are in the logic high state and the NDMOS power transistor is turned on to sink current through the coil connected to the positive supply.

The output current rises in this condition until limited by either the coil resistance or the FDMS2380 if the current reaches the output current trip level $I_{OUT(trip)}$ in which case the FDMS2380 will turn off the NDMOS and issue a protection diagnostic signal.

**RECIRCULATION MODE, INA = 1, INB = 0** The Recirculation mode normally follows the Excitation mode. In this mode the NDMOS is turned off and the PDMOS is on. The current in the coil, connected to the output, is re-circulated to the positive power supply pin through the low impedance path of the recirculation diode and the PDMOS transistor. In the Recirculation mode the coil current $I_{OUT}$ slowly decays due to the impedance of the inductive load and the forward voltage drop across the FDMS2380 recirculation path.

The FDMS2380 will also enter the Recirculation mode during over-voltage, over-current, and over-temperature conditions as a means to limit the power dissipation in the device.

**FAST TURN-OFF MODE, INA $-> 0$** The fast turn-off mode is initiated whenever the INA pin transitions from a logic high to low state with INB also in a logic low state. In this mode the output voltage "flies back" to $V_{BATT}+V_{OUT(cl2)}$ where it is clamped by the FDMS2380 and the coil current is recirculated through the device back to the $V_{BATT}$ supply. The larger amplitude flyback voltage causes the coil current to rapidly discharge shutting off the solenoid. This flyback condition shall last as long as the output voltage is greater then $V_{BATT}$ and less then $V_{OUT(cl1)}$. During this time, the output diagnostic pin DIAG is driven low for the duration of the flyback pulse. Any output flyback pulses which are less then the period $t_{DIAGFB(min)}$ will have its corresponding diagnostic pulse lengthened to a minimum of $t_{DIAGFB(min)}$ to help identify the flyback condition from a possible protection diagnostic fault.

If an under-voltage condition exists the flyback diagnostic pulse will be blocked, however, a flyback diagnostic pulse is generated if the flyback condition is still present at the end of the under-voltage condition.

For inputs INA and INB in the logic low state the NDMOS and PDMOS transistors will be off. Exceptions to this condition are; during an alternator load dump event that could drive the output to greater then $V_{OUT(cl1)}$ the NDMOS will clamp the output voltage, and during a flyback event the PDMOS will clamp the output to $V_{OUT(cl2)}$.

Using the curves from figures 7 through 12, the driving parameters (e.g., maximum duty cycle, etc.) and/or the solenoid characteristics (e.g., coil resistance or coil inductance) must be checked to ensure the FDMS2380 is not damaged by SCIS (self-clamped inductive switching) related overstress.

**SOFT SHORT TEST MODE, INA = 0 INB = 1** This test mode is used for detecting an output ground fault. The Soft Short mode is initiated any time INA=0 and INB=1 when in the Standby mode. The input conditions need to be held for a minimum of 2 ms to allow for the timing of the Soft Short detection circuit. After this setup time the FDMS2380 switches in a resistance ($R_{SS}$) of approximately 75 ohms between $V_{BATT}$ and the output (OUT) pin. This resistance, connected in parallel to the load, acts as an additional pull-up impedance to the positive power supply. To minimize power dissipation in the event of an output ground fault, the output pull-up resistor, activated in the Soft Short mode, is only switched on for a period of Tss by the FDMS2380. Regardless if the INA and INB signals remain in the Soft Short state for a longer period of time. Immediately prior to the end of this period, the output voltage $V_{OUT}$ is compared to the $V_{BATT}$ supply voltage and if the difference is greater then $V_{OUT(ss)}$ the diagnostic pin DIAG is pulled low. The diagnostic pin will stay activated until the Soft Short mode is terminated by a change of the INA or INB inputs.

To minimize the power dissipation the Soft Short test mode should not be restarted sooner than 10 ms after a previous Soft Short test.

## Self-Protection Functions

Refer to figures 2 through 6 for self-protection waveforms. All self-protection modes except over-voltage and under-voltage are reset when INA goes to logic 0. When a self-protection condition is detected the FDMS2380 will issue a protection fault on the diagnostic pin. This fault condition is signaled by a 2 μs to 10 μs pulse $t_{DIAG(prot)}$ on the diagnostic pin DIAG. If the INA pin is activated while the condition setting the protection fault is still active additional protection fault diagnostic pulses will be issued.

**Current Trip** (see figure 2) Anytime during Excitation mode, if the current in the NDMOS rises above the $I_{OUT(trip)}$ level, the FDMS2380 will turn off the NDMOS and enter into the Recirculation mode and issue a 2 μs to 10 μs protection fault pulse on the diagnostic pin DIAG. The device will remain in this Recirculation mode as long as the INA pin remains high and is terminated with the falling edge of INA.

**Thermal Shutdown** (see figure 3) The FDMS2380 is internally protected against over-temperature conditions by a temperature sensing circuit. When the FDMS2380 junction temperature exceeds the protection limit, $T_{J(tsd)}$, thermal shutdown of the device will occur. Upon entering thermal shutdown a 2 μs to 10 μs protection fault signal is activated in the DIAG pin. In thermal shutdown, the NDMOS is switched off and the FDMS2380 operates in recirculation to discharge the energy in the load coil and minimize power dissipation. The FDMS2380 will remain in this state until INA is taken to logic 0. A protection fault signal will be issued each time INA is brought to a logic high while the over-temperature conditions exists.

**Overvoltage** (see figure 4) While in the Excitation mode if the $V_{BATT}$ pin rises above the over-voltage threshold, $V_{BATT(ov)}$, the FDMS2380 is forced into the Recirculation mode and a protection fault signal on the diagnostic pin DIAG is generated. This condition is not reset by INA going low but by the voltage of the $V_{BATT}$ pin returning below the $V_{BATT(ov)}$ level. A protection fault pulse will be issued each time the device is driven into the Excitation state while the over-voltage condition exists.

The FDMS2380 is designed with a fast responding over-voltage circuit that disables the output slope control circuit which minimizes radiated EMI. However, voltage transitions on the $V_{BATT}$ pin which exceed 30 volts above the battery need to be limited to a rise time no faster then 2.2 V/μs through the use of a power supply bypass capacitor.

**Undervoltage** (see figure 6) The FDMS2380 will operate down to a minimum voltage of $V_{BATT(uv)}$. If the battery supply drops below this minimum voltage the device is forced into the Standby mode. If INA is high during this condition a 2 μs to 10 μs protection fault pulse is issued on the diagnostic DIAG pin. In addition, a diagnostic pulse will be generated each time INA transitions from a low to a high logic level while remaining in this under-voltage condition.

The FDMS2380 will return to normal operation when $V_{BATT}$ is 6 volts or greater.

## Diagnostic Functions

**Open Load Detect** (see figure 5) While INA and INB are high, if the load current fails to rise above the open load current level, $I_{OUT(ol)}$, before INB transitions low an open load diagnostic fault will be issued. The diagnostic pin will be driven low on the falling edge of the INB signal and remain low until INA is returned to a logic 0 condition. The open load detect mechanism senses current flowing through the NDMOS at the falling edge of the INB signal. If an open load condition exists during the Excitation phase but is corrected before the INB falling edge the open load condition would not be detected and the open load diagnostic fault would not be generated.

The open load detection circuit does not alter the operation of the FDMS2380 and the PDMOS and NDMOS output transistors will be driven into the operational modes as commanded by the INA and INB inputs.

If during the detection of the open load condition a protection fault condition also arises, the open load diagnostics will be terminated and then after a 2 μs to 10 μs blanking period the protection diagnostic will be generated.

## Operational Truth Table

| Conditions | INA | INB | NDMOS | PDMOS |
|---|---|---|---|---|
| Standby Mode: | L | L | OFF | OFF |
| Soft Short Test Mode | L | H | OFF | ON |
| Excitation Mode: (No protection faults) | H | H | ON | ON |
| Recirculation Mode | H | L | OFF | ON |
| Fast Turn-off Mode: $V_{FB} < V_{OUT} < V_{OUT(cl1)}$) | L | L | OFF | $V_{OUT}$ clamped to $V_{OUT(cl2)}$ |
| Alternator Load Dump: $V_{OUT} > V_{OUT(cl1)}$ | L | X | NDMOS in UIS operation | NA |
| Thermal Shutdown: $T_J > T_{J(tsd)}$ | H | X | OFF | ON |
| Current Trip: $I_{OUT} > I_{OUT(trip)}$ | H | H | OFF | ON |
| Overvoltage: $V_{BATT} > V_{BATT(ov)}$ | H | H | OFF | ON |
| Undervoltage: $V_{BATT} < V_{BATT(uv)}$ | H | X | OFF | OFF |
| Open Load: $I_{OUT} < I_{OUT(ol)}$ refer to Open Load waveforms (Figure 5) | - | - | - | - |

H = High, L = Low, X = Don't Care
General operation INA and INB are standard logic inputs that control Standby, Excitation, Recirculation, Diagnostics, and Fast turn-off modes in the FDMS2380.

## Typical Characteristics $T_C$ = 25°C unless otherwise noted

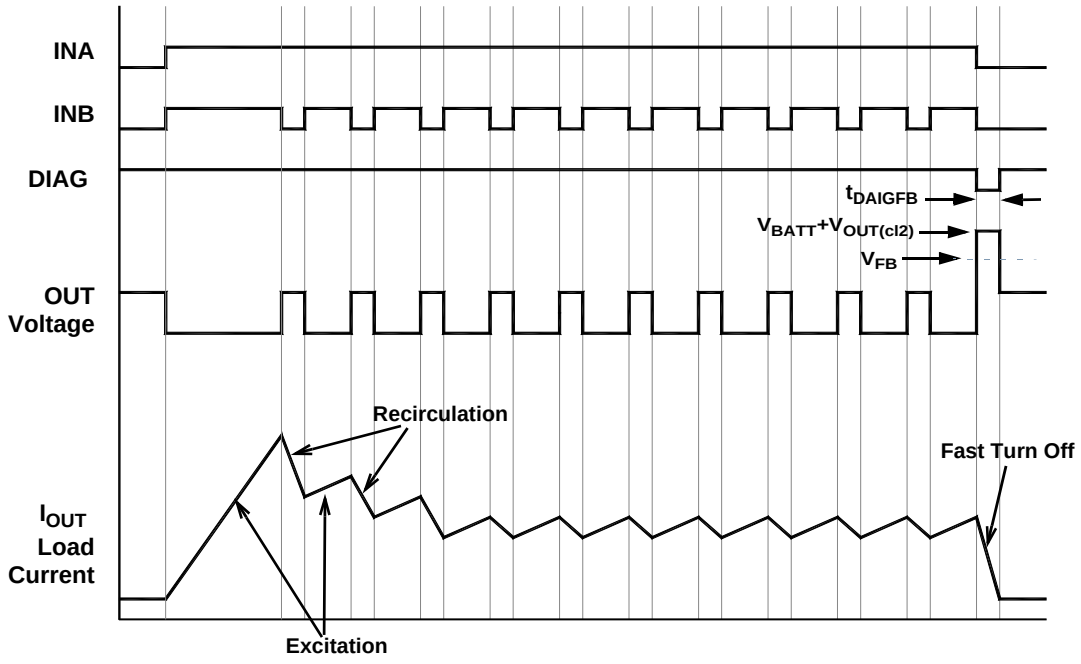



**Figure 1. Normal Operation**

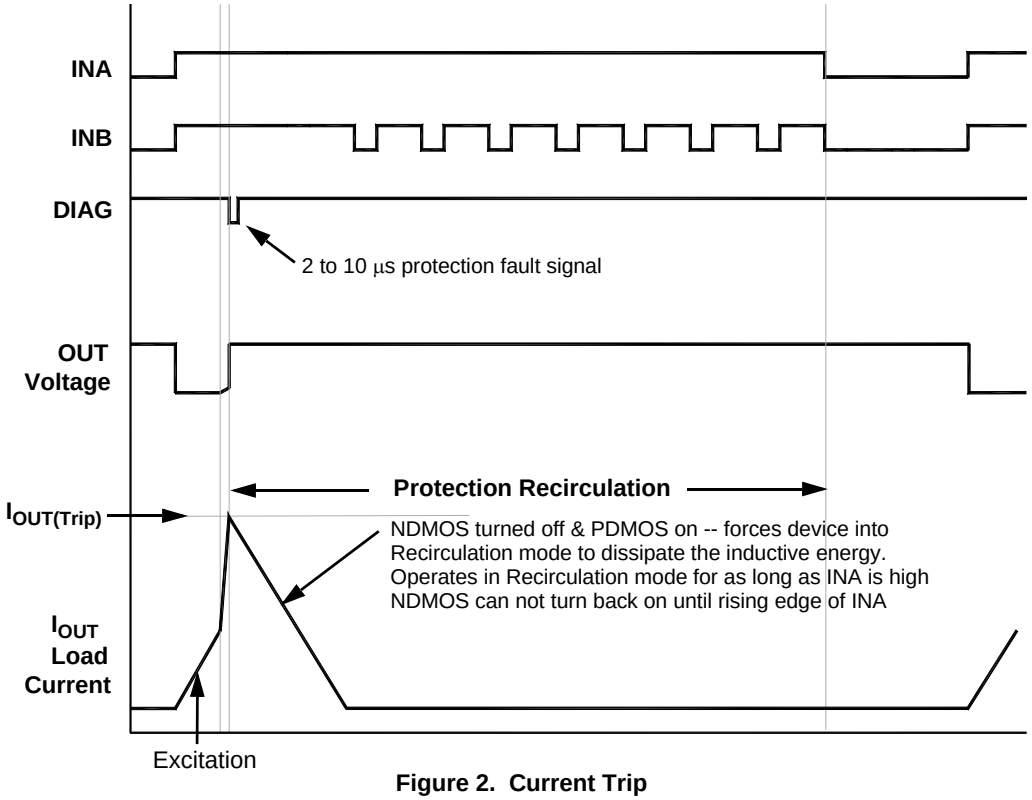



**Figure 2. Current Trip**

## Typical Characteristics $T_C$ = 25°C unless otherwise noted

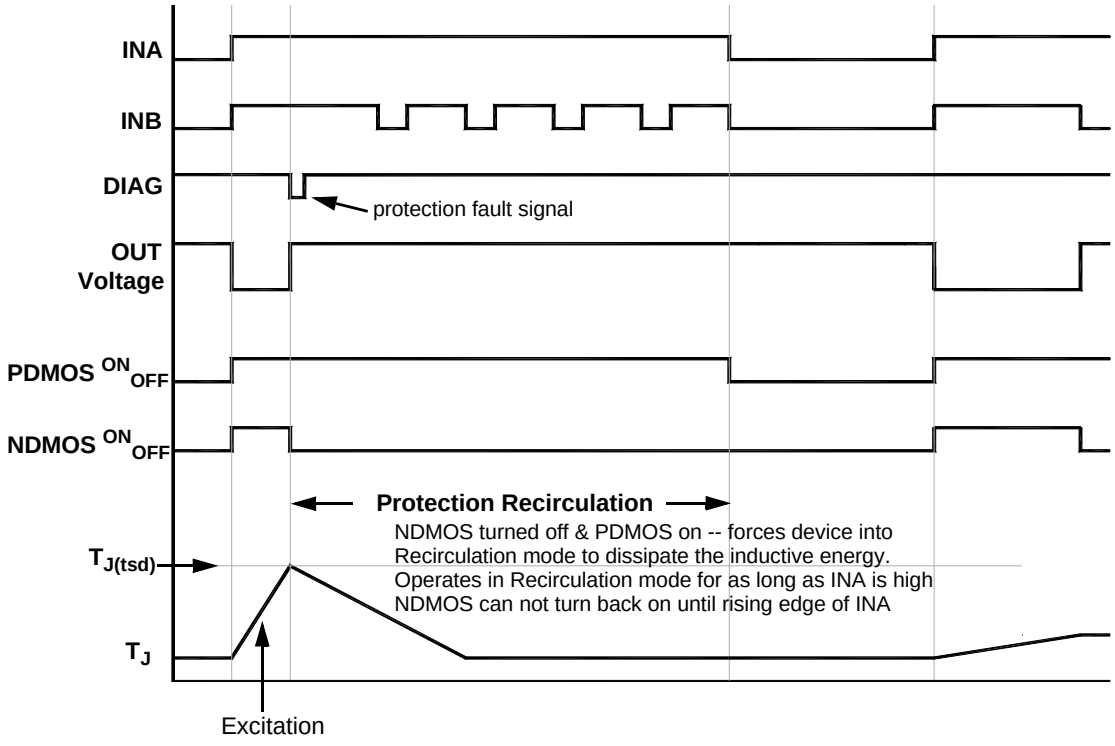



**Figure 3. Thermal Shutdown**

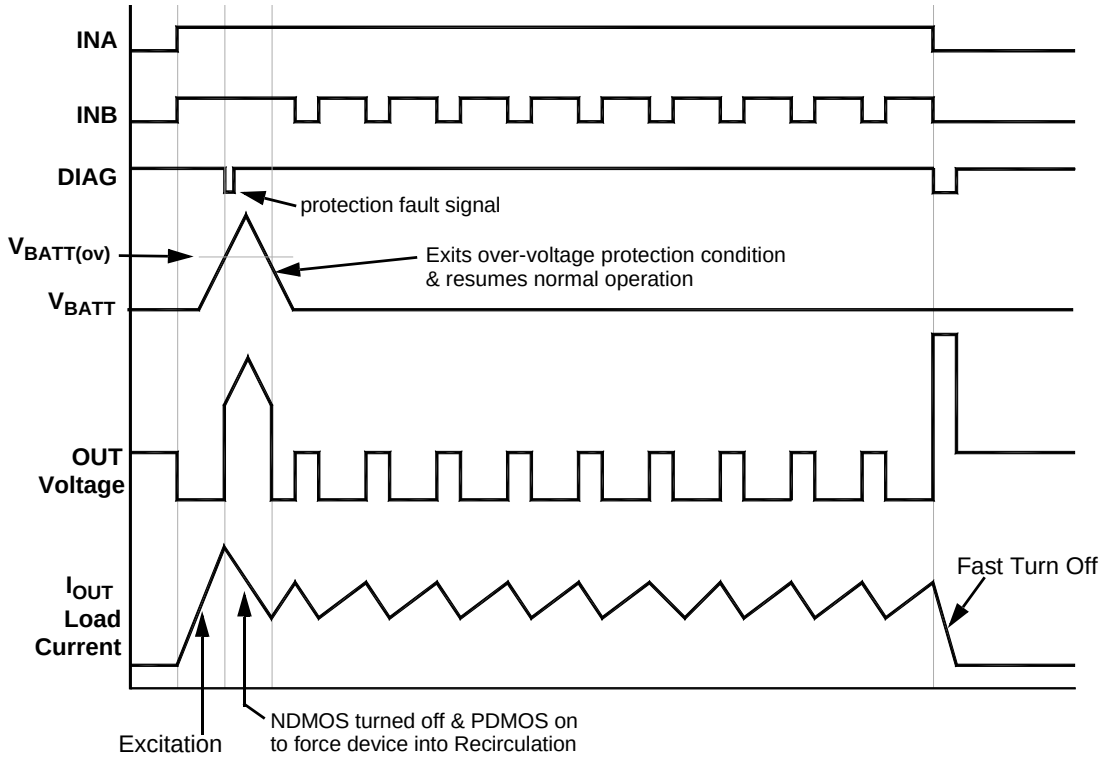



**Figure 4. Over-Voltage**

## Typical Characteristics $T_C$ = 25°C unless otherwise noted

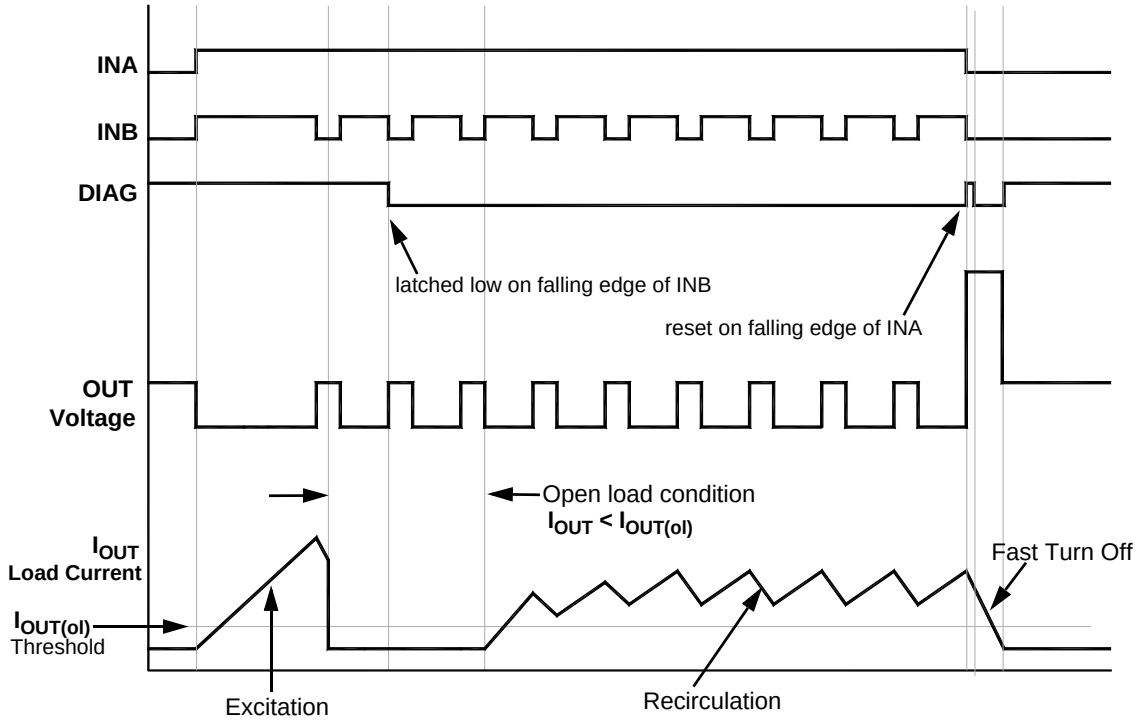



**Figure 5. Intermittent Open Load**

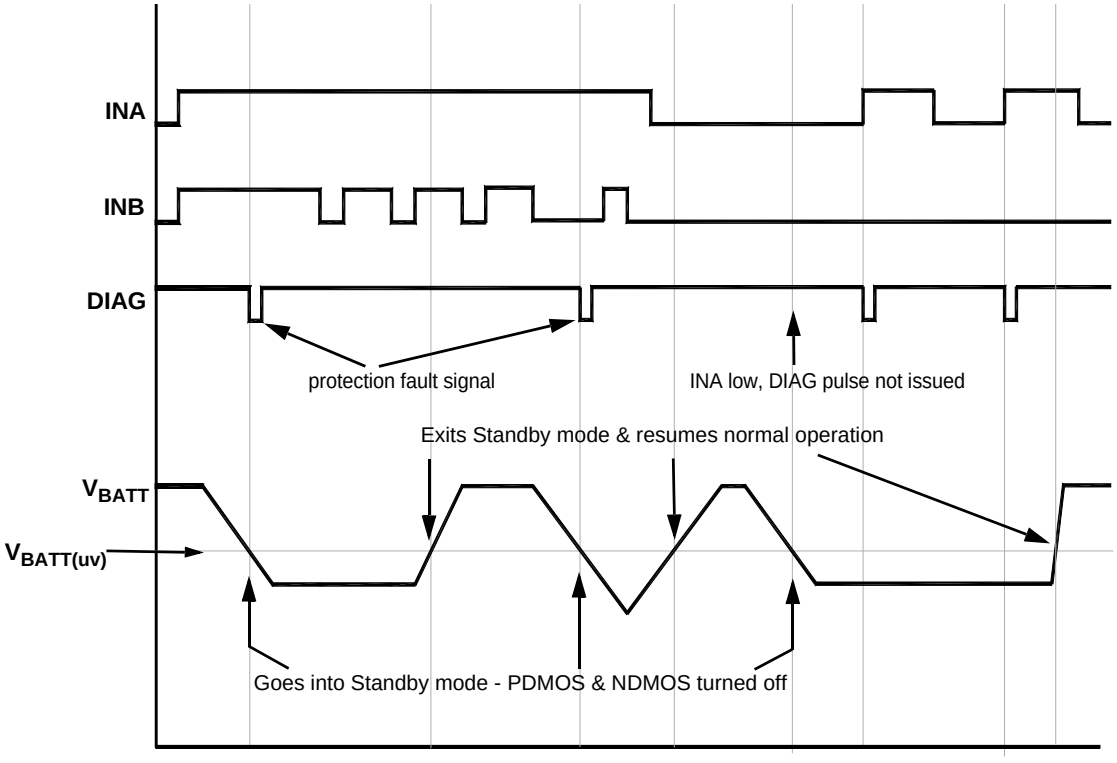



**Figure 6. Under-Voltage**

## Typical Characteristics $T_C$ = 25°C unless otherwise noted

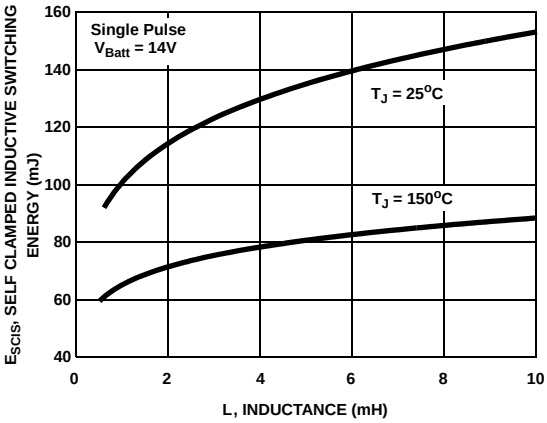



**Figure 7. Self Clamped Inductive Switching Energy vs Inductance**

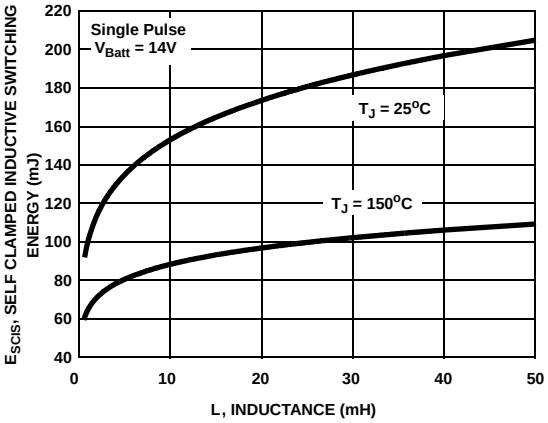



**Figure 8. Self Clamped Inductive Switching Energy vs Inductance**

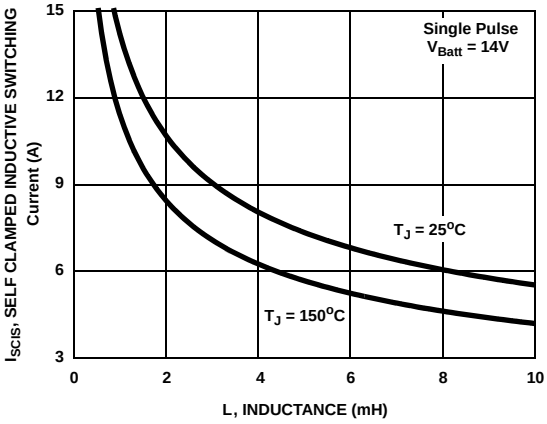



**Figure 9. Self Clamped Inductive Switching Current vs Inductance**

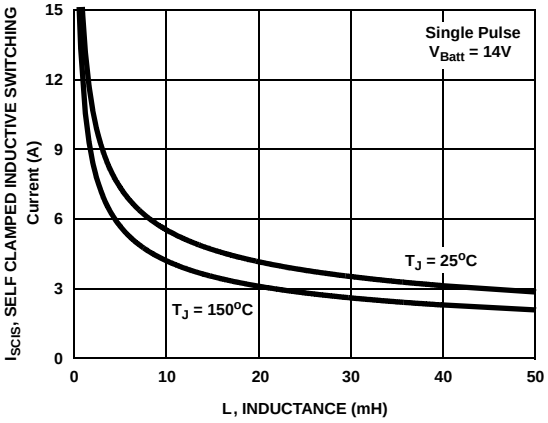



**Figure 10. Self Clamped Inductive Switching Current vs Inductance**

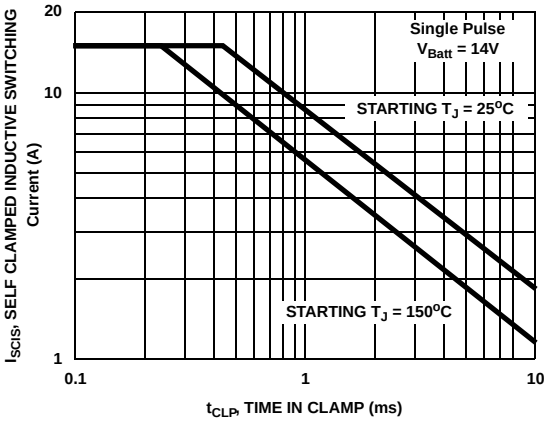



**Figure 11. Self Clamped Inductive Switching Current vs Time in Clamp**

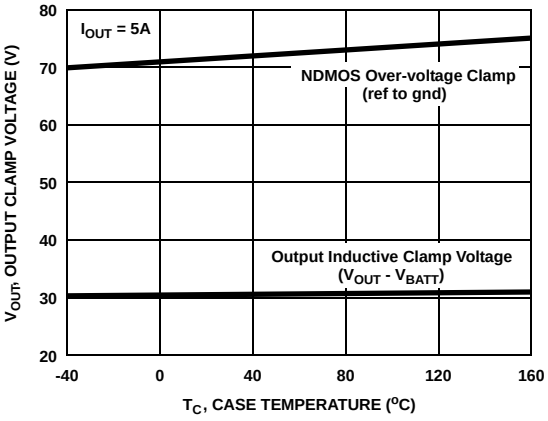



**Figure 12. Output Clamp Voltage vs Case Temperature**

## Typical Characteristics (Continued) $T_C$ = 25°C unless otherwise noted

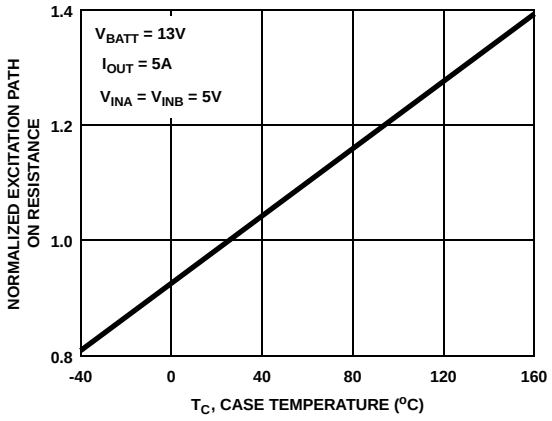



**Figure 13. Normalized Excitation Path On Resistance vs Case Temperature**

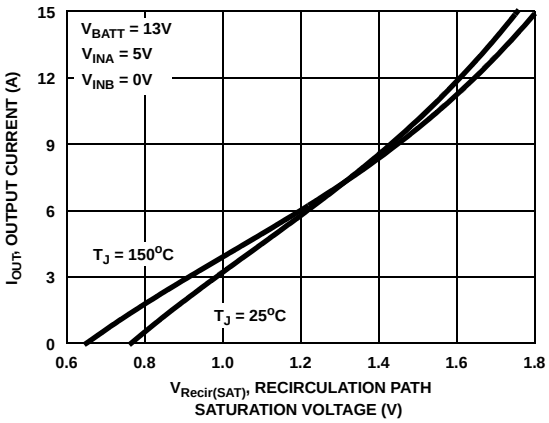



**Figure 14. Output Current vs Recirculation Path Saturation Voltage**

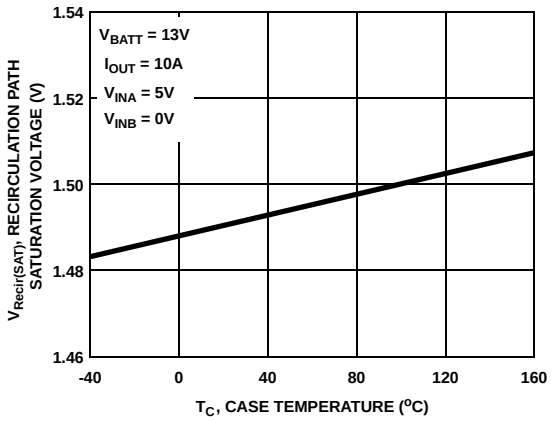



**Figure 15. Recirculation Path Saturation Voltage vs Case Temperature**

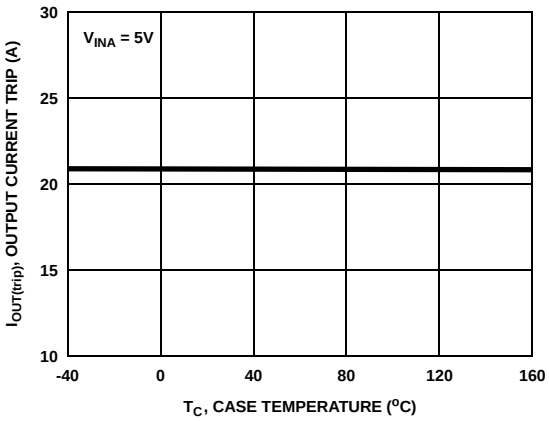



**Figure 16. Output Current Trip vs Case Temperature**

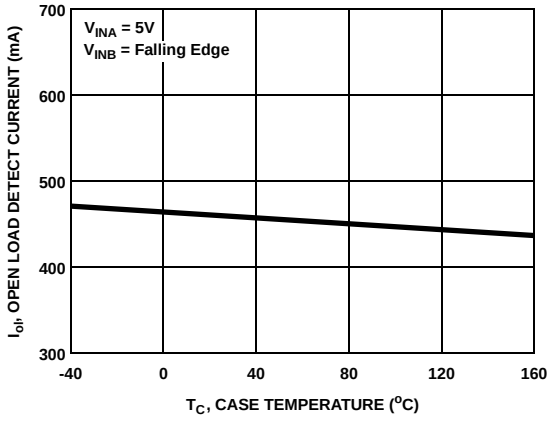



**Figure 17. Open Load Detect Current vs Case Temperature**

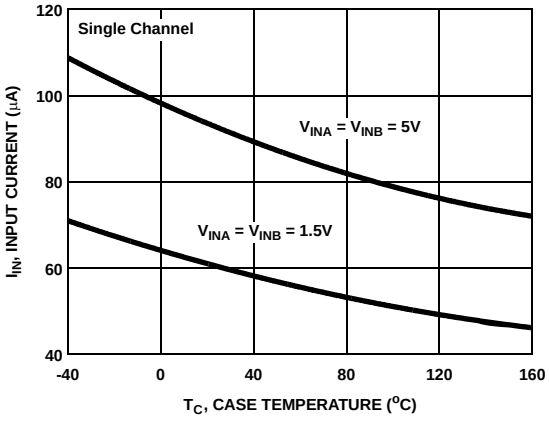



**Figure 18. Input Current vs Case Temperature**

## Typical Characteristics (Continued) $T_C$ = 25°C unless otherwise noted

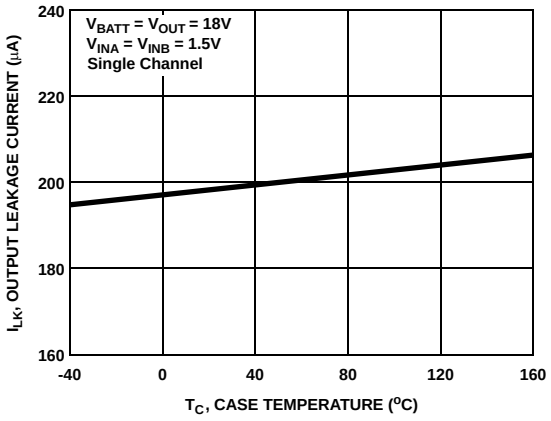



**Figure 19. Output Leakage Current vs Case Temperature**

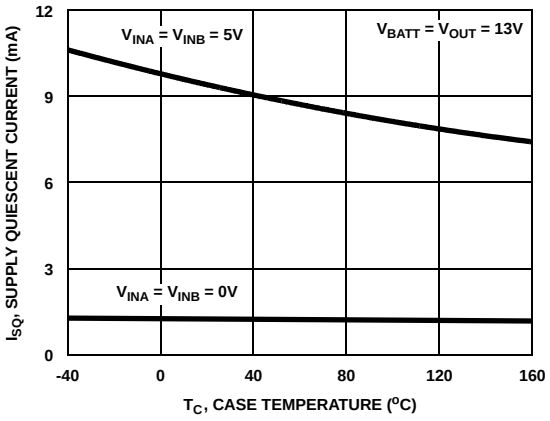
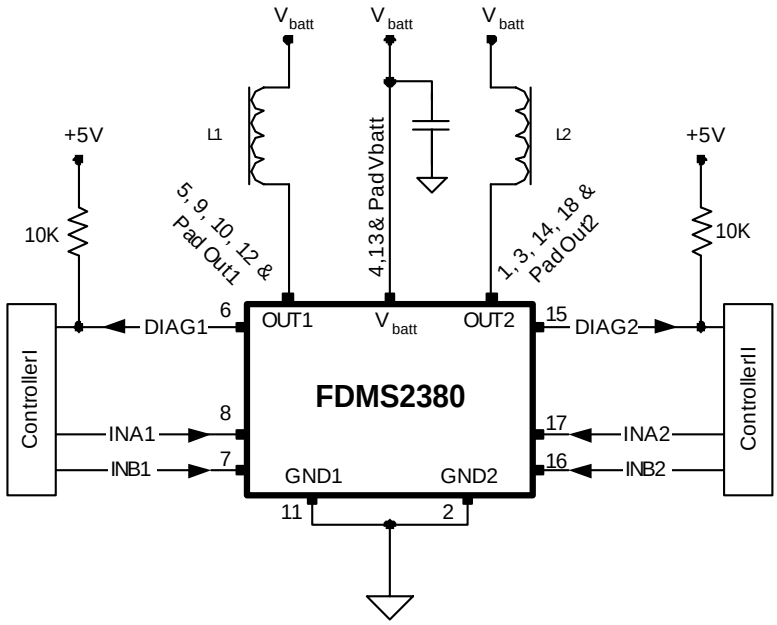



**Figure 20. Supply Quiescent Current vs Case Temperature**

## Typical Application Circuit

The following schematic of an FDMS2380 used in a basic application is just one of several possible variations for this device. It shows two external and independent controllers, one for each channel, and two solenoids being controlled by the FDMS2380. Furthermore, it shows the external local $V_{BATT}$ bypass capacitor, the details of which are discussed in the Maximum Ratings section. The FDMS2380 ground pins GND1 and GND2 are fully isolated; therefore, they are normally connected together on the PCB.

When designing the PCB for the FDMS2380 the user needs to provide as low a thermal impedance as is possible for both the $V_{BATT}$ and OUT[1,2] paddles on the bottom of the package. The power density in the dual integrated solenoid driver can be quite large and care should be taken to optimize the thermal impedance of the system to maximize the power handling capability of the device while minimizing the maximum operating temperature.



# Tape and Reel Specifications

## Tape Dimensions:

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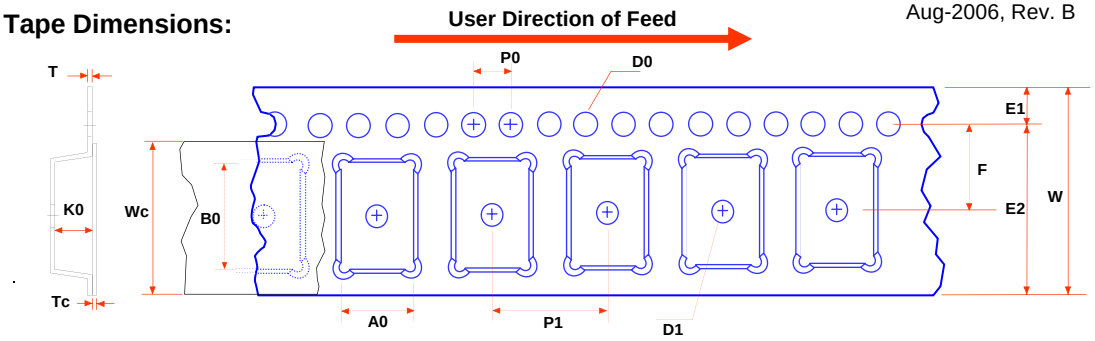
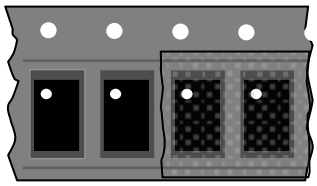



| Dimensions are in millimeter | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pkg. Type | A0 | B0 | W | D0 | D1 | E1 | E2 | F | P1 | P0 | K0 | T | Wc | Tc |
| 18 pin QFN | 8.35 +/-0.10 | 12.35 +/-0.10 | 24.0 +/-0.3 | 1.50 +0.10/-0.0 | 1.50 min | 1.75 +/-0.10 | 22.25 min | 11.50 +/-0.10 | 16.0 +/-0.1 | 4.0 +/-0.1 | 2.40 +/-0.10 | 0.30 +/-0.05 | 21.3 +/-0.1 | 0.10 max |

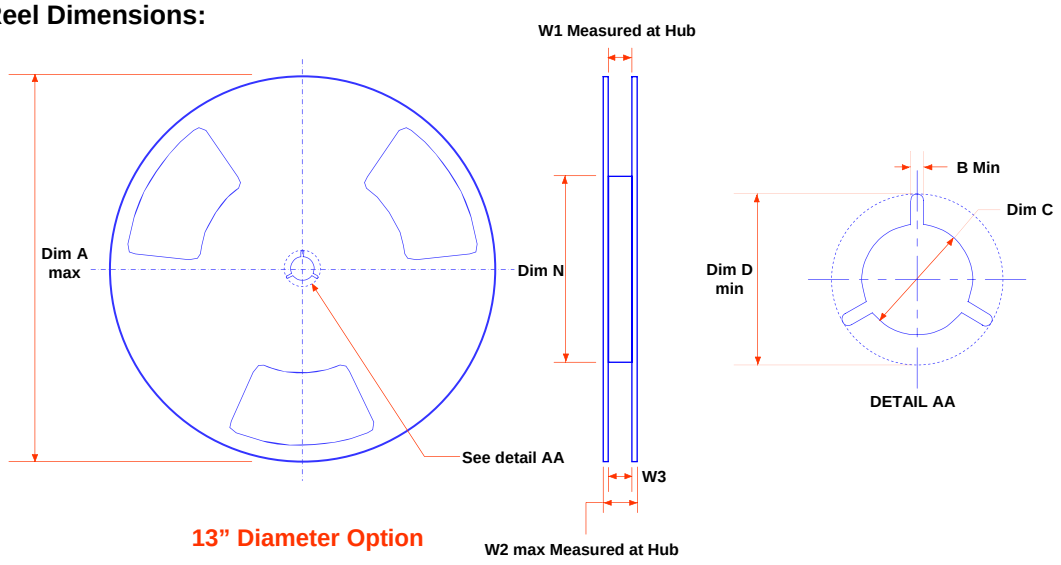
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements.


**Component Rotation** (Side Sectional View)



**Package Orientation**

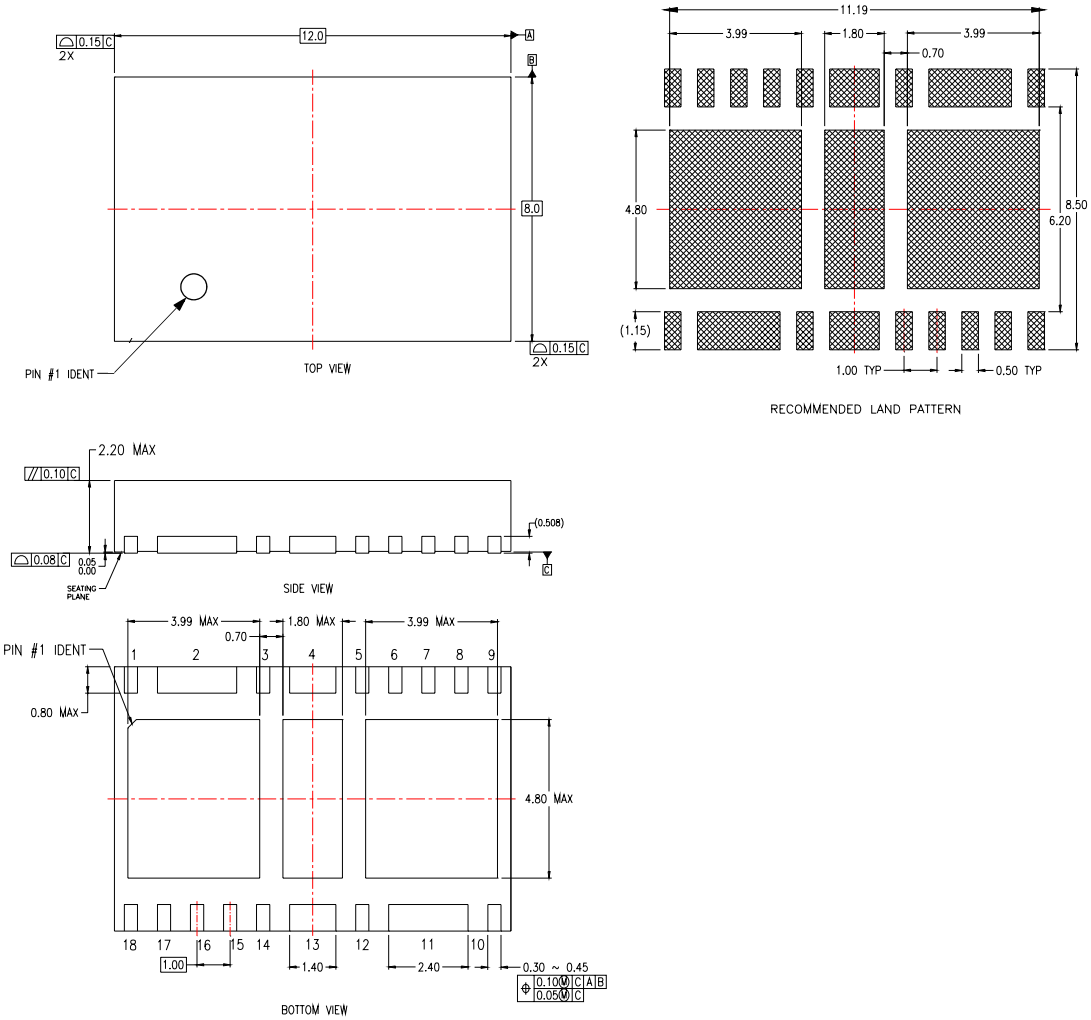
## Reel Dimensions:




**13” Diameter Option**

| Dimensions are in inches and millimeters | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Tape Size | Reel Option | Dim A | Dim B | Dim C | Dim D | Dim N | Dim W1 | Dim W2 | Dim W3 (LSL-USL) |
| 24 mm | 13” Dia | 13.00<br>330 | 0.079<br>2.0 | 0.512 ± 0.0008<br>13 ± 0.20 | 0.819<br>20.8 | 4.00<br>100 | 0.960 + 0.078/-0<br>24.4 + 2/-0 | 1.12<br>28.4 | 0.941 – 1.079<br>23.9 – 27.4 |

## Physical Dimensions




NOTES:

A. DIMENSIONS ARE IN MILLIMETERS.
B. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

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SMART START™
SPM®
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SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
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