FAIRCHILD SEMICONDUCTOR®

November 2013

FDMC86106LZ

N-Channel Shielded Gate PowerTrench® MOSFET

100 V, 7.5 A, 103 mΩ

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 103 mΩ at V_{GS} = 10 V, I_D = 3.3 A
- Max $r_{DS(on)}$ = 153 mΩ at V_{GS} = 4.5 V, I_D = 2.7 A
- HBM ESD protection level > 3 KV typical (Note 4)
- 100% UIL Tested
- RoHS Compliant

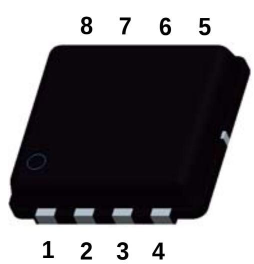
General Description

This N-Channel logic Level MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance. G-S zener has been added to enhance ESD voltage level.

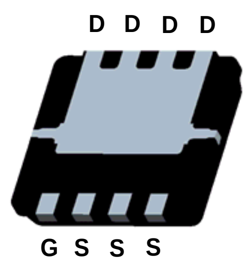
Application

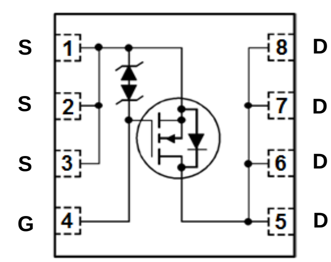
- DC - DC Conversion

Top



Bottom





MLP 3.3x3.3

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous (Package limited) T_C = 25 °C	7.5	A
	-Continuous (Silicon limited) T_C = 25 °C	9.6	
	-Continuous T_A = 25 °C (Note 1a)	3.3	
	-Pulsed	15	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	12	mJ
P_D	Power Dissipation T_C = 25 °C	19	W
	Power Dissipation T_A = 25 °C (Note 1a)	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	6.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC86106Z	FDMC86106LZ	Power 33	13 ”	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		73		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.0	1.8	2.2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 3.3 A		79	103	mΩ
		V_{GS} = 4.5 V, I_D = 2.7 A		105	153	
		V_{GS} = 10 V, I_D = 3.3 A, T_J = 125 °C		136	178	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 3.3 A		11		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		232	310	pF
C_{oss}	Output Capacitance			45	60	pF
C_{rss}	Reverse Transfer Capacitance			2.4	5	pF
R_g	Gate Resistance			0.7		Ω

Switching Characteristics

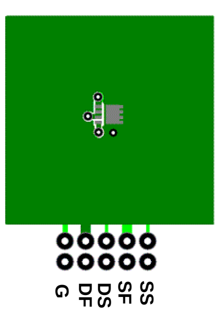
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50 V, I_D = 3.3 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		4.5	10	ns
t_r	Rise Time			1.3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			10	20	ns
t_f	Fall Time			1.4	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 50 V, I_D = 3.3 A		4	6	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 4.5 V; V_{DD} = 50 V, I_D = 3.3 A		2	3	nC
Q_{gs}	Total Gate Charge	V_{DD} = 50 V, I_D = 3.3 A		0.8		nC
Q_{gd}	Gate to Drain "Miller" Charge			0.7		nC

Drain-Source Diode Characteristics

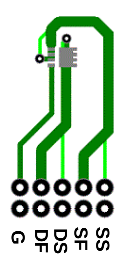
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 3.3 A (Note 2)		0.85	1.3	V
		V_{GS} = 0 V, I_S = 2 A (Note 2)		0.82	1.2	
t_{rr}	Reverse Recovery Time	I_F = 3.3 A, di/dt = 100 A/μs		33	54	ns
Q_{rr}	Reverse Recovery Charge			23	38	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 125 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. Starting T_J = 25 °C; N-ch: L = 1.0 mH, I_{AS} = 5.0 A, V_{DD} = 90 V, V_{GS} = 10 V.

4. The diode connected between gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics T_J = 25 °C unless otherwise noted

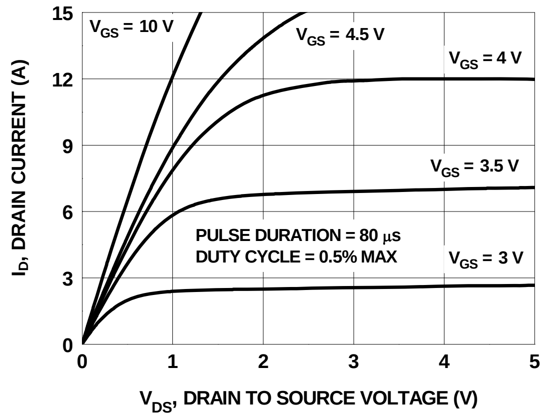


Figure 1. On Region Characteristics

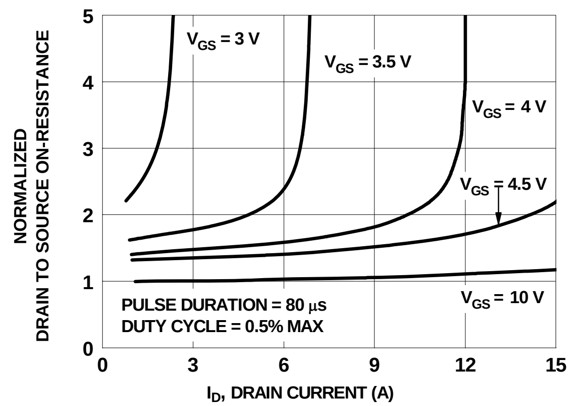


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

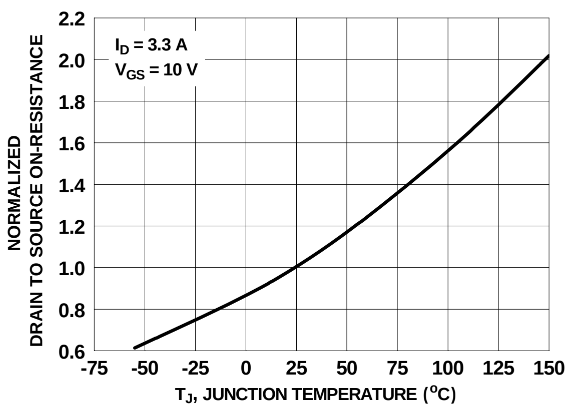


Figure 3. Normalized On Resistance vs Junction Temperature

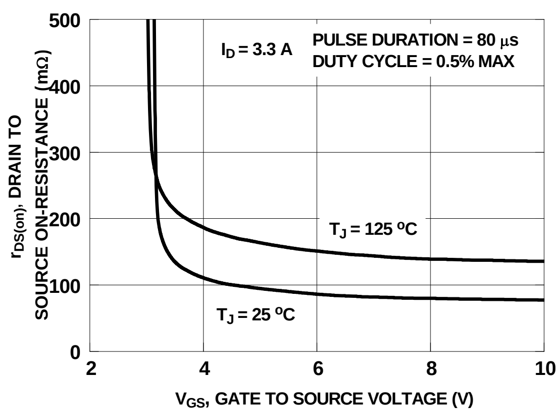


Figure 4. On-Resistance vs Gate to Source Voltage

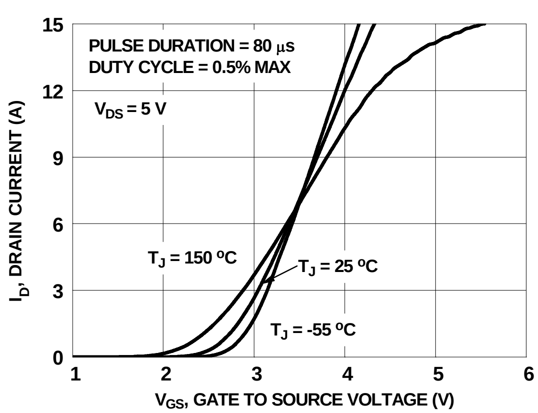


Figure 5. Transfer Characteristics

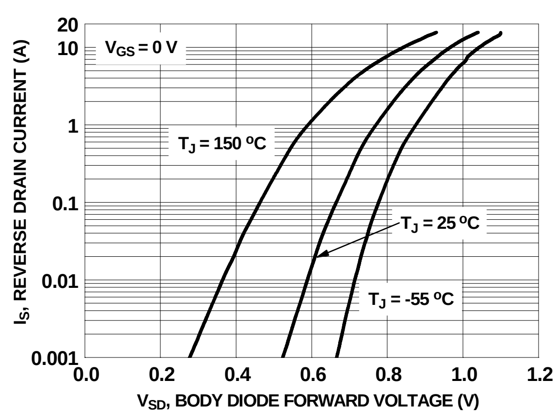


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

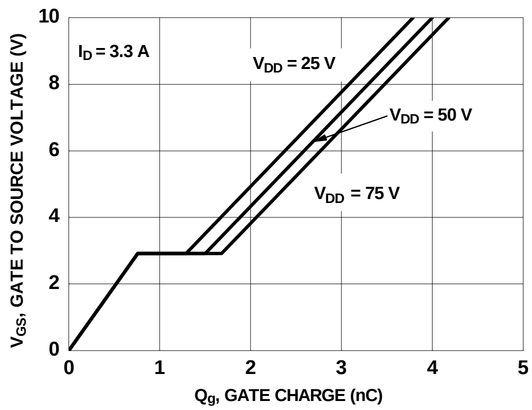


Figure 7. Gate Charge Characteristics

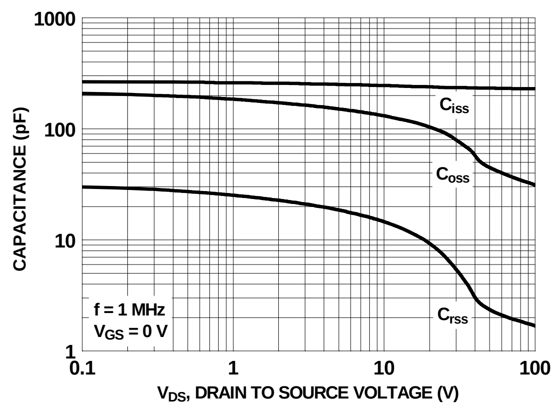


Figure 8. Capacitance vs Drain to Source Voltage

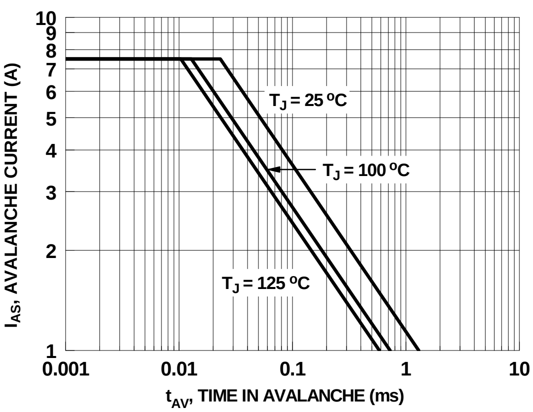


Figure 9. Unclamped Inductive Switching Capability

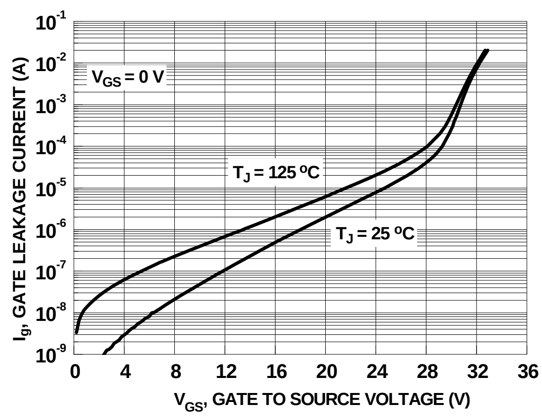


Figure 10. Gate Leakage Current vs Gate to Source Voltage

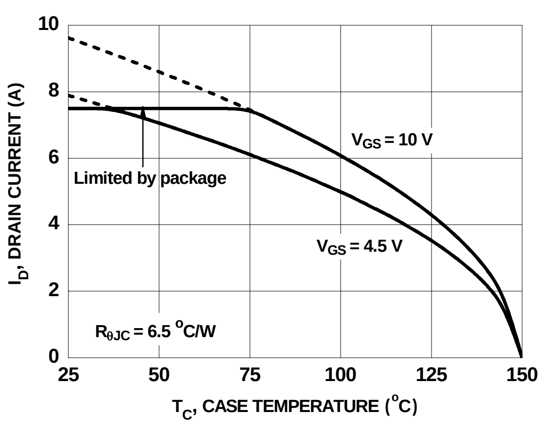


Figure 11. Maximum Continuous Drain Current vs Case Temperature

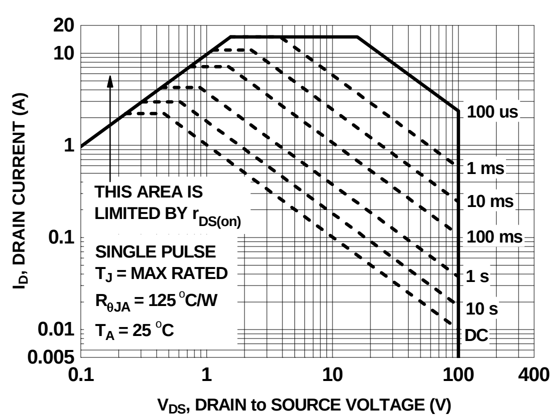


Figure 12. Forward Bias Safe Operating Area

Typical Characteristics T_J = 25 °C unless otherwise noted

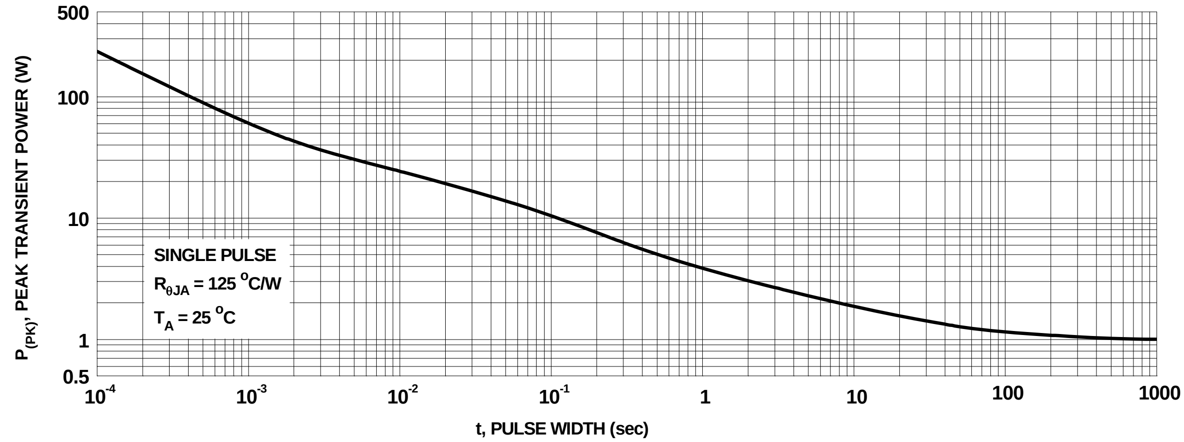


Figure 13. Single Pulse Maximum Power Dissipation

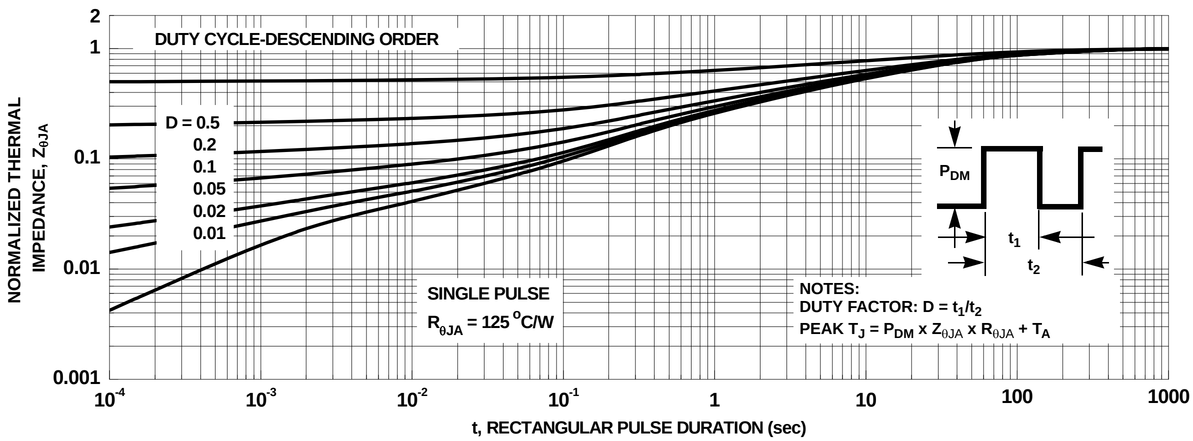
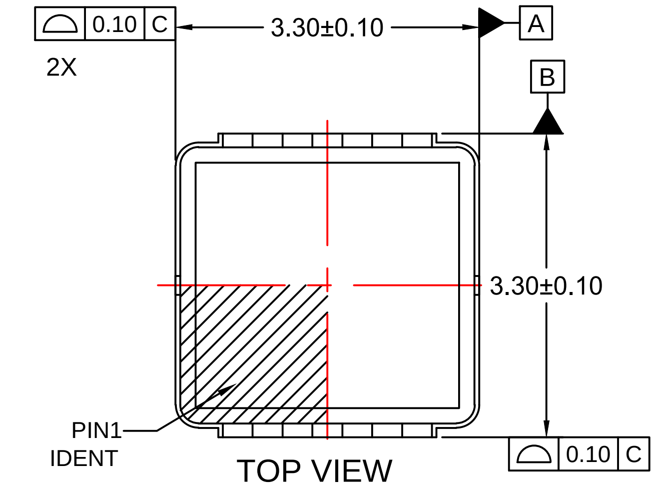
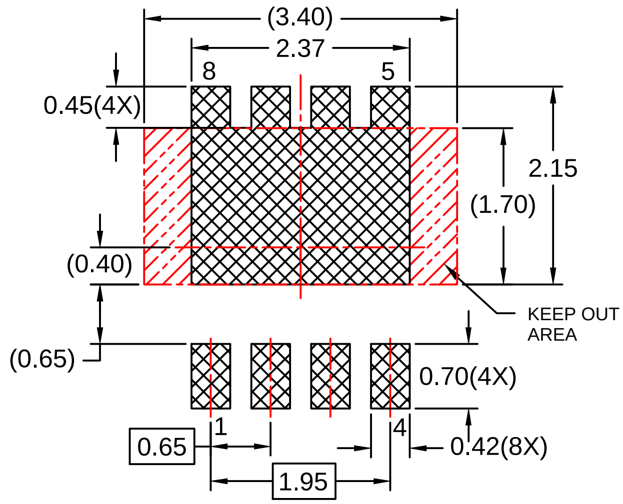


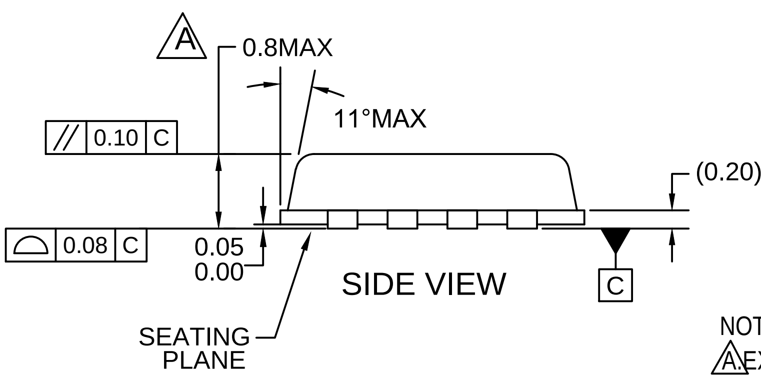
Figure 14. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout



TOP VIEW





SIDE VIEW

RECOMMENDED LAND PATTERN

NOTES:

A. EXCEPT AS NOTED, PACKAGE CONFORMS TO JEDEC REGISTRATION MO-240 VARIATION BA..

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M,1994.

D. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY

E. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATEBURRS.

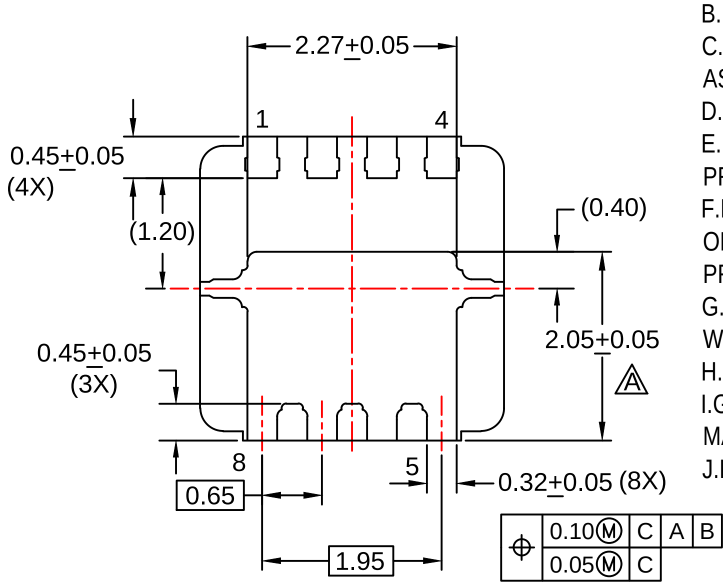
F. FLANGE DIMENSIONS INCLUDE INTERTERMINAL FLASH OR PROTRUSION. INTERTERMINAL FLASH OR PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.

G. IT IS RECOMMENDED TO HAVE NO TRACES OR VIA WITHIN THE KEEP OUT AREA.

H. DRAWING FILENAME: MKT-MLP08Trev3.

I. GENERAL RADII FOR ALL CORNERS SHALL BE 0.20MM MAX.

J. FAIRCHILD SEMICONDUCTOR.



BOTTOM VIEW

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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