FAIRCHILD SEMICONDUCTOR®

February 2007

FDMB668P

P-Channel 1.8V Logic Level PowerTrench® MOSFET

-20V, -6.1A, 35mΩ

Features

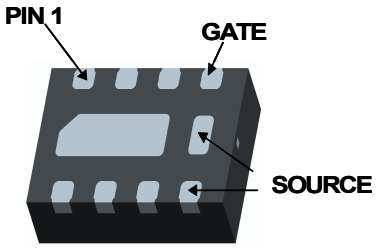
- Max $r_{DS(on)}$ = 35mΩ at V_{GS} = -4.5V, I_D = -6.1A
- Max $r_{DS(on)}$ = 50mΩ at V_{GS} = -2.5V, I_D = -5.1A
- Max $r_{DS(on)}$ = 70mΩ at V_{GS} = -1.8V, I_D = -4.3A
- Excellent for portable application at V_{GS} = -1.8V
- Thin profile - Maximum height = 0.8mm
- RoHS compliant

General Description

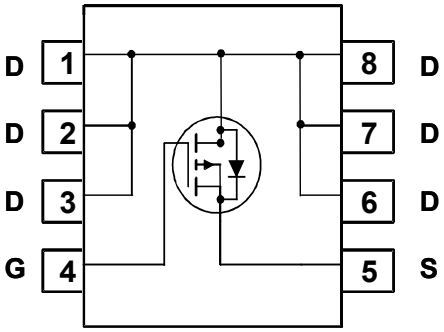
FDMB668P is excellent for load switch and DC-DC conversion among portable electronics. It achieves an optimal balance among efficiency, thermal transfer and small form by integrating a P-channel MOSFET with minimized on-state resistance into a MicroFET 3x1.9 package. When optimizing the dimension of portable applications, this little device offers a very efficient solution.

Applications

- Load Switch in:
  - -HDD
  - -Portable Gaming, MP3
  - -Notebook
- DC/DC Conversion



MicroFET 3X1.9



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DS}	Drain to Source Voltage		-20	V
V_{GS}	Gate to Source Voltage		±8	V
I_D	Drain Current -Continuous	(Note 1a)	-6.1	A
	-Pulsed		-40	
P_D	Power Dissipation	(Note 1a)	1.9	W
	Power Dissipation	(Note 1b)	0.8	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	65	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	165	

Package Marking and Ordering Information

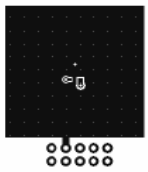
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
668	FDMB668P	MicroFET 3X1.9	7”	8mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250μA, V_{GS} = 0V	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250μA, referenced to 25°C		-11.4		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16V, V_{GS} = 0V			-1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8V, V_{DS} = 0V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250μA	-0.4	-0.6	-1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250μA, referenced to 25°C		2.8		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = -4.5V, I_D = -6.1A		22	35	mΩ
		V_{GS} = -2.5V, I_D = -5.1A		27	50	
		V_{GS} = -1.8V, I_D = -4.3A		35	70	
		V_{GS} = -4.5V, I_D = -6.1A, T_J = 125°C		31	50	
g_{FS}	Forward Transconductance	V_{DS} = -4.5V, I_D = -6.1A		27		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -10V, V_{GS} = 0V, f = 1MHz		1565	2085	pF
C_{oss}	Output Capacitance			210	280	pF
C_{rss}	Reverse Transfer Capacitance			175	265	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -10V, I_D = -6.1A, V_{GS} = -4.5V, R_{GEN} = 6Ω		7	14	ns
t_r	Rise Time			9	18	ns
$t_{d(off)}$	Turn-Off Delay Time			176	282	ns
t_f	Fall Time			84	135	ns
Q_g	Total Gate Charge	V_{GS} = 0V to -10V; V_{DD} = -10V, I_D = -6.1A		42	59	nC
Q_g	Total Gate Charge	V_{GS} = 0V to -5V; V_{DD} = -10V, I_D = -6.1A		22	31	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = -10V, I_D = -6.1A		3		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = -10V, I_D = -6.1A		5		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = -1.6A (Note 2)		-0.7	-1.2	V
t_{rr}	Reverse Recovery Time	I_F = -6.1A, di/dt = 100A/μs		29	44	ns
Q_{rr}	Reverse Recovery Charge			15	23	nC

Notes:

1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to- ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user’s board design.



a) 65°C/W when mounted on a $1in^2$ pad of 2 oz copper

b) 165°C/W when mounted on a minimum pad .

2: Pulse Test: Pulse Width < 300 us, Duty Cycle < 2%.

Typical Characteristics T_J = 25°C unless otherwise noted

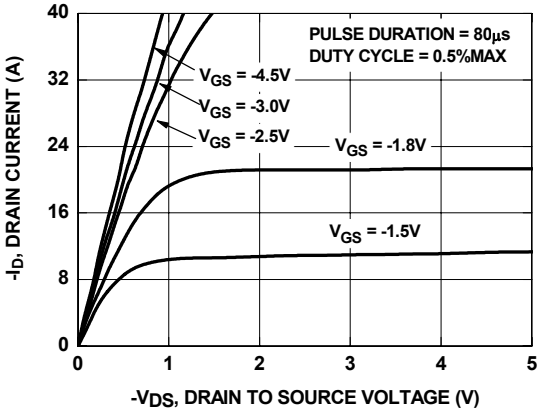


Figure 1. On-Region Characteristics

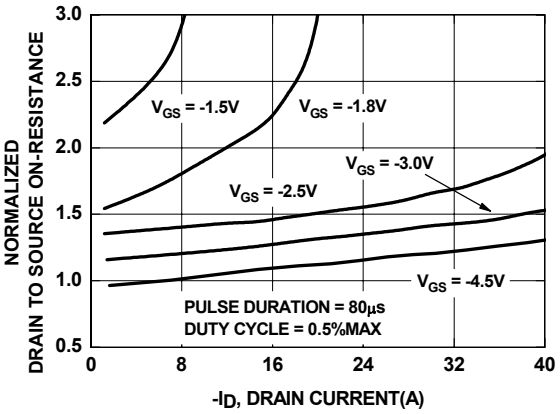


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

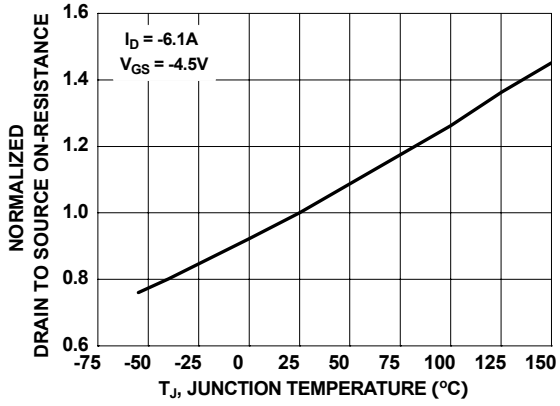


Figure 3. Normalized On-Resistance vs Junction Temperature

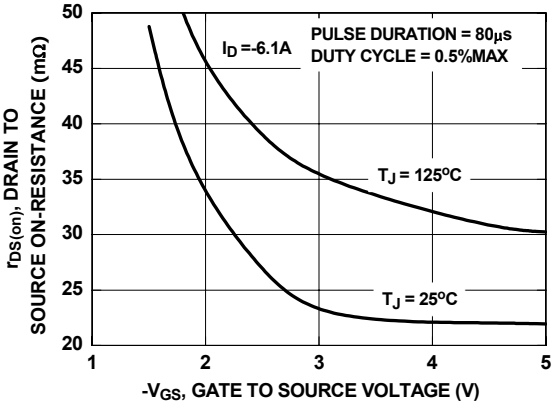


Figure 4. On-Resistance vs Gate to Source Voltage

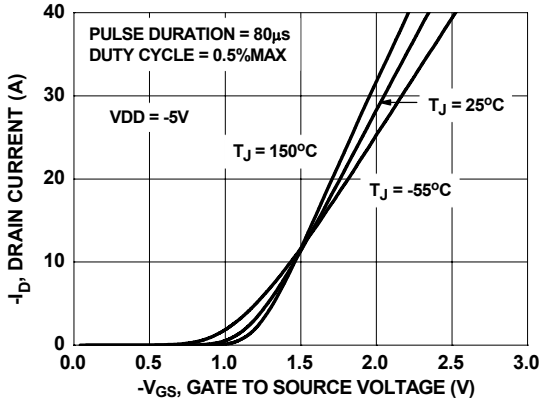


Figure 5. Transfer Characteristics

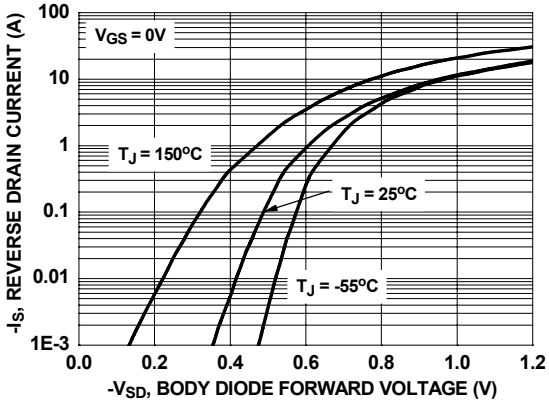


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

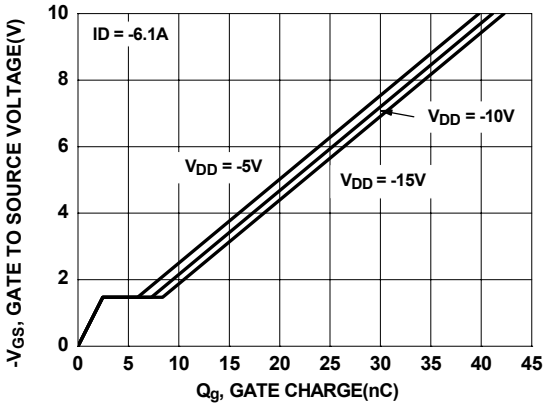


Figure 7. Gate Charge Characteristics

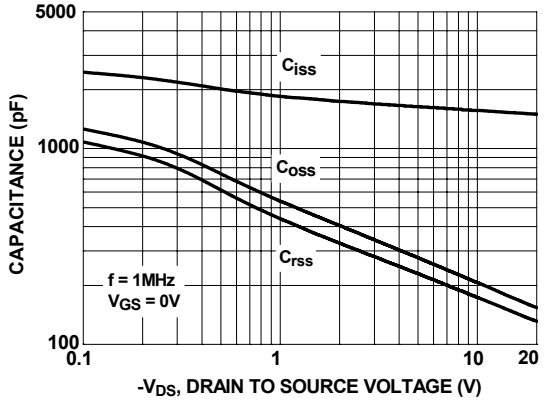


Figure 8. Capacitance vs Drain to Source Voltage

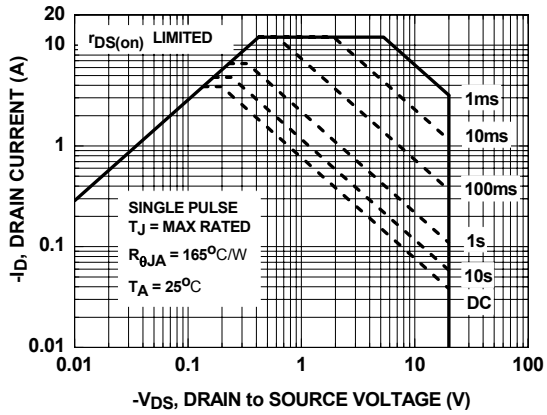


Figure 9. Forward Bias Safe Operating Area

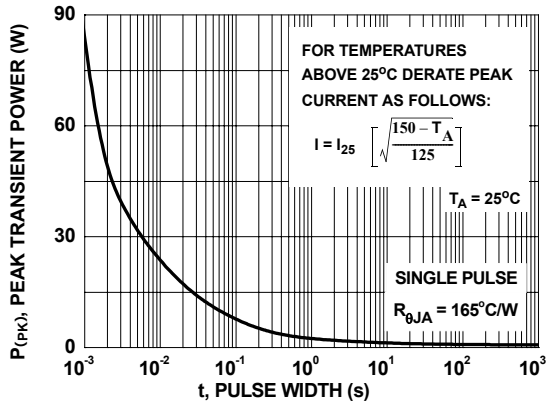


Figure 10. Single Pulse Maximum Power Dissipation

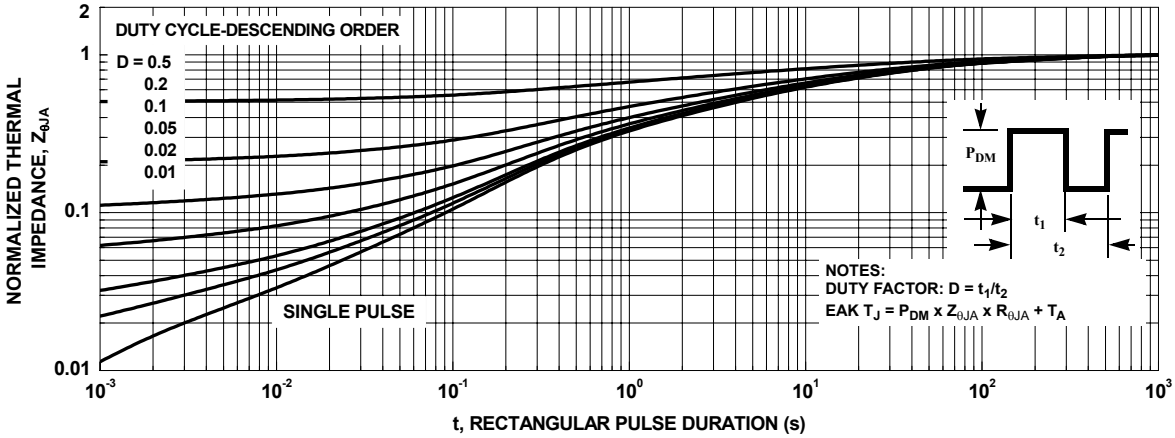
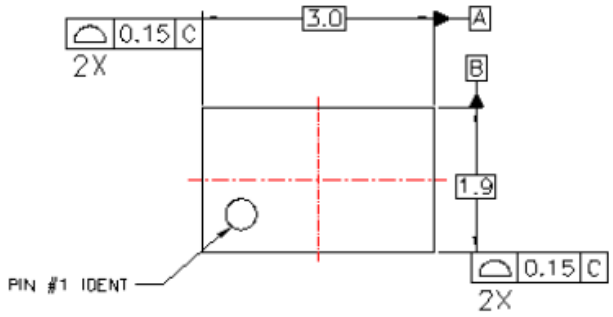
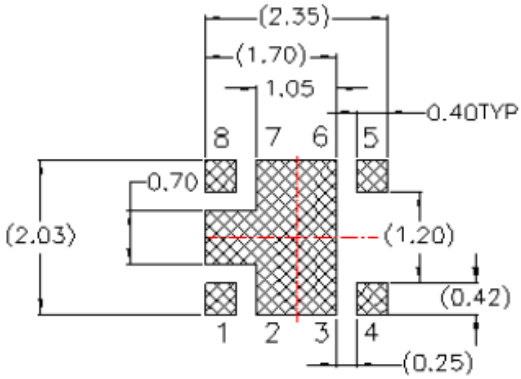


Figure 11. Transient Thermal Response Curve

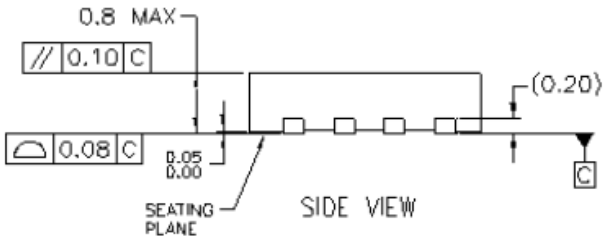
Dimensional Outline and Pad Layout



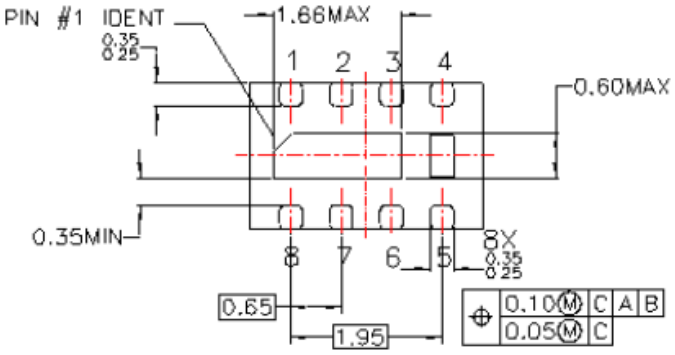
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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Rev. I22