

FDD6N20TM

N-Channel MOSFET

200V, 4.5A, 0.8Ω

Features

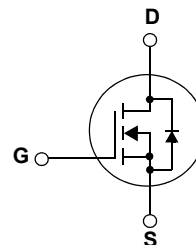
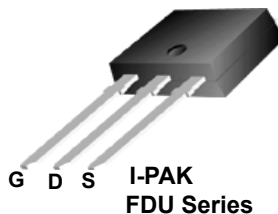
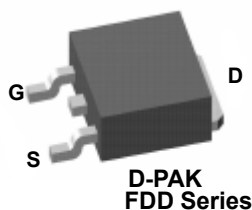
- $R_{DS(on)} = 0.6\Omega$ (Typ.) @ $V_{GS} = 10V$, $I_D = 2.3A$
- Low gate charge (Typ. 4.7nC)
- Low C_{rss} (Typ. 6.3pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- RoHS compliant



Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted*

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	200	V
V_{GSS}	Gate to Source Voltage	± 30	V
I_D	Drain Current	-Continuous ($T_C = 25^\circ\text{C}$)	A
		-Continuous ($T_C = 100^\circ\text{C}$)	
I_{DM}	Drain Current	- Pulsed (Note 1)	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	mJ
I_{AR}	Avalanche Current	(Note 1)	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	V/ns
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	W
		- Derate above 25°C	$W/^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.1	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	110	

Package Marking and Ordering Information $T_C = 25^\circ\text{C}$ unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD6N20	FDD6N20TM	D-PAK	380mm	16mm	2500
FDD6N20	FDD6N20TF	D-PAK	380mm	16mm	2000
FDU6N20	FDU6N20TU	I-PAK	-	-	70

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$, $T_J = 25^\circ\text{C}$	200	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	-	0.28	-	$V/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 200\text{V}$, $V_{GS} = 0\text{V}$	-	-	1	μA
		$V_{DS} = 160\text{V}$, $T_C = 125^\circ\text{C}$	-	-	10	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{V}$, $V_{DS} = 0\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 2.3\text{A}$	-	0.6	0.8	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{V}$, $I_D = 2.3\text{A}$ (Note 4)	-	2.9	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	170	230	pF
C_{oss}	Output Capacitance		-	45	60	pF
C_{rss}	Reverse Transfer Capacitance		-	6.3	9.5	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 160\text{V}$, $I_D = 6\text{A}$ $V_{GS} = 10\text{V}$ (Note 4, 5)	-	4.7	6.1	nC
Q_{gs}	Gate to Source Gate Charge		-	1.2	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	2.2	-	nC

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 100\text{V}$, $I_D = 6\text{A}$ $R_G = 25\Omega$ (Note 4, 5)	-	8.3	26.7	ns
t_r	Turn-On Rise Time		-	5.6	21.2	ns
$t_{d(off)}$	Turn-Off Delay Time		-	15	40	ns
t_f	Turn-Off Fall Time		-	12.8	35.5	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	4.5	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	18	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _{SD} = 4.5A	-	-	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0V, I _{SD} = 6A	-	120	-	ns
Q _{rr}	Reverse Recovery Charge	di _F /dt = 100A/μs (Note 4)	-	0.4	-	μC

Notes:

- 1: Repetitive Rating: Pulse width limited by maximum junction temperature
- 2: $L = 5.9\text{mH}$, $I_{AS} = 4.5\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
- 3: $I_{SD} \leq 4.5\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
- 4: Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
- 5: Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

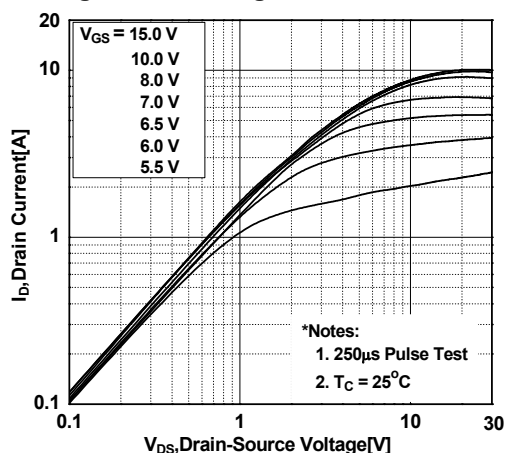


Figure 2. Transfer Characteristics

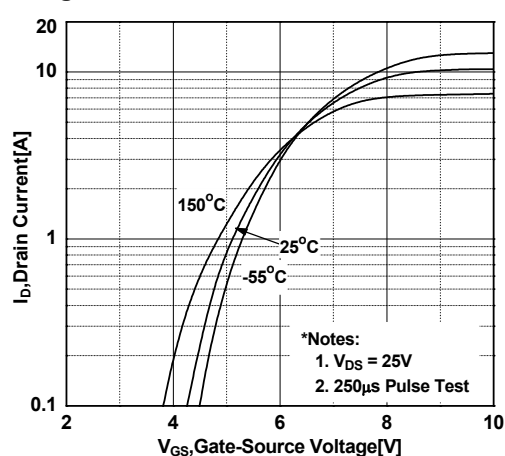


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

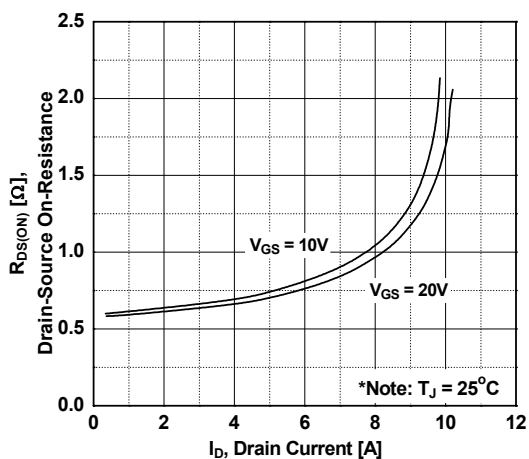


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

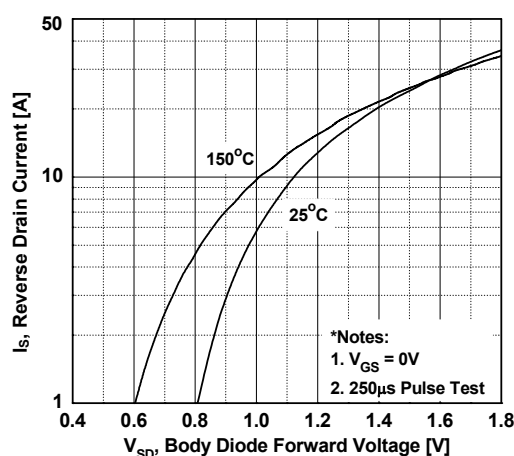


Figure 5. Capacitance Characteristics

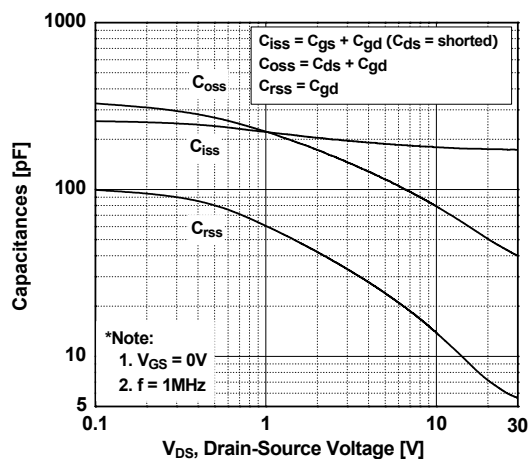
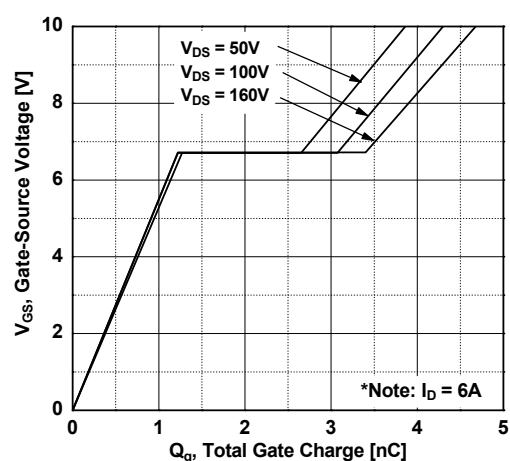


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

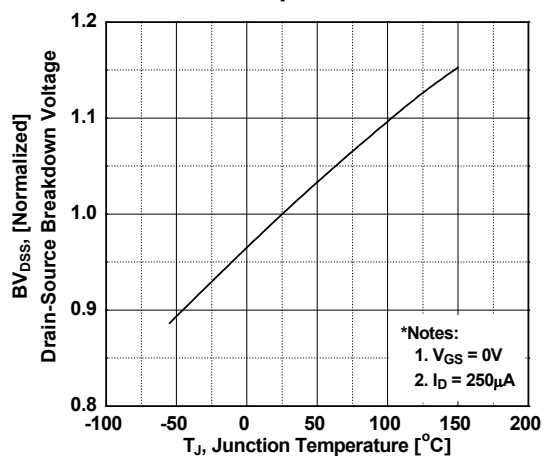


Figure 8. On-Resistance Variation vs. Temperature

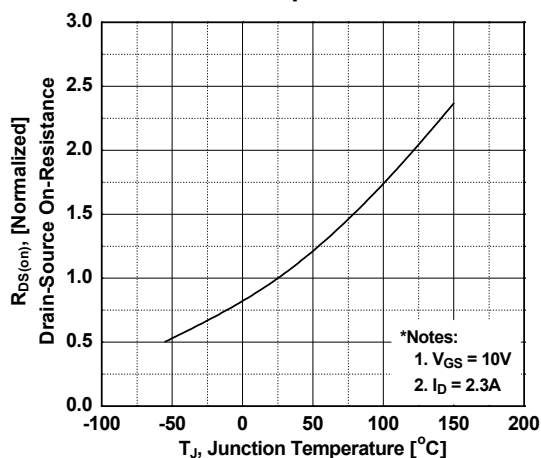


Figure 9. Maximum Safe Operating Area

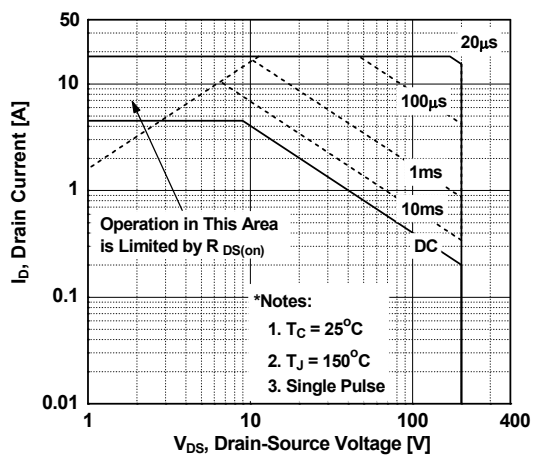


Figure 10. Maximum Drain Current vs. Case Temperature

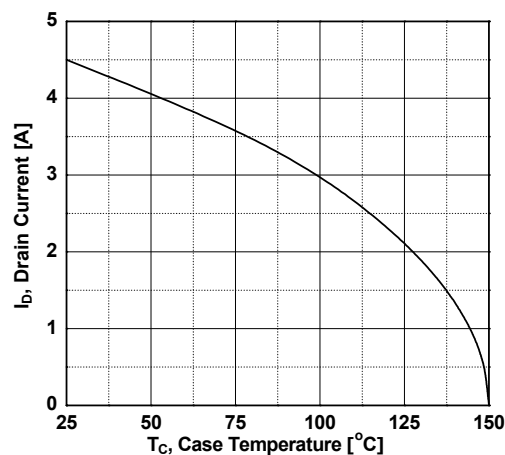
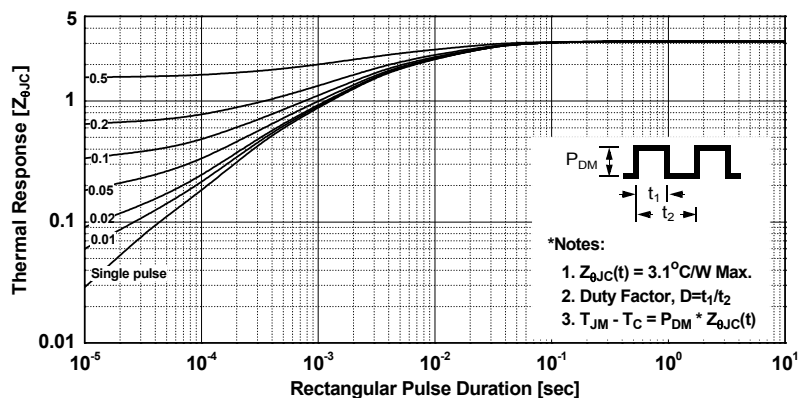
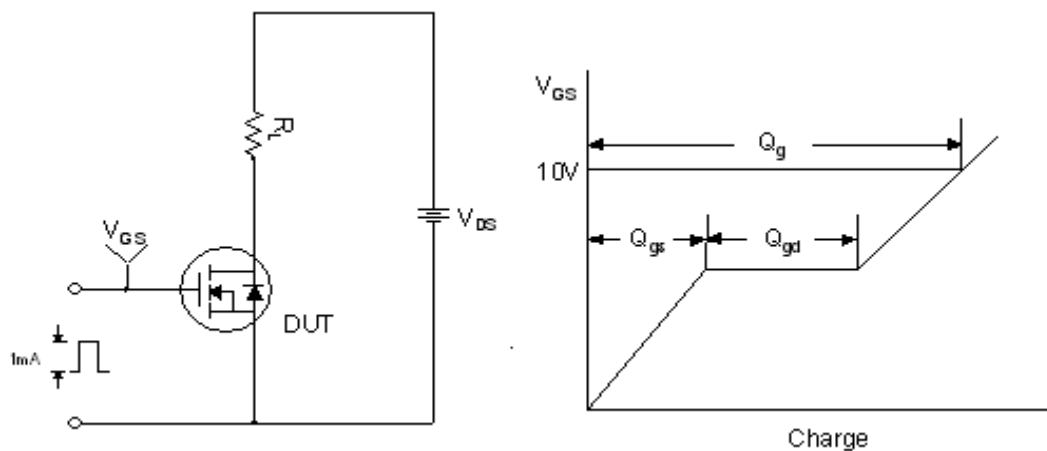


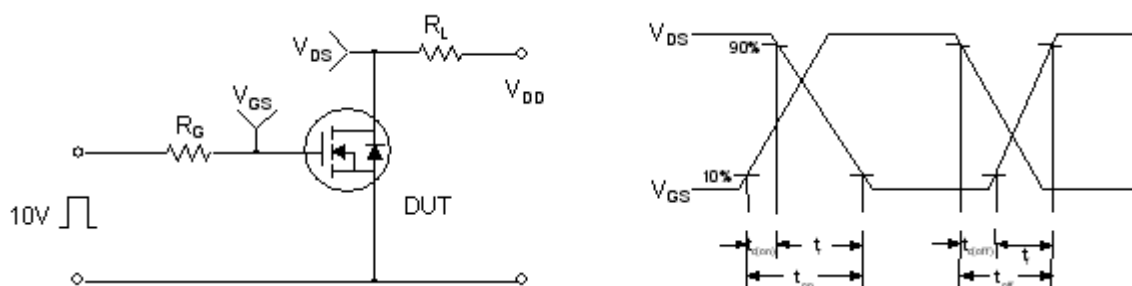
Figure 11. Transient Thermal Response Curve



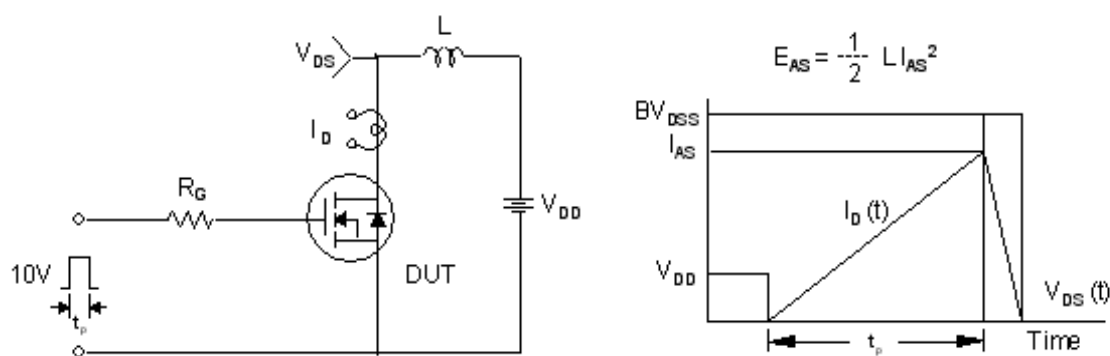
Gate Charge Test Circuit & Waveform



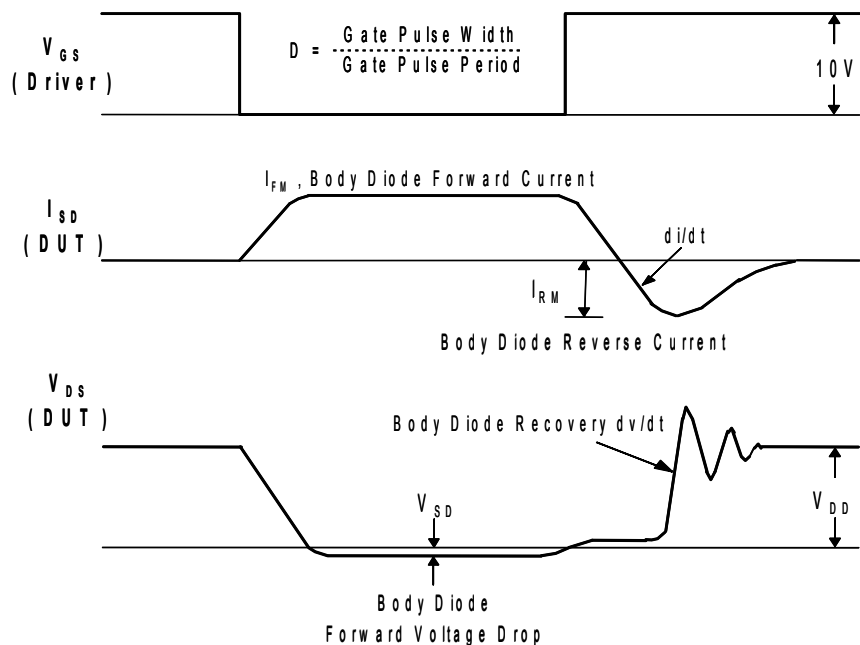
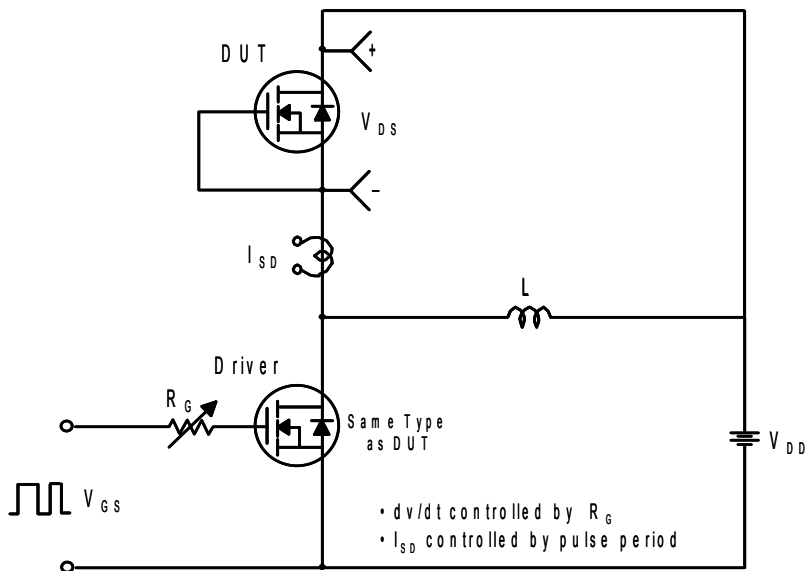
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

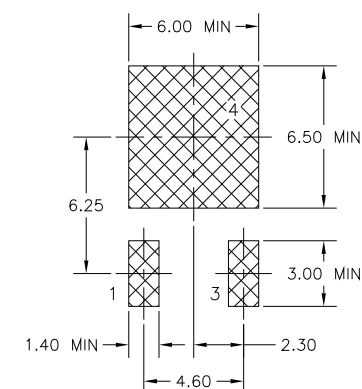
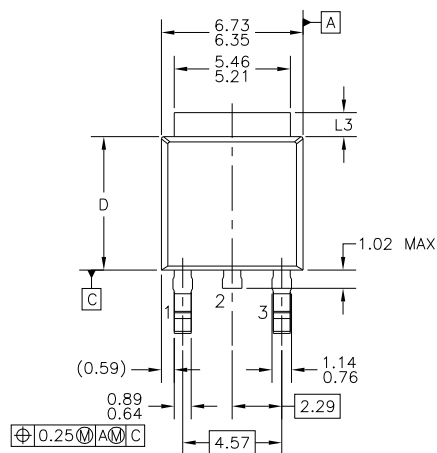


Peak Diode Recovery dv/dt Test Circuit & Waveforms

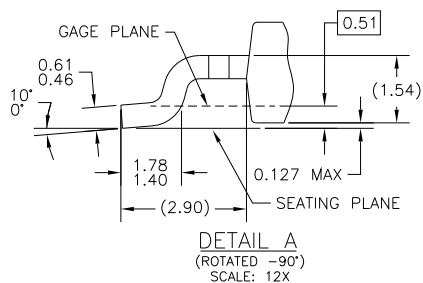
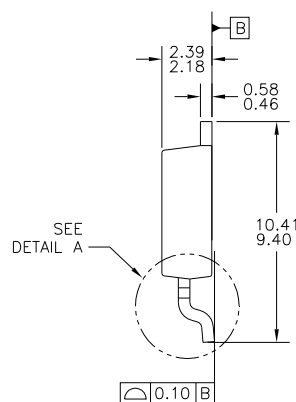
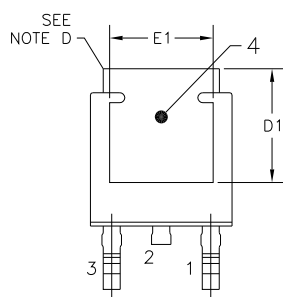


Mechanical Dimensions

D-PAK



LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED

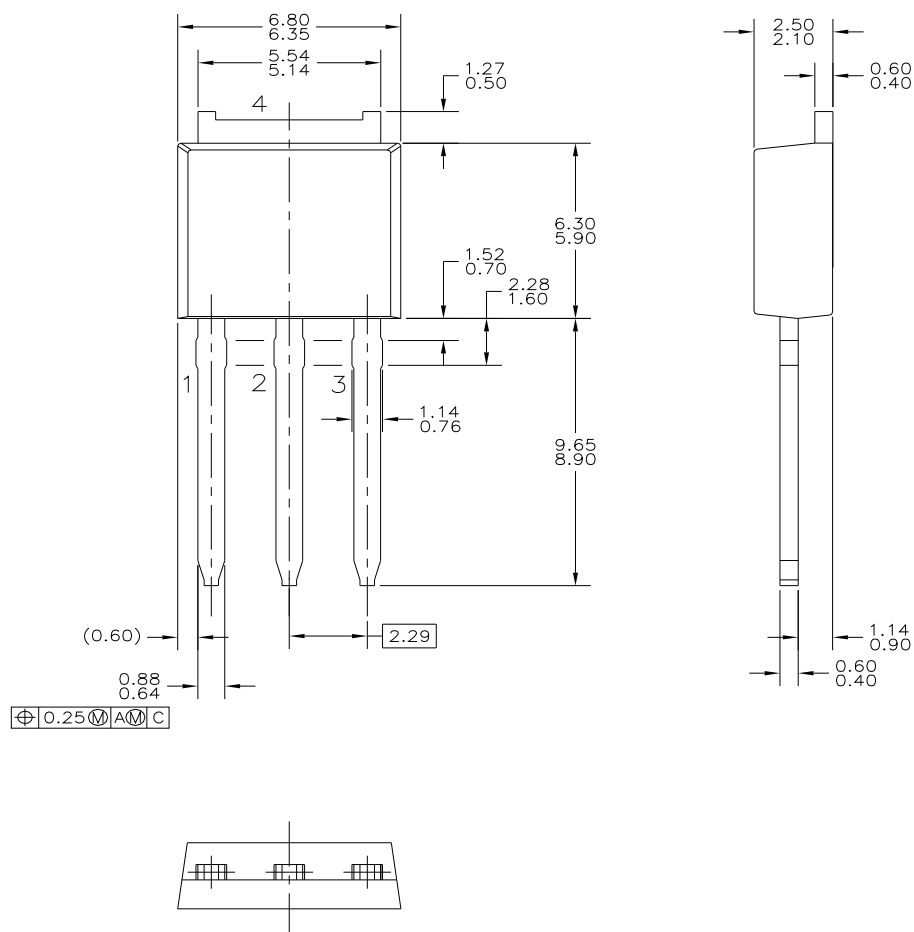
- ALL DIMENSIONS ARE IN MILLIMETERS.
- THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
- DIMENSIONS L3, D, E1 & D1 TABLE:

	OPTION AA	OPTION AB
L3	0.89-1.27	1.52-2.03
D	5.97-6.22	5.33-5.59
E1	4.32 MIN	3.81 MIN
D1	5.21 MIN	4.57 MIN

- PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

Mechanical Dimensions

I-PAK





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FastvCore™	OPTOPLANAR®	STEALTH™	µSerDes™
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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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