FAIRCHILD SEMICONDUCTOR®

January 2009

FDD6776A / FDU6776A_F071

N-Channel PowerTrench® MOSFET

25 V, 7.5 mΩ

Features

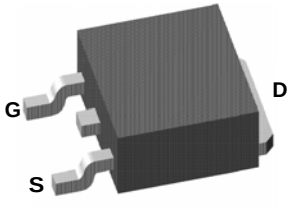
- Max $r_{DS(on)}$ = 7.5 mΩ at V_{GS} = 10 V, I_D = 17.7 A
- Max $r_{DS(on)}$ = 17.0mΩ at V_{GS} = 4.5 V, I_D = 13.2 A
- 100% UIL test
- RoHS Compliant

General Description

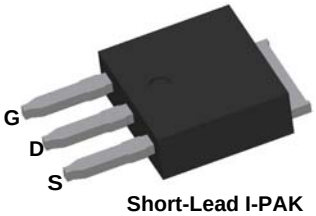
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$ and fast switching speed.

Applications

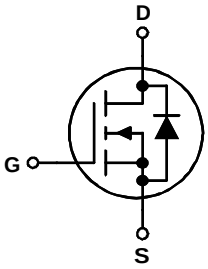
- Vcore DC-DC for Desktop Computers and Servers
- VRM for Intermediate Bus Architecture



D-PAK
(TO-252)



Short-Lead I-PAK
(TO-251AA)



MOSFET Maximum Ratings T_C = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			25	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous (Package limited)	T_C = 25 °C		30	A
	-Continuous (Silicon limited)	T_C = 25 °C		54	
	-Continuous	T_A = 25 °C	(Note 1a)	17.7	
	-Pulsed			100	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	32	mJ
P_D	Power Dissipation	T_C = 25 °C		39	W
	Power Dissipation	T_A = 25 °C	(Note 1a)	3.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	40	

Package Marking and Ordering Information

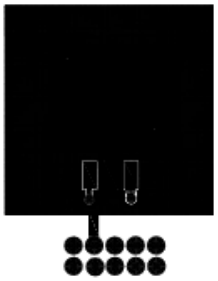
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD6776A	FDD6776A	D-PAK (TO-252)	13 ”	12 mm	2500 units
FDU6776A	FDU6776A_F071	TO-251AA	N/A(Tube)	N/A	75 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		16		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 20 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.0	1.9	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 17.7 A		5.8	7.5	mΩ
		V_{GS} = 10 V, I_D = 17.7 A Short-Lead I-PAK version		6.0	7.7	
		V_{GS} = 4.5 V, I_D = 13.2 A		12.6	17.0	
		V_{GS} = 4.5 V, I_D = 13.2 A Short-Lead I-PAK version		12.8	17.2	
		V_{GS} = 10 V, I_D = 17.7 A, T_J = 150 °C		8.8	11.4	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 17.7 A		84		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 13 V, V_{GS} = 0 V, f = 1 MHz		1120	1490	pF
C_{oss}	Output Capacitance			238	320	pF
C_{rss}	Reverse Transfer Capacitance			221	335	pF
R_g	Gate Resistance			0.9		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 13 V, I_D = 17.7 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		8	16	ns
t_r	Rise Time			5	10	ns
$t_{d(off)}$	Turn-Off Delay Time			18	33	ns
t_f	Fall Time			3	10	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 13 V, I_D = 17.7 A		20	29	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 5 V; V_{DD} = 13 V, I_D = 17.7 A		12	17	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 13 V, I_D = 17.7 A		3.5		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 13 V, I_D = 17.7 A		4.9		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 3.1 A (Note 2)		0.8	1.2	V
		V_{GS} = 0 V, I_S = 17.7 A (Note 2)		0.9	1.3	
t_{rr}	Reverse Recovery Time	I_F = 17.7 A, di/dt = 100 A/μs		17	31	ns
Q_{rr}	Reverse Recovery Charge			5	10	nC

Notes:

1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 40 °C/W when mounted on a 1 in^2 pad of 2 oz copper

b) 96 °C/W when mounted on a minimum pad.

2: Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3: E_{AS} of 32 mJ is based on starting T_J = 25 °C, L = 1 mH, I_{AS} = 8 A, V_{DD} = 23 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 19 A.

Typical Characteristics T_J = 25 °C unless otherwise noted

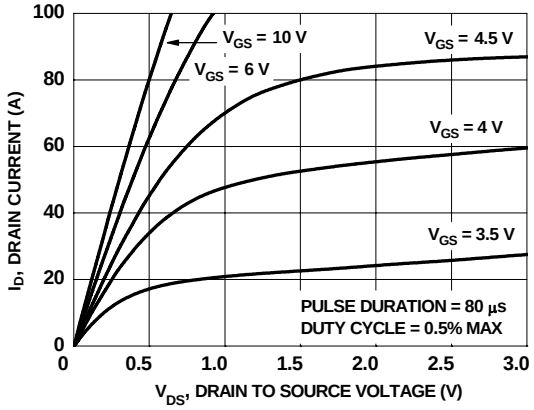


Figure 1. On-Region Characteristics

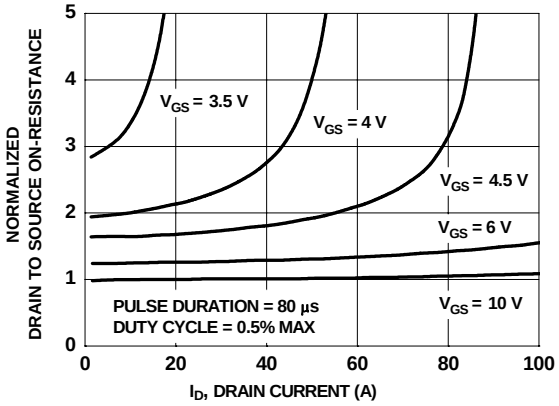


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

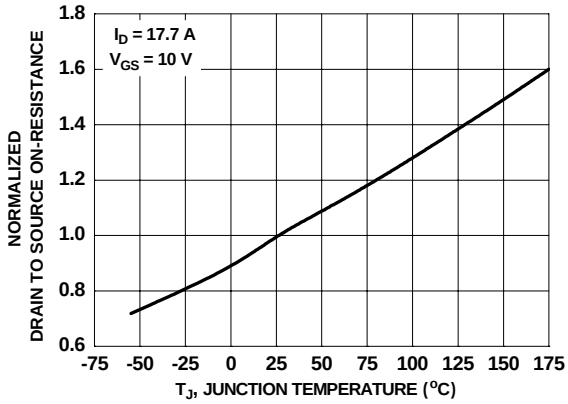


Figure 3. Normalized On-Resistance vs Junction Temperature

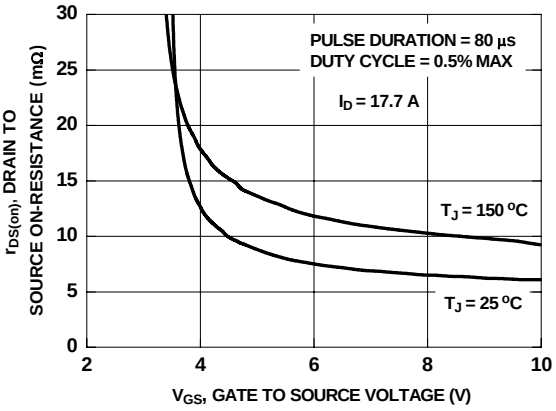


Figure 4. On-Resistance vs Gate to Source Voltage

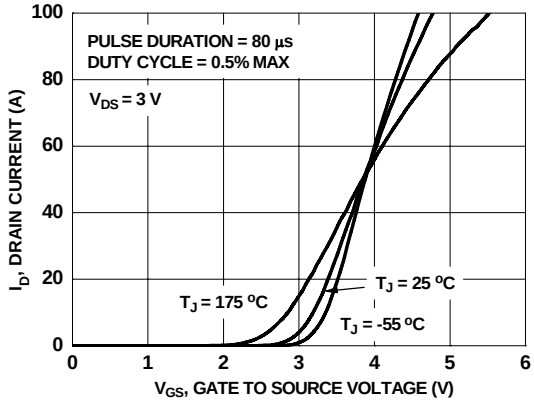


Figure 5. Transfer Characteristics

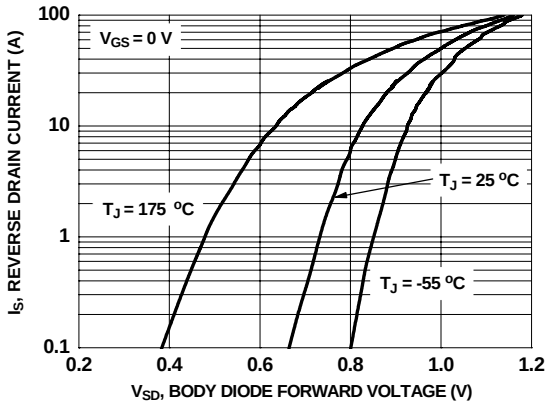


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

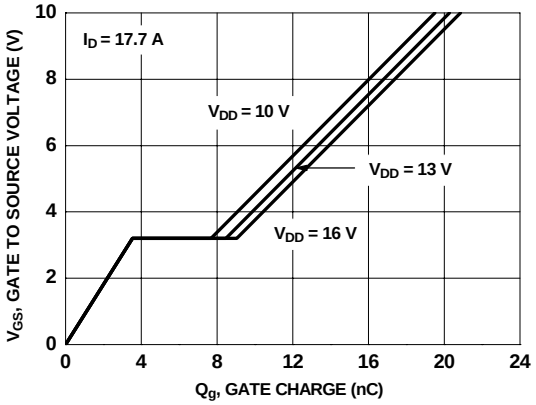


Figure 7. Gate Charge Characteristics

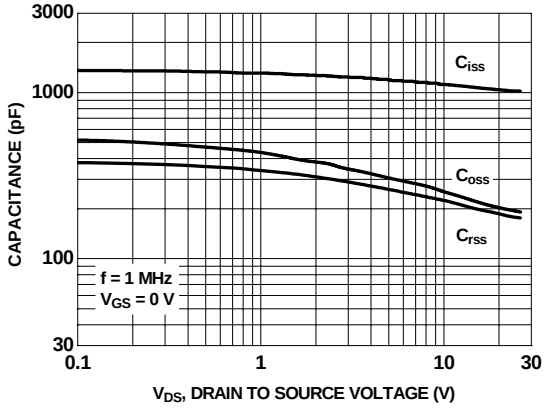


Figure 8. Capacitance vs Drain to Source Voltage

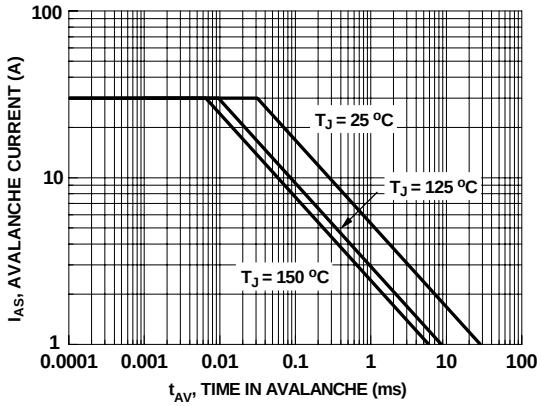


Figure 9. Unclamped Inductive Switching Capability

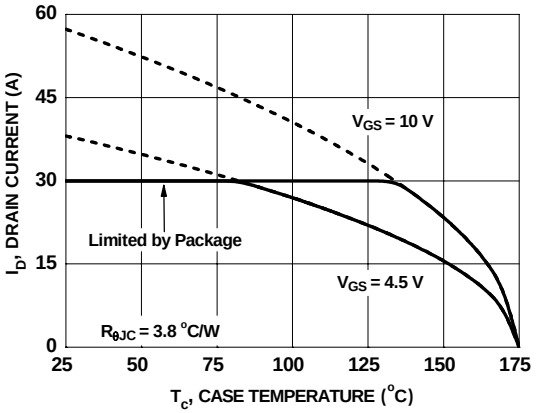


Figure 10. Maximum Continuous Drain Current vs Case Temperature

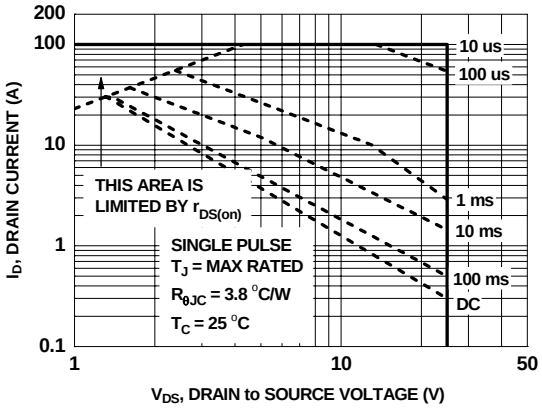


Figure 11. Forward Bias Safe Operating Area

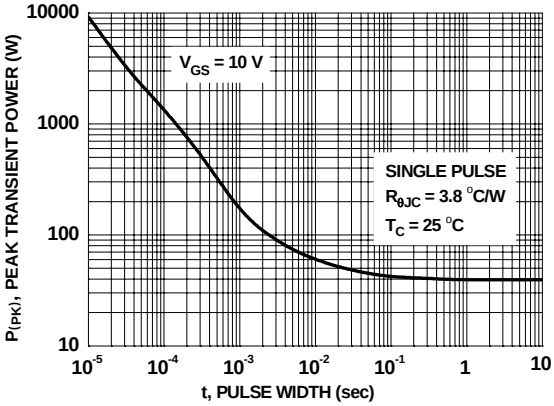


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

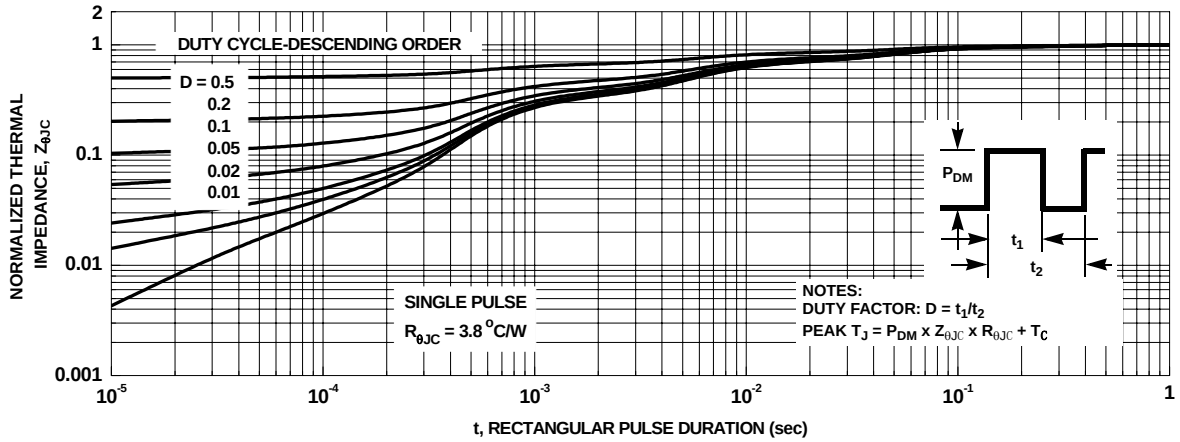


Figure 13. Transient Thermal Response Curve

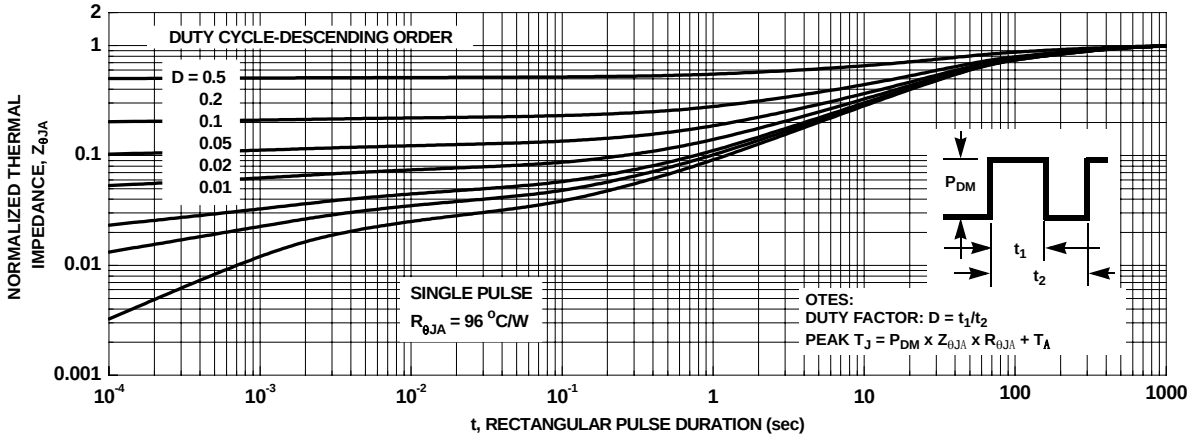


Figure 14. Transient Thermal Response Curve

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