

# FDD6696/FDU6696

## 30V N-Channel PowerTrench<sup>®</sup> MOSFET

### General Description

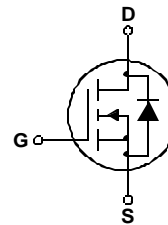
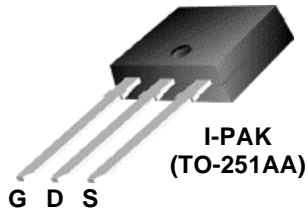
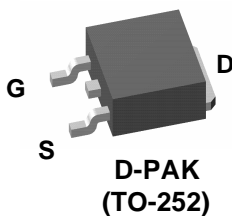
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $R_{DS(ON)}$  and fast switching speed.

### Applications

- DC/DC converter
- Motor drives

### Features

- 50A, 30 V  $R_{DS(ON)} = 8.0 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$   
 $R_{DS(ON)} = 10.7 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$
- Low gate charge (17nC typical)
- Fast switching
- High performance trench technology for extremely low  $R_{DS(ON)}$



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 16$	
$I_b$	Continuous Drain Current @ $T_C=25^\circ\text{C}$ (Note 3)	@ $T_A=25^\circ\text{C}$ (Note 1a)	50
		Pulsed (Note 1a)	13
			100
$P_D$	Power Dissipation @ $T_C=25^\circ\text{C}$ (Note 3)	@ $T_A=25^\circ\text{C}$ (Note 1a)	52
			3.8
		@ $T_A=25^\circ\text{C}$ (Note 1b)	1.6
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +175	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	2.9	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	40	
	Thermal Resistance, Junction-to-Ambient (Note 1b)	96	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape width	Quantity
FDD6696	FDD6696	D-PAK (TO-252)	13"	12mm	2500 units
FDU6696	FDU6696	I-PAK (TO-251)	Tube	N/A	75

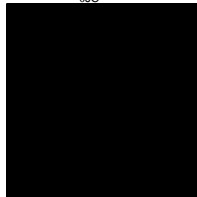
## Electrical Characteristics

T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Drain-Source Avalanche Ratings (Note 2)</b>						
E <sub>AS</sub>	Drain-Source Avalanche Energy	Single Pulse, V <sub>DD</sub> = 15 V, I <sub>b</sub> = 13 A			165	mJ
I <sub>AS</sub>	Drain-Source Avalanche Current				13	A
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>b</sub> = 250 μA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>b</sub> = 250 μA, Referenced to 25°C		23		mV/°C
I <sub>bSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V			10	μA
I <sub>GSSF</sub>	Gate-Body Leakage	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0 V			±100	nA
<b>On Characteristics (Note 2)</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>b</sub> = 250 μA	1	2	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I <sub>b</sub> = 250 μA, Referenced to 25°C		-5		mV/°C
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>b</sub> = 13 A V <sub>GS</sub> = 4.5 V, I <sub>b</sub> = 12 A V <sub>GS</sub> = 10 V, I <sub>b</sub> = 13 A, T <sub>J</sub> = 125°C		6.7 8.6 10.2	8.0 10.7 15.0	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 5 V, I <sub>b</sub> = 13 A		51		S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		1715		pF
C <sub>oss</sub>	Output Capacitance			410		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			180		pF
R <sub>G</sub>	Gate Resistance	V <sub>GS</sub> = 15 mV, f = 1.0 MHz		1.3		Ω
<b>Switching Characteristics (Note 2)</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 15 V, I <sub>b</sub> = 13 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω		13	23	ns
t <sub>r</sub>	Turn-On Rise Time			4	9	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			27	43	ns
t <sub>f</sub>	Turn-Off Fall Time			17	31	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 15 V, I <sub>b</sub> = 13 A, V <sub>GS</sub> = 5 V		17	24	nC
Q <sub>gs</sub>	Gate-Source Charge			5		nC
Q <sub>gd</sub>	Gate-Drain Charge			6		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				13	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 13 A (Note 2)		0.8	1.2	V
t <sub>rr</sub>	Diode Reverse Recovery Time	I <sub>F</sub> = 13 A, dI <sub>F</sub> /dt = 100 A/μs		27		nS
Q <sub>rr</sub>	Diode Reverse Recovery Charge			15		nC

**Notes:**

- R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.



a) R<sub>θJA</sub> = 40°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b) R<sub>θJA</sub> = 96°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

- Maximum current is calculated as: 
$$I_{max} = \sqrt{\frac{P_D}{R_{DS(on)}}}$$
 where P<sub>D</sub> is maximum power dissipation at T<sub>C</sub> = 25°C and R<sub>DS(on)</sub> is at T<sub>J(max)</sub> and V<sub>GS</sub> = 10V. Package current limitation is 21A

## Typical Characteristics

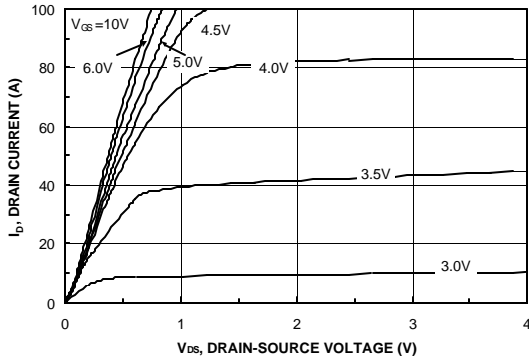


Figure 1. On-Region Characteristics

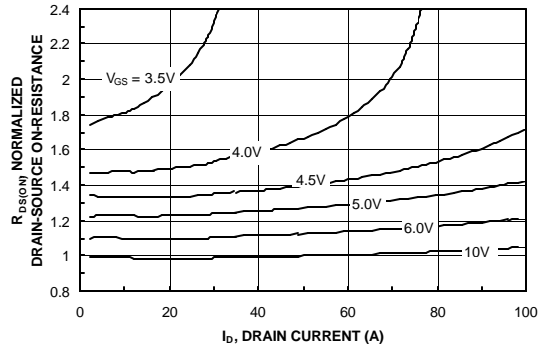


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

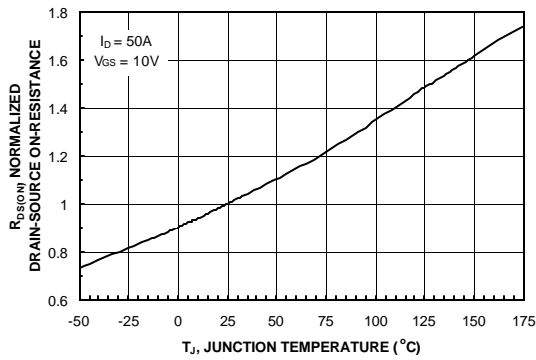


Figure 3. On-Resistance Variation with Temperature

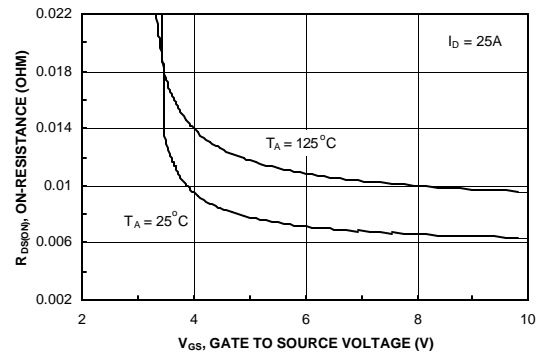


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

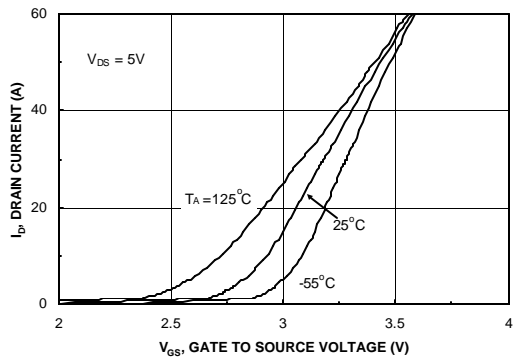


Figure 5. Transfer Characteristics

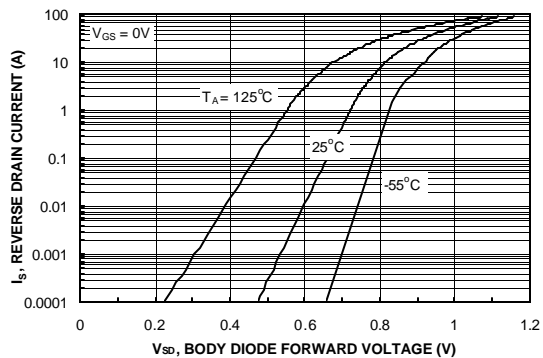


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

## Typical Characteristics

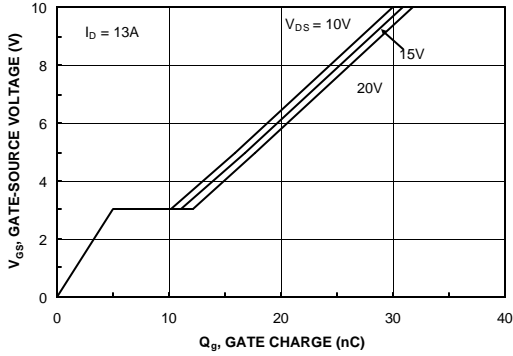


Figure 7. Gate Charge Characteristics

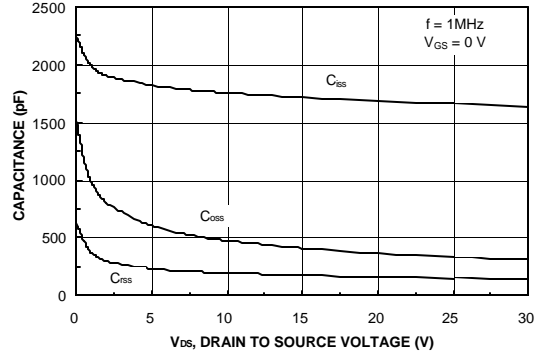


Figure 8. Capacitance Characteristics

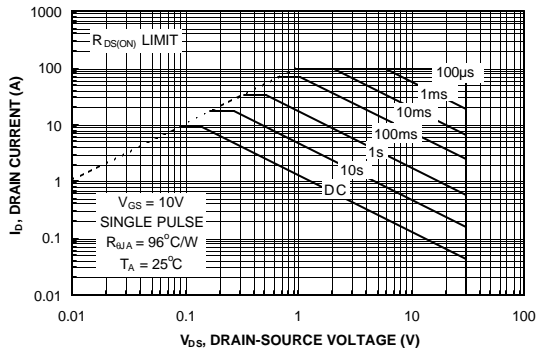


Figure 9. Maximum Safe Operating Area

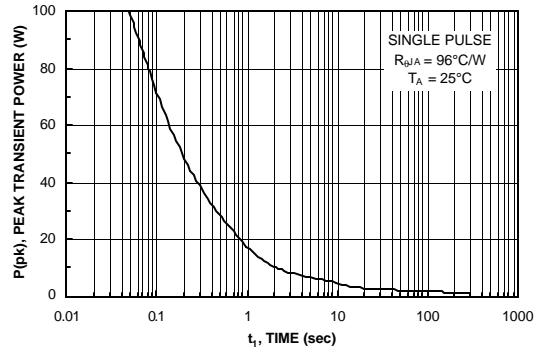


Figure 10. Single Pulse Maximum Power Dissipation

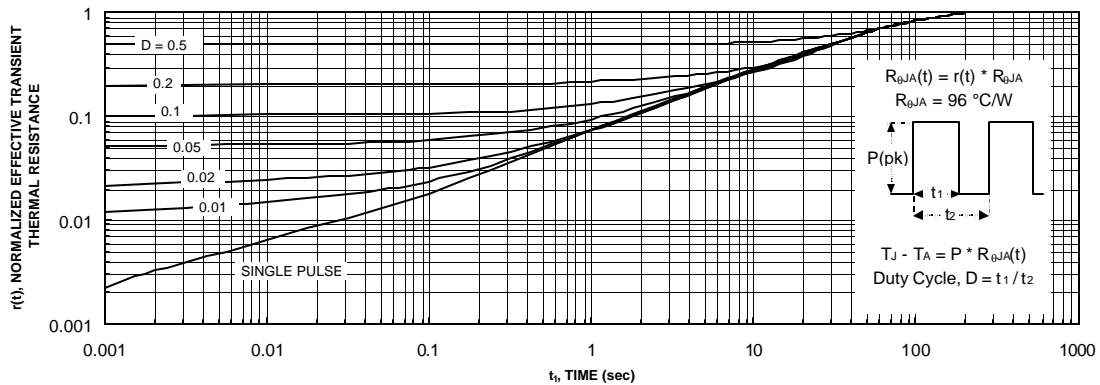


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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