FAIRCHILD SEMICONDUCTOR®

January 2004

# FDC3616N

## 100V N-Channel PowerTrench® MOSFET

### General Description

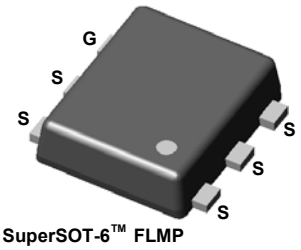
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

### Applications

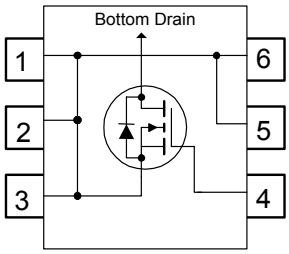
- DC/DC converter
- Load Switching

### Features

- 3.7 A, 100 V. $R_{DS(ON)}$ = 70 mΩ @ $V_{GS}$ = 10 V
  $R_{DS(ON)}$ = 80 mΩ @ $V_{GS}$ = 6.0 V
- High performance trench technology for extremely low $R_{DS(ON)}$
- Low gate charge (23nC typical)
- High power and current handling capability
- Fast switching speed.




SuperSOT-6™ FLMP




## Absolute Maximum Ratings

$T_A$=25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 100 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ± 20 | V |
| $I_D$ | Drain Current – Continuous | (Note 1a) | 3.7 | A |
| | – Pulsed | | 20 | |
| $P_D$ | Maximum Power Dissipation | (Note 1a) | 2 | W |
| | | (Note 1b) | 1.1 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | –55 to +150 | °C |

## Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 60 | °C/W |
| | | (Note 1b) | 111 | |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | | 0.5 | |

## Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|---|---|---|---|---|
| .616 | FDC3616N | 7'' | 8mm | 3000 units |

## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Drain-Source Avalanche Ratings (Note 2)** | | | | | | |
| $W_{DSS}$ | Drain-Source Avalanche Energy | Single Pulse, $V_{DD}$ = 50 V, $I_D$= 3.7A | | | 244 | mJ |
| $I_{AR}$ | Drain-Source Avalanche Current | | | | 3.7 | A |
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 100 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | | 114 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 80 V, $V_{GS}$ = 0 V | | | 10 | μA |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 30 V, $V_{GS}$ = 0 V | | | 1 | μA |
| $I_{GSSF}$ | Gate–Body Leakage, Forward | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | | | 100 | nA |
| $I_{GSSR}$ | Gate–Body Leakage, Reverse | $V_{GS}$ = –20 V, $V_{DS}$ = 0 V | | | –100 | nA |
| **On Characteristics (Note 2)** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 2 | 2.5 | 4 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | | –7.4 | | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 3.7 A<br>$V_{GS}$ = 6.0 V, $I_D$ = 3.5 A<br>$V_{GS}$ = 10 V, $I_D$ = 3.7 A, $T_J$ = 125°C | | 55<br>58<br>104 | 70<br>80<br>139 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 3.7 A | | 19 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 50 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 1215 | | pF |
| $C_{oss}$ | Output Capacitance | | | 72 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 39 | | pF |
| $R_G$ | Gate Resistance | $V_{GS}$ = 15 mV, f = 1.0 MHz | | 1.1 | | Ω |
| **Switching Characteristics (Note 2)** | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = 50 V, $I_D$ = 1 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 9 | 18 | ns |
| $t_r$ | Turn–On Rise Time | | | 4 | 8 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 28 | 45 | ns |
| $t_f$ | Turn–Off Fall Time | | | 10 | 20 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 50 V, $I_D$ = 3.7 A, $V_{GS}$ = 10 V | | 23 | 32 | nC |
| $Q_{gs}$ | Gate–Source Charge | | | 4.8 | | nC |
| $Q_{gd}$ | Gate–Drain Charge | | | 5.4 | | nC |

## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Drain–Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $t_{rr}$ | Diode Reverse Recovery Time | $I_F$ = 3.7 A, $d_{iF}/d_t$ = 100 A/µs | | 41 | | nS |
| $Q_{rr}$ | Diode Reverse Recovery Charge | | | 107 | | nC |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | | | 2.1 | A |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 2.1 A (Note 2) | | 0.75 | 1.2 | V |

**Notes:**

**1.** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 60°C/W when mounted on a 1in$^2$ pad of 2 oz copper

b) 111°C/W when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

**2.** Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

## Typical Characteristics

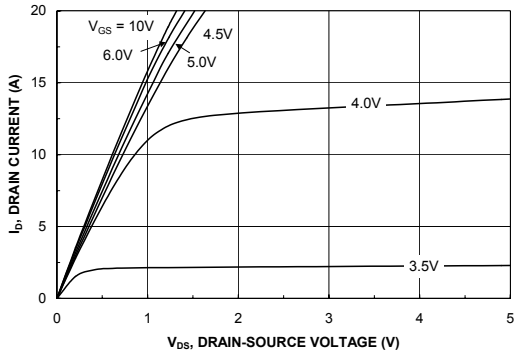



**Figure 1. On-Region Characteristics.**

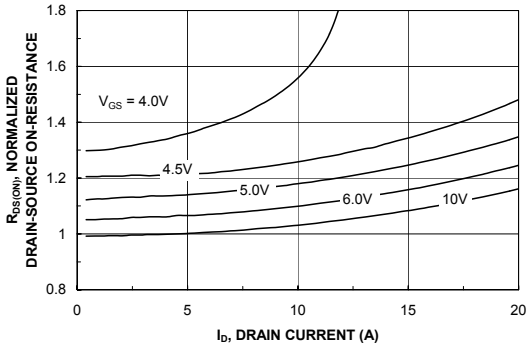



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

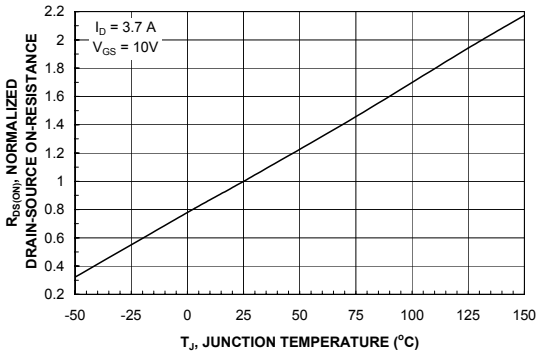



**Figure 3. On-Resistance Variation with Temperature.**

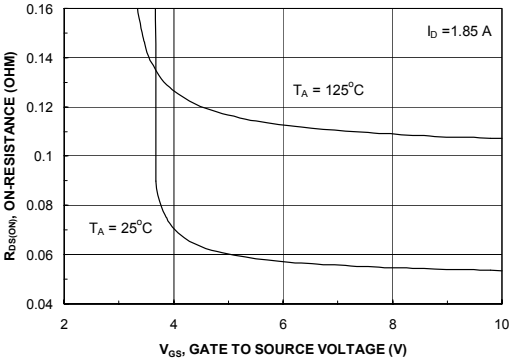



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

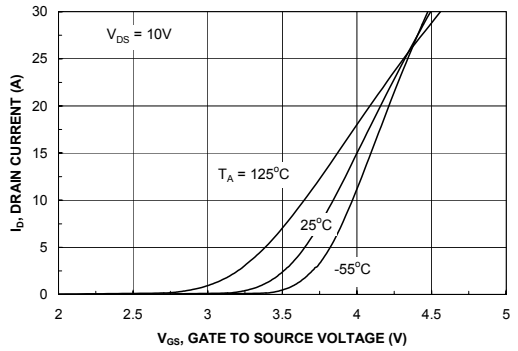



**Figure 5. Transfer Characteristics.**

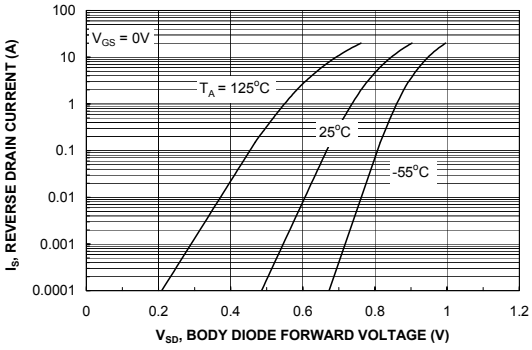



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics

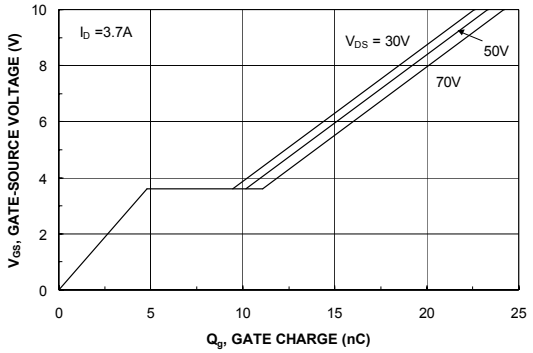



**Figure 7. Gate Charge Characteristics.**

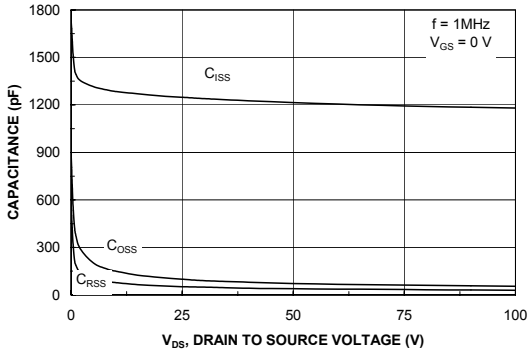



**Figure 8. Capacitance Characteristics.**

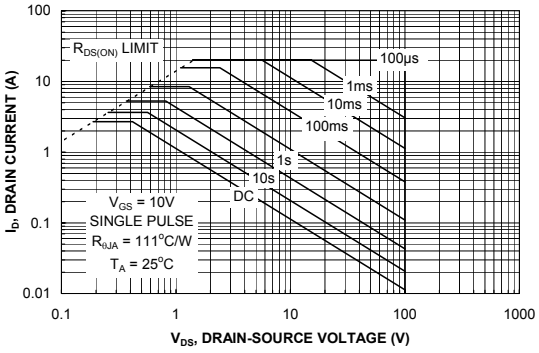



**Figure 9. Maximum Safe Operating Area.**

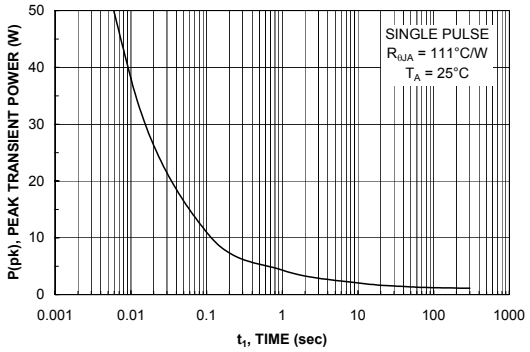



**Figure 10. Single Pulse Maximum Power Dissipation.**

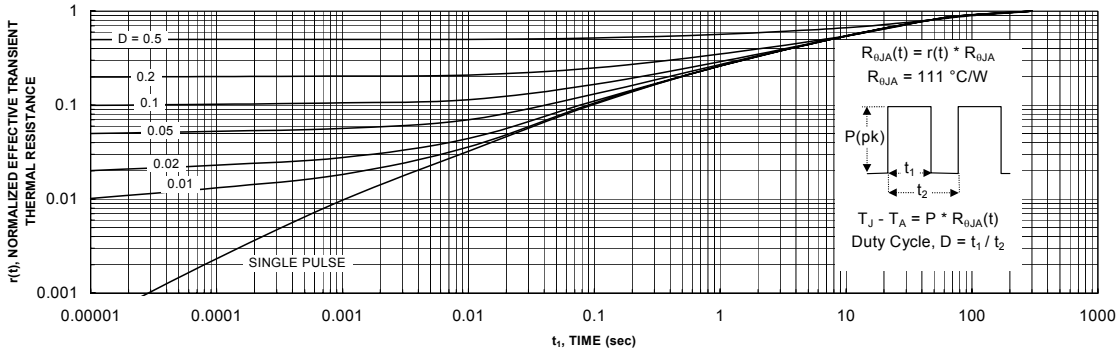
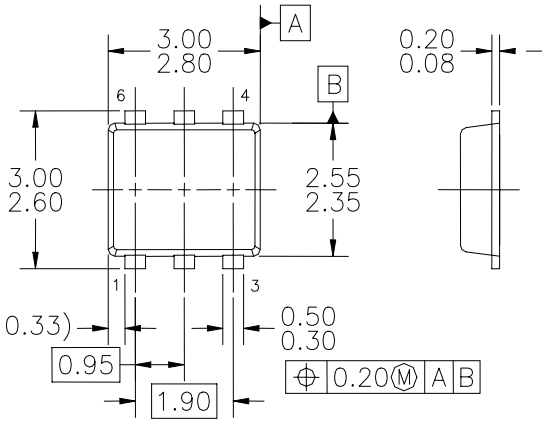
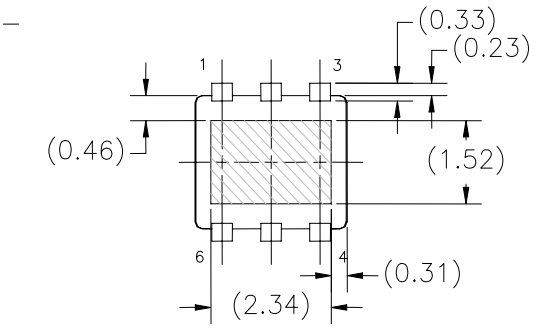



**Figure 11. Transient Thermal Response Curve.**

**Thermal characterization performed using the conditions described in Note 1b.**
**Transient thermal response will change depending on the circuit board design.**

## Dimensional Outline and Pad Layout

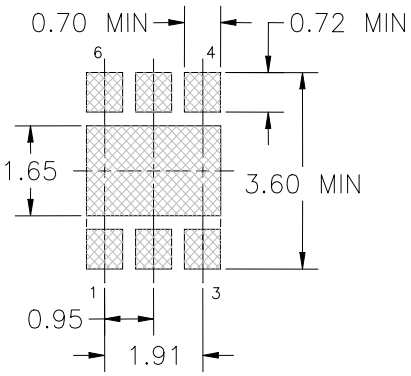


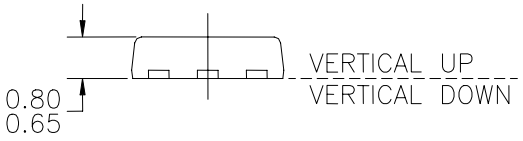




BOTTOM VIEW




LAND PATTERN
RECOMMENDATION




NOTES: UNLESS OTHERWISE SPECIFIED

A) NO PACKAGE STANDARD REFERENCE AS OF MARCH, 2001.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH AND CUTTING BURRS.
D) LEAD TIP BURR:
HORIZONTAL: 0.20 mm MAX
VERTICAL UP: 0.20 mm MAX
VERTICAL DOWN: 0.05 mm MAX

## TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

| | | | | |
|---|---|---|---|---|
| ACEx™ | FACT Quiet Series™ | ISOPLANAR™ | POP™ | SuperFET™ |
| ActiveArray™ | FAST® | LittleFET™ | Power247™ | SuperSOT™-3 |
| Bottomless™ | FASTr™ | MICROCOUPLER™ | PowerTrench® | SuperSOT™-6 |
| CoolFET™ | FPS™ | MicroFET™ | QFET® | SuperSOT™-8 |
| *CROSSVOLT*™ | FRFET™ | MicroPak™ | QS™ | SyncFET™ |
| DOME™ | GlobalOptoisolator™ | MICROWIRE™ | QT Optoelectronics™ | TinyLogic® |
| EcoSPARK™ | GTO™ | MSX™ | Quiet Series™ | TINYOPTO™ |
| $E^2CMOS^{TM}$ | HiSeC™ | MSXPro™ | RapidConfigure™ | TruTranslation™ |
| EnSigna™ | $I^2C$™ | OCX™ | RapidConnect™ | UHC™ |
| FACT™ | ImpliedDisconnect™ | OCXPro™ | SILENT SWITCHER® | UltraFET® |
| Across the board. Around the world.™ | | OPTOLOGIC® | SMART START™ | VCX™ |
| The Power Franchise™ | | OPTOPLANAR™ | SPM™ | |
| Programmable Active Droop™ | | PACMAN™ | Stealth™ | |

### DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.
As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

### PRODUCT STATUS DEFINITIONS

**Definition of Terms**

| Datasheet Identification | Product Status | Definition |
|---|---|---|
| Advance Information | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| No Identification Needed | Full Production | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| Obsolete | Not In Production | This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only. |