

October 2010

FDB8445_F085

N-Channel PowerTrench® MOSFET 40V, 70A, 9m Ω

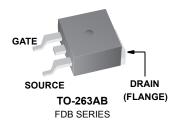
Features

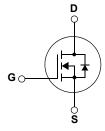
- Typ $r_{DS(on)}$ = 6.8m Ω at V_{GS} = 10V, I_D = 70A
- Typ $Q_{g(10)}$ = 44nC at V_{GS} = 10V
- Low Miller Charge
- Low Q_{rr} Body Diode
- UIS Capability (Single Pulse/ Repetitive Pulse)
- Qualified to AEC Q101
- RoHS Compliant

Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Electronic Transmission
- Distributed Power Architecture and VRMs
- Primary Switch for 12V Systems







Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	40	V
V_{GS}	Gate to Source Voltage	±20	V
	Drain Current Continuous (V _{GS} = 10V) (Note 1)	70	Α
'D	Pulsed	Figure 4	
E _{AS}	Single Pulse Avalanche Energy (Note 2)	102	mJ
В	Power Dissipation	92	W
P_{D}	Derate above 25°C	0.6	W/°C
T _J , T _{STG}	Operating and Storage Temperature	-55 to +175	°C

Thermal Characteristics

$R_{\theta JC}$	Maximum Thermal Resistance, Junction to Case	1.63	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient TO-263, lin ² copper pad area	43	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB8445	FDB8445_F085	TO-263AB	330mm	24mm	800 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics					
B _{VDSS}	Drain to Source Breakdown Voltage	I _D = 250μA, V _{GS} = 0V	40	-	-	V
	Zara Cata Valtaga Drain Current	V _{DS} = 32V	-	-	1	μА
IDSS	Zero Gate Voltage Drain Current	$V_{GS} = 0V$ $T_J = 150^{\circ}C$	-	-	250	μΑ
less	Gate to Source Leakage Current	$V_{GS} = \pm 20V$	-	-	±100	nA

On Characteristics

V_{GS}	S(th)	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2	2.5	4	V
			I _D = 70A, V _{GS} = 10V	-	6.8	9	
r _{DS(}	(on)	Drain to Source On Resistance	I _D = 70A, V _{GS} = 10V, T _J = 175°C	ı	13	17.2	mΩ

Dynamic Characteristics

C _{iss}	Input Capacitance	\\ - 25\\ \\ - 0\\		-	2860	3805	pF
C _{oss}	Output Capacitance	$V_{DS} = 25V, V_{GS}$ f = 1MHz	$V_{DS} = 25V, V_{GS} = 0V,$ f = 1MHz		295	395	pF
C _{rss}	Reverse Transfer Capacitance	1 - 11/11/12			180	270	pF
R_G	Gate Resistance	f = 1MHz		-	1.95	-	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	V _{GS} = 0 to 10V		-	44	62	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0$ to $2V$	V _{DD} =20V,	1	2.9	4.1	nC
Q_{gs}	Gate to Source Gate Charge	Source Gate Charge I _D = 70A,		1	11	1	nC
Q _{gs2}	Gate Charge Threshold to Plateau			-	8.2	-	nC
Q_{gd}	Gate to Drain "Miller" Charge			ı	11	-	nC

Electrical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Switching	g Characteristics					
t _(on)	Turn-On Time		-	-	45	ns
t _{d(on)}	Turn-On Delay Time		-	10	-	ns
t _r	Turn-On Rise Time	$V_{DD} = 20V, I_{D} = 70A$ $V_{GS} = 10V, R_{GS} = 5\Omega$	-	19	-	ns
t _{d(off)}	Turn-Off Delay Time	V_{GS} = 10V, R_{GS} = 5Ω	-	36	-	ns
t _f	Turn-Off Fall Time		-	16	-	ns
t _{off}	Turn-Off Time		-	-	81	ns

Drain-Source Diode Characteristics

V	V _{SD} Source to Drain Diode Voltage	I _{SD} = 70A	-	-	1.25	V
V SD		I _{SD} = 35A	-	-	1.0	٧
t _{rr}	Reverse Recovery Time	$I_F = 70A$, di/dt = $100A/\mu s$	-	-	59	ns
Q _{rr}	Reverse Recovery Charge	$I_F = 70A$, di/dt = $100A/\mu s$	-	-	77	nC

Notes:
1: Maximum wire current carrying capacity is 70A.
2: Starting T_J = 25°C, L = 65uH, I_{AS} = 56A.

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: http://www.aecouncil.com/
All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

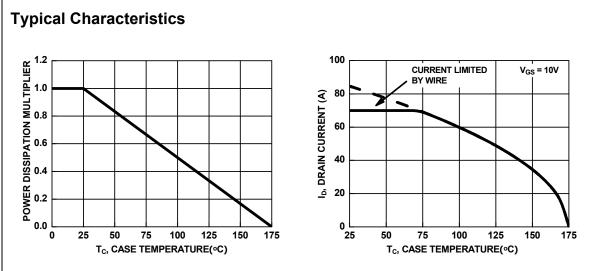


Figure 1. Normalized Power Dissipation vs Case Temperature

Figure 2. Maximum Continuous Drain Current vs Case Temperature

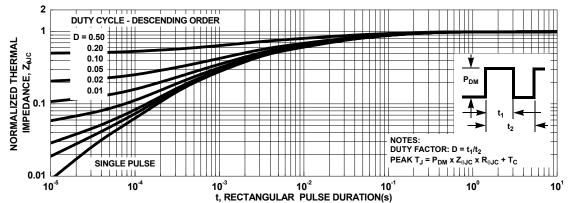


Figure 3. Normalized Maximum Transient Thermal Impedance

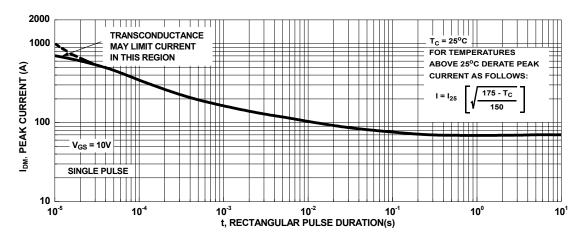


Figure 4. Peak Current Capability

Typical Characteristics

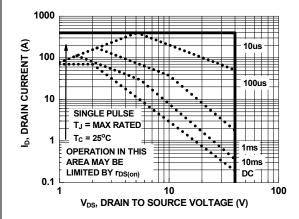
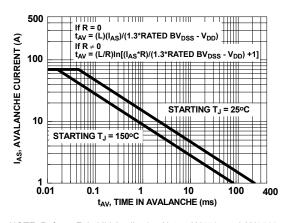


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

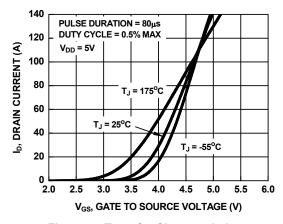


Figure 7. Transfer Characteristics

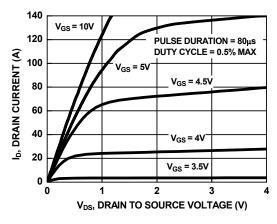


Figure 8. Saturation Characteristics

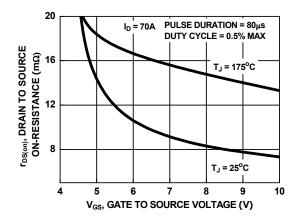


Figure 9. Drain to Source On-Resistance Variation vs Gate to Source Voltage

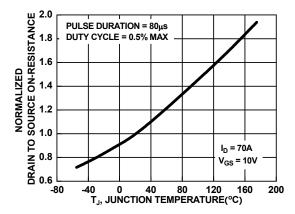


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics

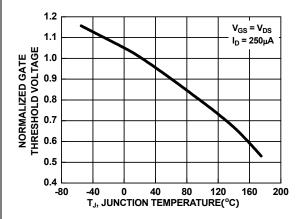


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

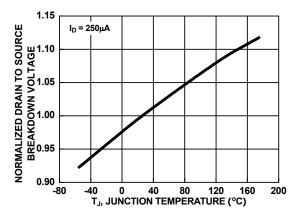


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

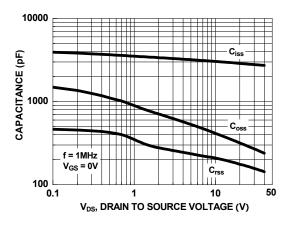


Figure 13. Capacitance vs Drain to Source Voltage

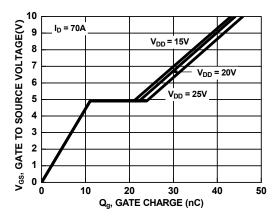


Figure 14. Gate Charge vs Gate to Source Voltage





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