September 2000



FDP4020P/FDB4020P

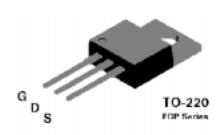
P-Channel 2.5V Specified Enhancement Mode Field Effect Transistor

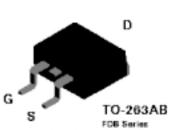
General Description

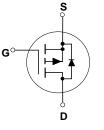
Features

This P-Channel low threshold MOSFET has been designed for use as a linear pass element for low voltage outputs. In addition, the part may be used as a low voltage load switch when switching outputs on or off for power management. The part may also be used in conjunction with DC-DC converters requiring P-Channel.

- -16 A, -20 V. R_{DS(on)} = 0.08 Ω @ V_{GS} = -4.5 V R_{DS(on)} = 0.11 Ω @ V_{GS} = -2.5 V.
 Critical DC electrical parameters specified at elevated temperature.
- High density cell design for extremely low R_{DS(on)}
- TO-220 and TO-263 (D²PAK) package for both through hole and surface mount applications.
- 175°C maximum junction temperature rating.







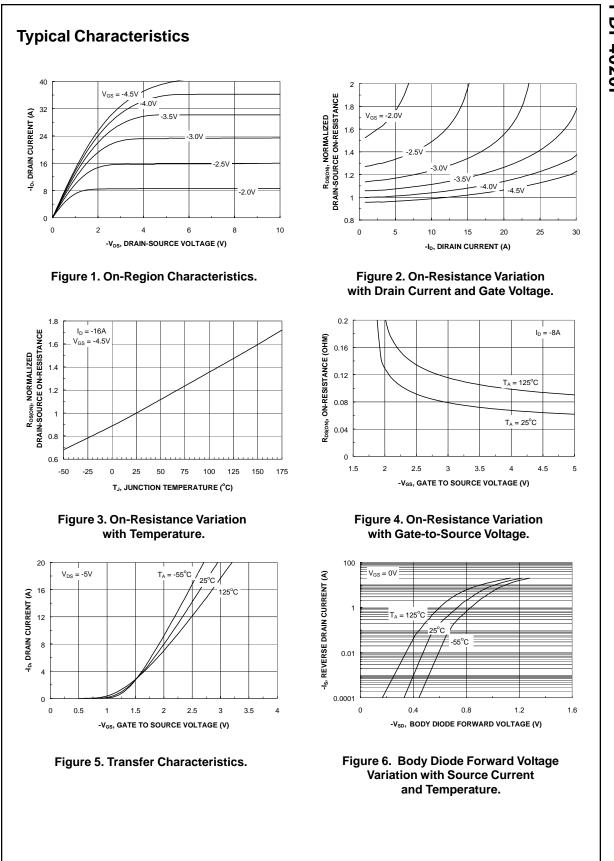
Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		FDP4020P	FDB40201	P Units	
V _{DSS}	Drain-Source Voltage		-20		V	
V _{GSS}	Gate-Source Voltage		±8		V	
I _D	Drain Current - Continuous		-16		A	
		- Pulsed		-4	8	
P _D	Total Power Dissipation @ T _c = 25°C Derate above 25°C		37.5		W	
			0.25		W/∘C	
T _J , T _{STG}	Operating and Storage Junction Temperature Range		-65 to +175		۰C	
Therma	I Character	istics				
R _θ JC	Thermal Resistance, Junction-to- Case		4		∘C/W	
R _{AJA}	Thermal Resistance, Junction-to- Ambient (Note 1)		62.5	40	∘C/W	
		,	· · ·			
Packag	e Outlines	and Ordering Inf	ormation			
Dovice	Marking	Device	Rool Sizo	Tane Wi	dth	Quantity

Device Marking	Device	Reel Size	Tape Width	Quantity
FDP4020P	FDP4020P	13"	12mm	2500 units

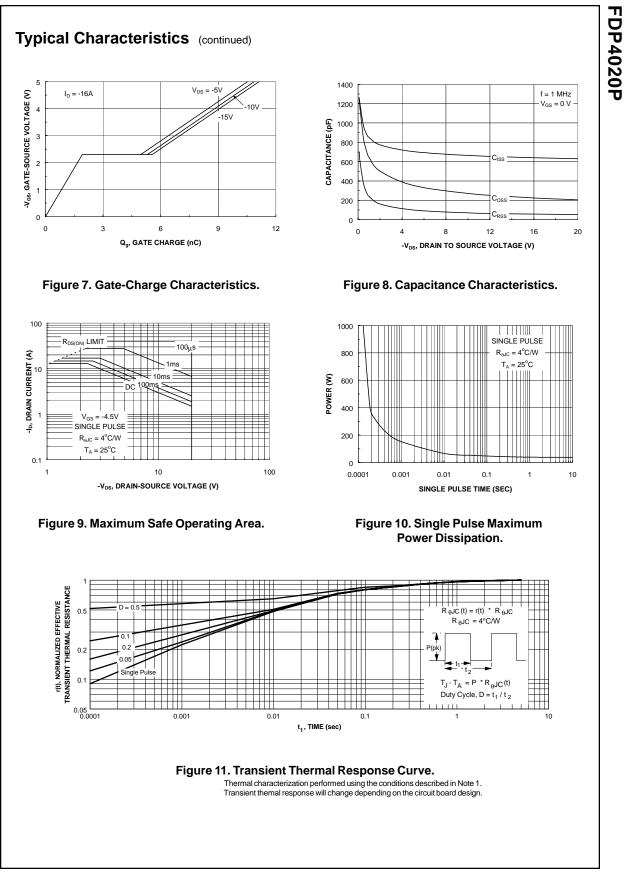
FDP4020P

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics					
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = -250 \mu\text{A}$	-20			V
<u>A</u> BVdss ATJ	Breakdown Voltage Temperature Coefficient	$I_D = -250 \ \mu$ A, Referenced to 25°C		-28		mV/∘C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			-1	μA
I _{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 8 \text{ V}, V_{DS} = 0 \text{ V}$			100	nA
	Gate-Body Leakage Current, Reverse	$V_{GS} = -8 \ V, \ V_{DS} = 0 \ V$			-100	nA
On Chara	acteristics (Note 2)					
V _{GS(th)}	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}, \ I_{\text{D}} = -250 \ \mu\text{A}$	-0.4	-0.58	-1	V
<u>AVGS(th)</u> ΔTJ	Gate Threshold Voltage Temperature Coefficient	$I_D = -250 \ \mu\text{A}$, Referenced to 25°C		2		mV/∘C
R _{DS(on)}	Static Drain-Source On-Resistance	$ \begin{array}{l} V_{GS}=-4.5 \ V, I_{D}=-8 \ A, \\ V_{GS}=-4.5 \ V, I_{D}=-8 \ A, T_{J}{=}125^{\circ}C \\ V_{GS}=-2.5 \ V, I_{D}=-7 \ A \end{array} $		0.068 0.098 0.096	0.08 0.13 0.110	Ω
I _{D(on)}	On-State Drain Current	$V_{GS} = -4.5 \text{ V}, \text{ V}_{DS} = -5 \text{ V}$	-20			Α
g _{FS}	Forward Transconductance	$V_{DS} = -5 V, I_{D} = -8 A$		14		S
D	Ok ana stanistica					
<u>Dynamic</u> C _{iss}	Characteristics	$V_{DS} = -10 \text{ V}, \text{ V}_{GS} = 0 \text{ V},$		665		pF
C _{oss}	Output Capacitance	f = 1.0 MHz		270		pF
C _{rss}	Reverse Transfer Capacitance			70		pF
	g Characteristics (Note 2)				L	
t _{d(on)}	Turn-On Delay Time	$V_{DD} = -5 V, I_D = -1 A,$		8	16	ns
t _r	Turn-On Rise Time	V_{GS} = -4.5 V, R_{GEN} = 6 Ω		24	38	ns
t _{d(off)}	Turn-Off Delay Time			50	80	ns
t _f	Turn-Off Fall Time			29	45	ns
Qg	Total Gate Charge	V _{DS} = -5 V,		9.5	13	nC
Q _{gs}	Gate-Source Charge	$I_{D} = -16 \text{ A}, \text{ V}_{GS} = -4.5 \text{ V}$		1.3		nC
Q _{gd}	Gate-Drain Charge			2.2		nC
Drain-So	urce Diode Characteristics	and Maximum Ratings				
l _s	Maximum Continuous Drain-Sour				-16	Α
I _{SM}	Maximum Pulsed Drain-Source D	iode Forward Current (Note 2)			-48	
	Drain-Source Diode Forward	$V_{GS} = 0 V, I_S = -16 A$ (Note 2)			-1.2	V





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