

FAN7085_F085

High Side Gate Driver with Recharge FET

Features

- Qualified to AEC Q100
- Floating channel designed for bootstrap operation fully operational up to 300V.
- Tolerance to negative transient voltage on VS pin
- dv/dt immune.
- Gate drive supply range from 4.5V to 20V
- Under-voltage lockout
- CMOS Schmitt-triggered inputs with pull-down and pull-up
- High side output out of phase with input (Inverted input)
- Reset input
- Internal recharge FET for bootstrap refresh

Typical Applications

- Diesel and gasoline injectors/valves
- MOSFET and IGBT high side driver applications

Description

The FAN7085_F085 is a high-side gate drive IC with reset input and built-in recharge FET. It is designed for high voltage and high speed driving of MOSFET or IGBT, which operates up to 300V. Fairchild's high-voltage process and common-mode noise cancellation technique provide stable operation in the high side driver under high-dV/dt noise circumstances. Logic input is compatible with standard CMOS outputs. The UVLO circuits prevent from malfunction when VCC and VBS are lower than the specified threshold voltage. It is available with space saving SOIC-8 Package. Minimum source and sink current capability of output driver is 250mA and 250mA. Built-in recharge FET to refresh bootstrap circuit is very useful for circuit topology requiring switches on low and high side of load.

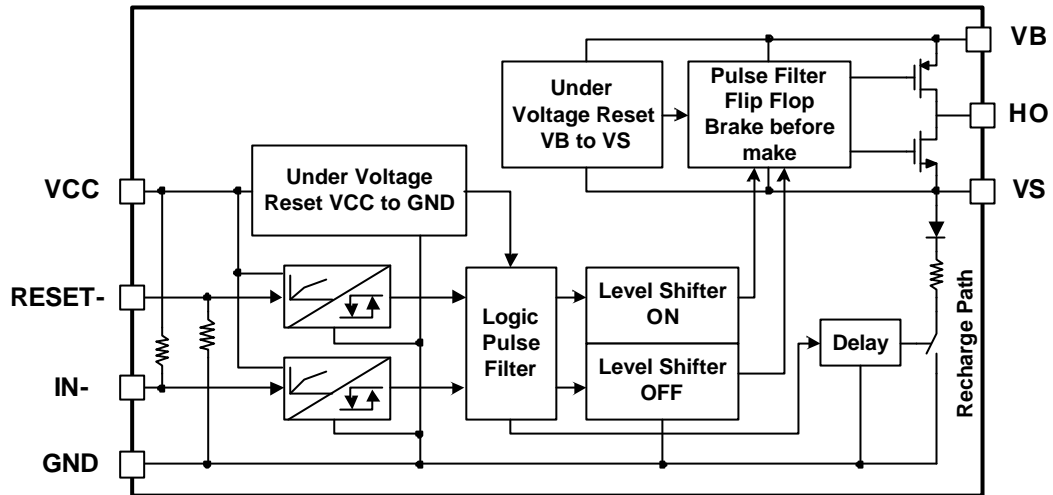


Ordering Information

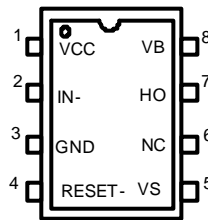
| Device | Package | Operating Temp. |
|------------|---------|-----------------|
| FAN7085CM | SOIC-8 | -40 °C ~ 125 °C |
| FAN7085CMX | SOIC-8 | -40 °C ~ 125 °C |

X : Tape & Reel type

Block Diagrams



Pin Assignments



Pin Definitions

| Pine Number | Pin Name | I/O | Pin Function Description |
|-------------|----------|-----|--|
| 1 | VCC | P | Driver supply voltage, typically 5V |
| 2 | IN- | I | Driver control signal input (Negative Logic) |
| 3 | GND | P | Ground |
| 4 | RESET- | I | Driver enable input signal (Negative Logic) |
| 5 | VS | P | High side floating offset for MOSFET Source connection |
| 6 | NC | - | No connection (No Bond wire) |
| 7 | HO | A | High side drive output for MOSFET Gate connection |
| 8 | VB | P | Driver output stage supply |

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND.

| Parameter | Symbol | Min. | Max. | Unit |
|--|-------------------|---------------------|----------------------|------|
| High side floating supply voltage | V _{BS} | -0.3 | 25 | V |
| High side driver output stage voltage Neg. transient: 0.5 ms, external MOSFET off | V _B | -5 | 325 | V |
| High side floating supply offset voltage Neg. transient 0.2 us | V _S | -25 | 300 | V |
| High side floating output voltage | V _{HO} | V _S -0.3 | V _B +0.3 | V |
| Supply voltage | V _{CC} | -0.3 | 25 | V |
| Input voltage for IN- | V _{IN} | -0.3 | V _{CC} +0.3 | V |
| Input voltage for RESET- | V _{RES} | -0.3 | V _{CC} +0.3 | V |
| Power Dissipation ¹⁾ | P _d | | 0.625 | W |
| Thermal resistance, junction to ambient ¹⁾ | R _{thja} | | 200 | °C/W |
| Electrostatic discharge voltage (Human Body Model) | V _{ESD} | 1.5K | | V |
| Charge device model | V _{CDM} | 500 | | V |
| Junction Temperature | T _j | | 150 | °C |
| Storage Temperature | T _S | -55 | 150 | °C |

Note: 1) The thermal resistance and power dissipation rating are measured below conditions;

JESD51-2: Integrated Circuit Thermal Test Method Environmental Conditions - Natural condition(StillAir)

JESD51-3: Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Package

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. -40°C ≤ T_a ≤ 125°C

| Parameter | Symbol | Min. | Max. | Unit |
|---|-----------------------------------|---------------------|--------------------|------|
| High side floating supply voltage(DC) Transient: -10V @ 0.2 us | V _B | V _S +4.5 | V _S +20 | V |
| High side floating supply offset voltage(DC) @ V _{BS} =7V | V _S | -3 | 300 | V |
| High side floating supply offset voltage(Transient) 0.2us @ V _{BS} <25V | V _S | -25 | 300 | V |
| High side floating output voltage | V _{HO} | V _S | V _B | V |
| Allowable offset voltage Slew Rate ¹⁾ | dV/dt | - | 50 | V/ns |
| Supply voltage for logic part | V _{CC} | 4.5 | 20 | V |
| Input voltage for IN- | V _{IN} | 0 | V _{CC} | V |
| Input voltage for RESET- | V _{RESET} | 0 | V _{CC} | V |
| Switching frequency ²⁾ | F _S | | 200K | Hz |
| Minimum low input width ³⁾ | t _{IN(Low,min)} | 1000 | - | ns |
| Minimum high input width ³⁾ | t _{IN(High,min)} | 60 | - | ns |
| Minimum operating voltage of V _B related to GND | V _{B(MIN)} ⁴⁾ | 4 | - | V |
| Ambient temperature | T _a | -40 | 125 | °C |

Note: 1) Guaranteed by design.

2) Duty = 0.5, V_{BS} ≥ 7V

3) Guaranteed by design. Pulse widths below the specified values, may be ignored. Output will either follow the input signal or will ignore it.

No false output state is guaranteed when minimum input width is smaller than t_{in}

4) Guaranteed by design

Statics Electrical Characteristics

Unless otherwise specified, $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$, $V_{CC} = 5\text{V}$, $V_{BS} = 7\text{V}$, $V_S = 0\text{V}$, $V_{RESET} = 5\text{V}$, $R_L = 50\Omega$, $C_L = 2.5\text{nF}$.

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|------------------|--|------------|------|----------|------------|
| VCC and VBS Supply Characteristics | | | | | | |
| VCC and VBS supply under voltage positive going threshold | VCCUV+ VBSUV+ | VCC and VBS rising from 0V | - | 3.7 | 4.3 | V |
| VCC and VBS supply under voltage negative going threshold | VCCUV- VBSUV- | VCC and VBS dropping from 5V | 2.8 | 3.4 | - | V |
| VCC and VBS under voltage hysteresis | VCCUVH VBSUVH | - | 0.02 | 0.3 | - | V |
| Under voltage lockout response time | tduvcc tduvbs | VCC: 6.5V->2.4V or 2.4V->6.5V VBS: 6.5V->2.4V or 2.4V->6.5V | 0.5 0.5 | | 20 20 | us us |
| Offset supply leakage current | ILK | VB=VS=300V | - | - | 200 | uA |
| Quiescent Vcc supply current | Iqcc | Vcc=20V | - | - | 500 | uA |
| Quiescent VBS supply current | IqBS1 | Static mode, VBS=7V, VIN=0 or 5V | | | 100 | uA |
| Quiescent VBS supply current | IqBS2 | Static mode, VBS=16V, VIN=0 or 5V | | | 200 | uA |
| VBS drop due to output turn-on (Design guaranty) | ΔV_{BS} | VBS=7V, Cbs=1uF, tdiG-IN=3uS, tTEST=100uS | | | 210 | mV |
| Input Characteristics | | | | | | |
| High logic level input voltage for IN- | VIH | | 0.6Vcc | - | - | V |
| Low logic level input voltage for IN- | VIL | | - | - | 0.28Vcc | V |
| Low logic level input bias current for IN- | IIN- | VIN=0 | 5 | 25 | 60 | uA |
| High logic level input bias current for IN- | IIN+ | VIN=5V | - | - | 5 | uA |
| Full up resistance at IN | RIN | | 83 | 200 | 1000 | K Ω |
| High logic level input voltage for RESET- | VRH | | 0.6Vcc | - | - | V |
| Low logic level input voltage for RESET- | VRL | | | | 0.28Vcc | V |
| High logic level input current for RESET- | IRRES+ | VRESET=5V | 5 | 25 | 60 | uA |
| Low logic level input bias current for RESET- | IRRES- | VRESET=0 | | | 5 | uA |
| Full down resistance at RESET- | RRES | | 83 | 200 | 1000 | K Ω |
| Output characteristics | | | | | | |
| High level output voltage, VB - VHO | VOH | Io=0 | - | - | 0.1 | V |
| Low level output voltage, VHO-GND | VOL | Io=0 | - | - | 0.1 | V |
| Peak output source current | Io+ | VIN=5V | 250 | 450 | - | mA |
| Peak output sink current | Io- | VIN=0 | 250 | 450 | - | mA |
| Equivalent output resistance | ROP | | | 15.5 | 28 | Ω |
| | RON | | | 15.5 | 28 | Ω |
| Recharge Characteristics | | | | | | |
| Recharge TR turn-on propagation delay | Ton_rech | | 4 | 7.9 | 9.8 | us |
| Recharge TR turn-off propagation delay | Toff_rech | | | 0.2 | 0.4 | us |
| Recharge TR on-state voltage drop | VRECH | Is=1mA, VIN=5V @125°C | | | 1.2 | V |
| Dead Time Characteristics | | | | | | |
| High side turn-off to recharge gate turn-on | DTHOFF | VCC=5V, VS=7V | 4 | 7.8 | 9.8 | us |
| Recharge gate turn-off to high side turn-on | DTHON | VCC=5V, VS=7V | 0.1 | 0.4 | 0.7 | us |

Note: The input parameter are referenced to GND. The VO and IO parameters are referenced to GND.

Dynamic Electrical Characteristics

Unless otherwise specified, $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$, $V_{CC} = 5\text{V}$, $V_{BS} = 7\text{V}$, $V_S = 0\text{V}$, $V_{RESET} = 5\text{V}$, $R_L = 50\Omega$, $C_L = 2.5\text{nF}$.

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|--|----------------|---|------|------|------|------|
| Input-to-output turn-on propagation delay | t_{plh} | 50% input level to 10% output level, $V_S = 0\text{V}$ | | 0.56 | 1 | us |
| Input-to-output turn-off propagation delay | t_{phl} | 50% input level to 90% output level $V_S = 0\text{V}$ | - | 0.15 | 0.5 | us |
| RESET-to-output turn-off propagation delay | t_{ph_res} | 50% input level to 90% output level | - | 0.17 | 0.5 | us |
| RESET-to-output turn-on propagation delay | t_{plh_res} | 50% input level to 10% output level | - | 0.56 | 1 | us |
| Output rising time | t_{r1} | $T_j = 25^{\circ}\text{C}$ | - | 65 | 200 | ns |
| | t_{r2} | | | - | 400 | ns |
| | t_{r3} | $T_j = 25^{\circ}\text{C}, V_{BS} = 16\text{V}$ | | 65 | 200 | ns |
| | t_{r4} | $V_{BS} = 16\text{V}$ | | - | 400 | ns |
| Output falling time | t_{f1} | $T_j = 25^{\circ}\text{C}$ | - | 25 | 200 | ns |
| | t_{f2} | | | - | 300 | ns |
| | t_{f3} | $T_j = 25^{\circ}\text{C}, V_{BS} = 16\text{V}$ | | 25 | 200 | ns |
| | t_{f4} | $V_{BS} = 16\text{V}$ | | - | 300 | ns |

Application Information

1. Logic Tables

| VCC | VBS | RESET- | IN- | Ho | RechFET |
|------------|------------|--------|------|-----|---------|
| < VCCUVLO- | X | X | X | OFF | ON |
| X | X | LOW | X | OFF | ON |
| X | X | X | HIGH | OFF | ON |
| > VCCUVLO+ | > VBSUVLO+ | HIGH | LOW | ON | OFF |
| > VCCUVLO+ | < VBSUVLO- | HIGH | LOW | OFF | OFF |

Notes:

X means independent from signal

IN=LOW indicates that the high side NMOS is ON

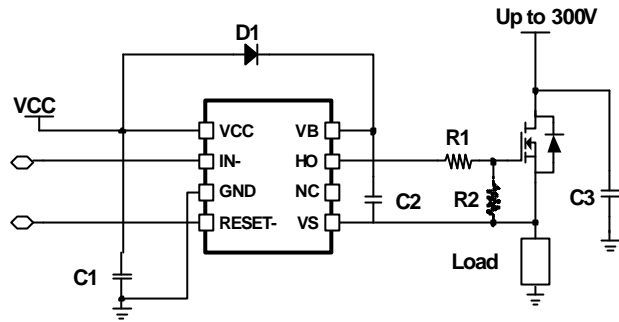
IN=HIGH indicates that the high side NMOS is OFF

RechFET =ON indicates that the recharge MOSFET is ON

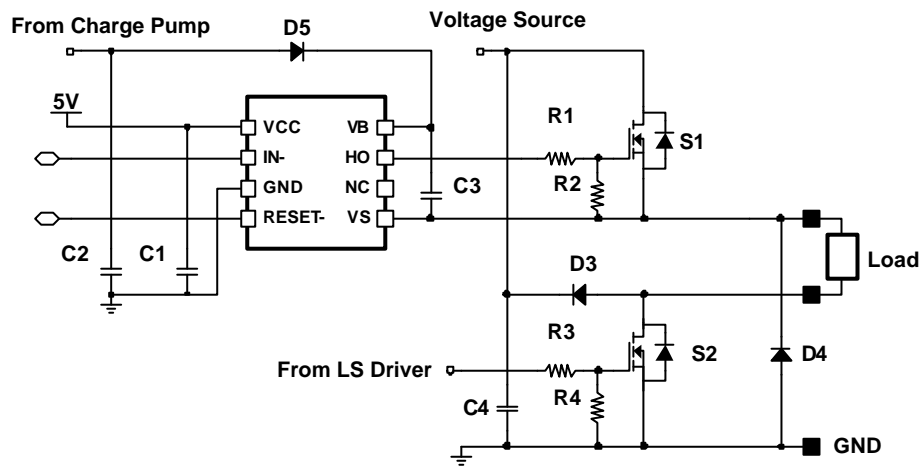
RechFET =OFF indicates that the recharge MOSFET is OFF

Typical Application Circuit

1. Typical Application Circuit



2. Application Example



Input-Output Waveforms

1. Input/Output Timing Diagrams

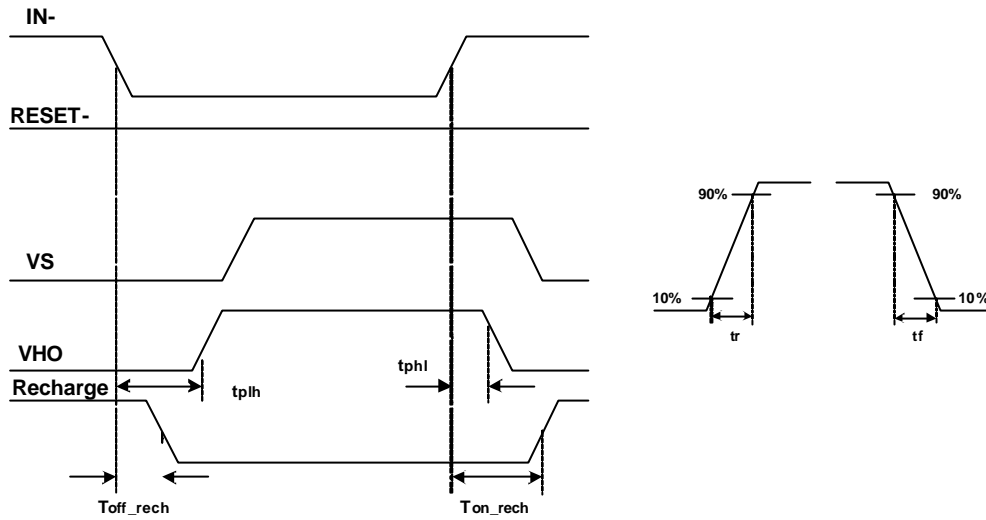


Figure.1 Input and Output Timing Diagram and Switching Time Waveform Definition

2. Reset Timing Diagrams

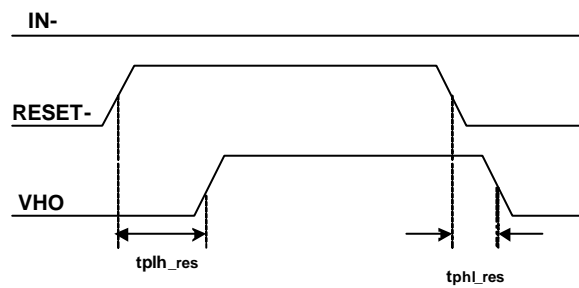


Figure.2 Reset and Output Timing Diagram

3.VB Drop Voltage Diagram

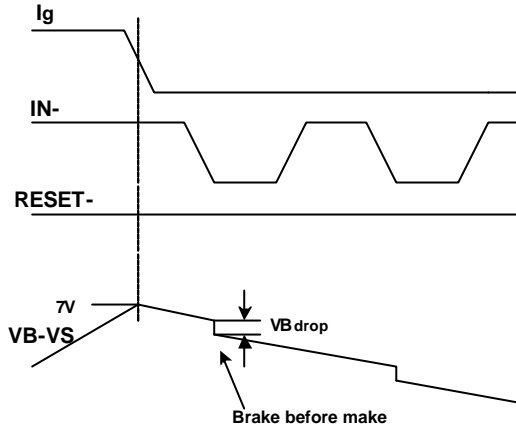


Figure3.a VB Drop Voltage Diagram

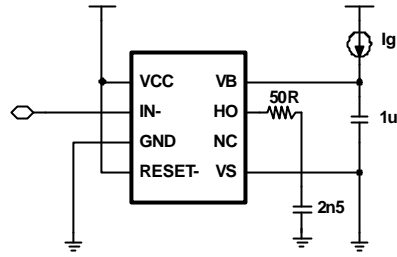


Figure3.b VB Drop Voltage Test Circuit

Performance Graphs

This performance graphs based on ambient temperature $-40^{\circ}\text{C} - 125^{\circ}\text{C}$

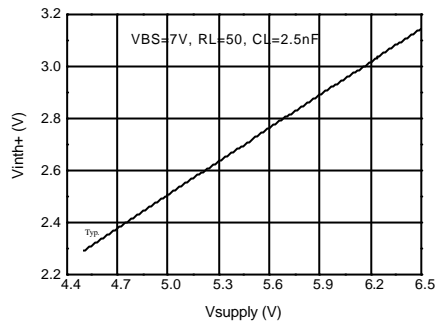


Figure 4a. Positive IN and RESET Threshold vs VCC Supply

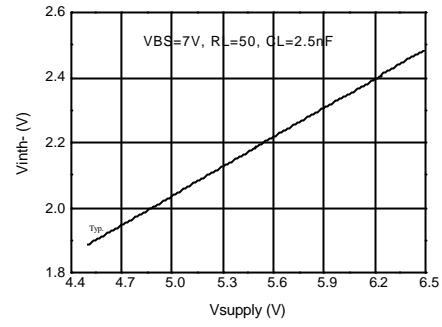


Figure 4b. Negative IN and RESET Threshold vs VCC Supply

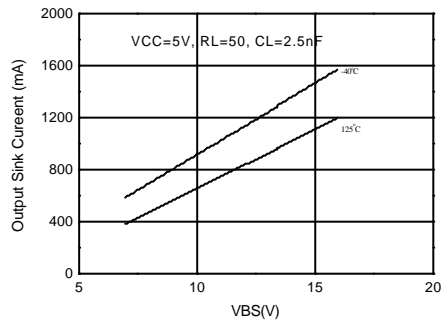


Figure 5a. Output Sink Current vs VBS Supply

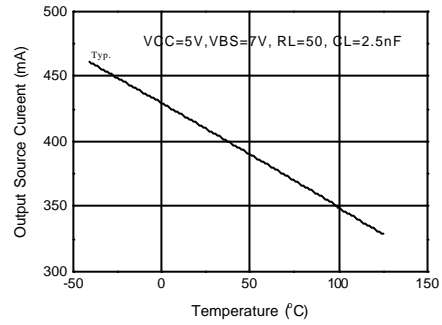


Figure 5b. Output Source Current vs Temperature

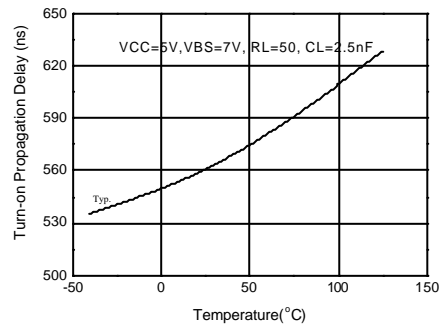


Figure 6a. Turn-On Propagation Delay Time vs Temperature

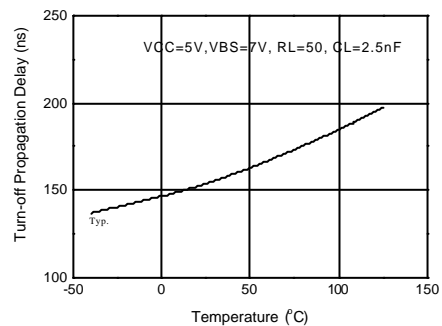


Figure 6b. Turn-Off Propagation Delay Time vs Temperature

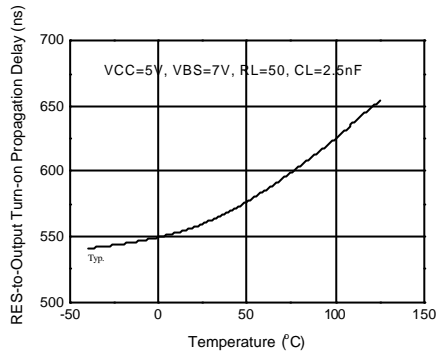


Figure 7a. RES to Output Turn-On Propagation Delay vs Temperature

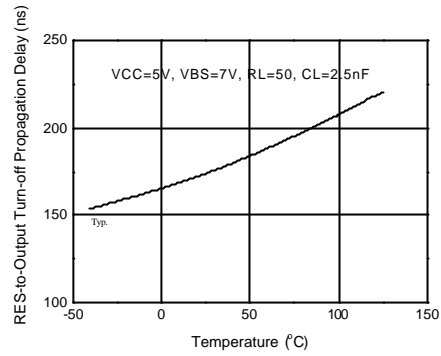


Figure 7b. RES to Output Turn-Off Propagation Delay vs Temperature

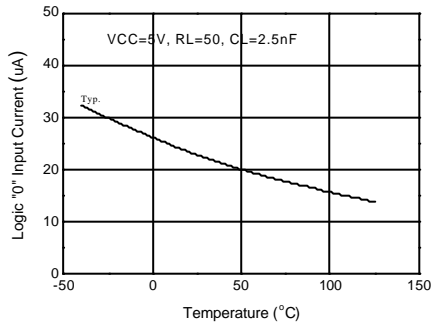


Figure 8. Logic "0" IN Input Current vs Temperature

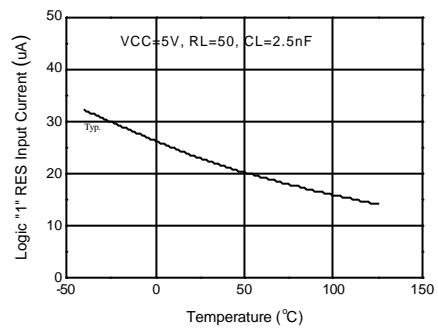


Figure 9. Logic "1" RESET Input Current vs Temperature

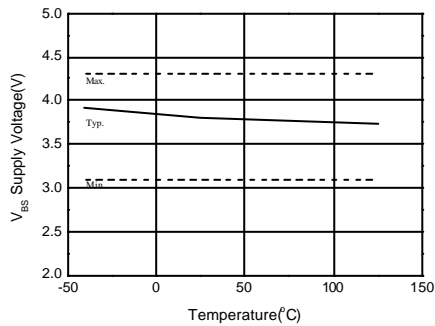


Figure 10a. VBS Under Voltage Threshold(+) vs Temperature

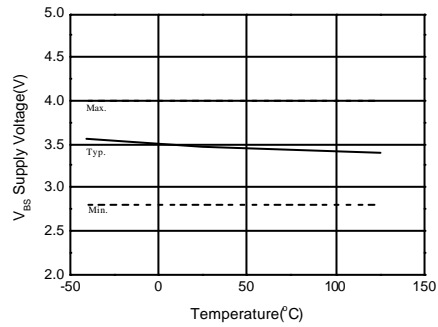


Figure 10b. VBS Under Voltage Threshold(-) vs Temperature

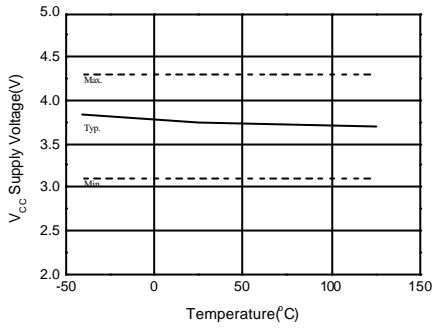


Figure 11a. VCC Under Voltage Threshold(+) vs Temperature

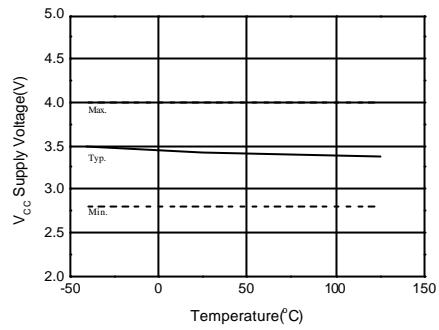


Figure 11b. VCC Under Voltage Threshold(-) vs Temperature

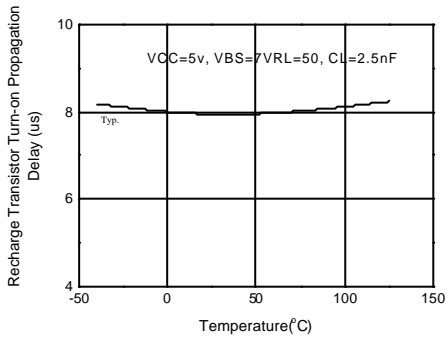


Figure 12. Recharge FET Turn-on Delay time

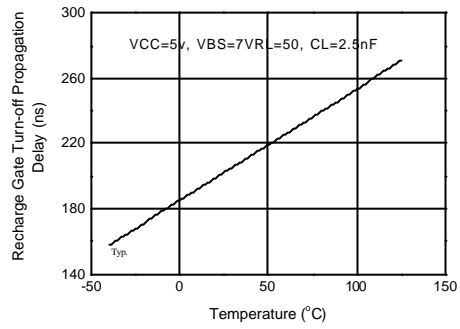


Figure 12. Recharge FET Turn-off Delay time

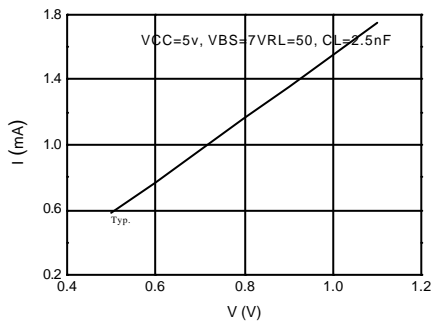


Figure 14. Recharge FET I-V curve

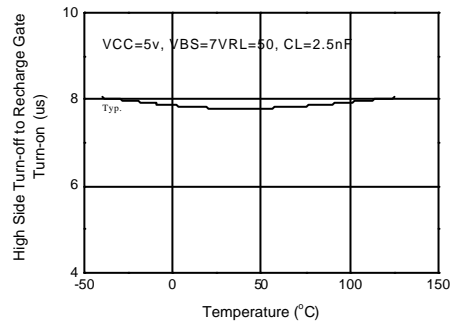
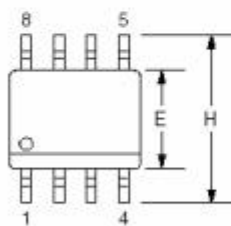


Figure 15. High Side Turn-off to Recharge FET turn-on VS Temperature

Package Dimensions

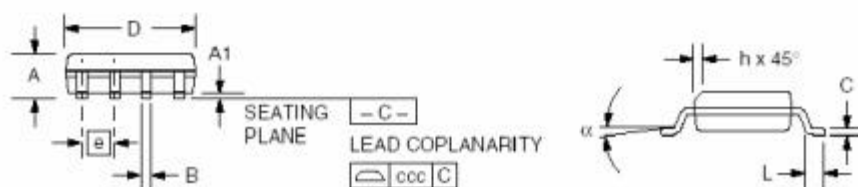
8-SOP

| Symbol | Inches | | Millimeters | | Notes |
|----------|----------|------|-------------|------|-------|
| | Min. | Max. | Min. | Max. | |
| A | .053 | .069 | 1.35 | 1.75 | |
| A1 | .004 | .010 | 0.10 | 0.25 | |
| B | .013 | .020 | 0.33 | 0.51 | |
| C | .0075 | .010 | 0.20 | 0.25 | 5 |
| D | .189 | .197 | 4.80 | 5.00 | 2 |
| E | .150 | .158 | 3.81 | 4.01 | 2 |
| e | .050 BSC | | 1.27 BSC | | |
| H | .228 | .244 | 5.79 | 6.20 | |
| h | .010 | .020 | 0.25 | 0.50 | |
| L | .016 | .050 | 0.40 | 1.27 | 3 |
| N | 8 | | 8 | | 6 |
| α | 0° | 8° | 0° | 8° | |
| ccc | — | .004 | — | 0.10 | |



Notes:


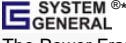
1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.





TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- | | | | |
|--|---|--|---|
| Build it Now™ | FRFET® | Programmable Active Droop™ | the power franchise™ |
| CorePLUS™ | Global Power Resource SM | QFET® | TinyBoost™ |
| CorePOWER™ | Green FPS™ | QS™ | TinyBuck™ |
| CROSSVOLT™ | Green FPS™ e-Series™ | Quiet Series™ | TinyLogic® |
| CTL™ | GTO™ | RapidConfigure™ | TINYOPTO™ |
| Current Transfer Logic™ | IntelliMAX™ |  ™ | TinyPower™ |
| EcoSPARK® | ISOPLANAR™ | Saving our world, 1mW/W/kW at a time™ | TinyPWM™ |
| EfficientMax™ | MegaBuck™ | SmartMax™ | TinyWire™ |
| EZSWITCH™* | MICROCOUPLER™ | SMART START™ | TriFault Detect™ |
|  ™* | MicroFET™ | SPM® | TRUECURRENT™* |
|  ® | MicroPak™ | STEALTH™ | µSerDes™ |
| Fairchild® | MillerDrive™ | SuperFET™ |  ™ |
| Fairchild Semiconductor® | MotionMax™ | SuperSOT™-3 | UHC® |
| FACT Quiet Series™ | Motion-SPM™ | SuperSOT™-6 | Ultra FRFET™ |
| FACT® | OPTOLOGIC® | SuperSOT™-8 | UniFET™ |
| FAST® | OPTOPLANAR® | SupreMOS™ | VCX™ |
| FastvCore™ |  ® | SyncFET™ | VisualMax™ |
| FlashWriter®* | PDP SPM™ |  ®* | XS™ |
| FPS™ | Power-SPM™ | The Power Franchise® | |
| F-PFS™ | PowerTrench® | | |
| | PowerXS™ | | |

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

| Datasheet Identification | Product Status | Definition |
|--------------------------|-----------------------|---|
| Advance Information | Formative / In Design | Datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
| No Identification Needed | Full Production | Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design. |
| Obsolete | Not In Production | Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only. |