FAN5250

Mobile Processor Core-Voltage Regulator

Features

- High efficiency over wide load range
- Non dissipative current-sense; uses MOSFET $R_{DS(ON)}$ or can use optional Current-Sense resistor for greater precision
- Overcurrent protection
- Powerful drivers for N-Channel MOSFETs with adaptive dead time
- Precision core voltage control
- Remote “Kelvin” sensing
- Summing current-mode control with programmable Active Droop for Optimum Transient Response and Lower Processor Power Dissipation
- 5-Bit Digital Output Voltage Selection
- Wide Range output voltage: 0.6 VDC to 1.0 VDC in 25mV Steps, and from 1.0 VDC to 1.75 VDC in 50mV Steps
- “On-the-Fly” VID code change with programmable slew rate
- Alternative input to set output voltage during start-up or power saving modes
- Forced continuous conduction mode of operation
- Output voltage (Power-Good) monitor
- No negative core voltage on turn-off
- Over-Voltage, Under-Voltage and Over-Current fault monitors
- Selectable 300/600kHz Switching Frequency

Applications

- Transmeta’s Crusoe™ CPU core power
- Intel P3-M™ processor (IMVP-2)

Description

The FAN5250 is a single output power controller to power mobile CPU cores. The FAN5250 includes a 5-bit digital-to-analog converter (DAC) that adjusts the core PWM output voltage from 0.6VDC to 1.75VDC, and may be changed during operation. Special measures are taken to allow the output to transition with controlled slew rate to comply with Transmeta’s LongRun™ and Intel’s P3-M Speed-Step™ requirements. The FAN5250 includes a precision reference, and a proprietary architecture with integrated compensation providing excellent static and dynamic core voltage regulation.

With nominal currents, the controller operates at a selectable frequency of 300kHz or 600kHz. At light loads, when the filter inductor current becomes discontinuous, the controller operates in a hysteretic mode dramatically improving system efficiency. The hysteretic mode of operation can be inhibited by the $\overline{\text{FPWM}}$ control pin.

The FAN5250 monitors the output voltage and issues a PGOOD (Power-Good) when soft start is completed and the output is in regulation. A built-in over-voltage protection (OVP) forces the lower MOSFET on to prevent output voltages from exceeding 1.9V. Undervoltage protection latches the chip off when the output drops below 75% of the set value. The PWM controller's overcurrent circuitry monitors the converter load by sensing the voltage drop across the lower MOSFET. The overcurrent threshold is set by an external resistor. If precision overcurrent protection is required, an optional external current-sense resistor may be used.

Typical Application

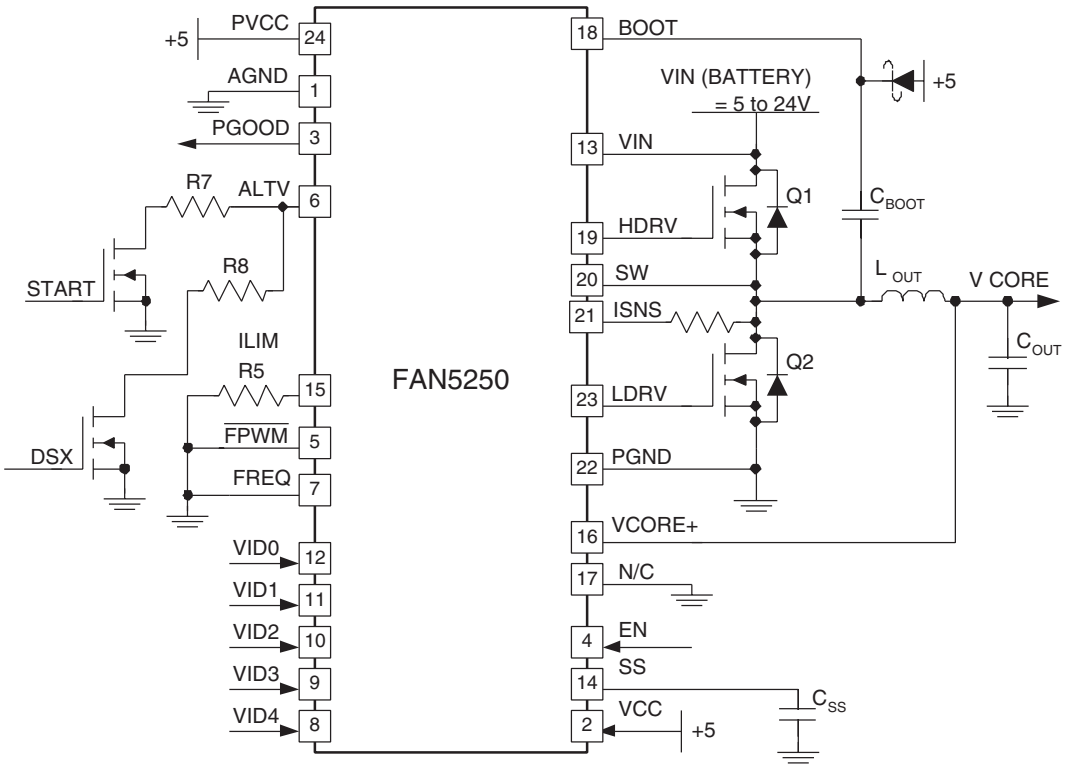
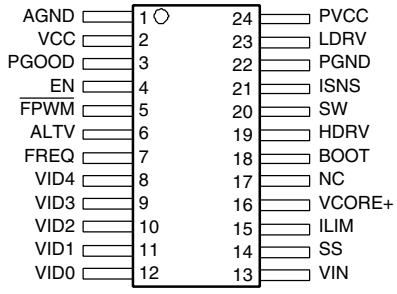


Figure 1.

Pin Assignments



QSOP-24
Θ_{JA} = 90°C

Pin Description

Pin Number	Pin Name	Pin Function Description
1	AGND	**Analog Ground**. This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin.
2	VCC	**VCC.** This pin powers the chip. The IC starts to operate when voltage on this pin exceeds 4.6V (UVLO rising) and shuts down when it drops below 4.3V (UVLO falling).
3	PGOOD	**Power Good Flag.** An open-drain output that will pull LOW when the core output is outside of a +25% –10% range of the VID reference voltage The PGOOD pin is kept high during transitions between VID settings, Deep Sleep, and Reserved Mode transitions.
4	EN	**ENABLE.** This pin enables IC operation when either left open, or pulled up to VCC. Toggling EN will also reset the chip after a latched fault condition.
5	$\overline{\text{FPWM}}$	**Forced PWM mode.** When logic low, inhibits the chip from entering hysteretic operating mode.
6	ALTV	**Alternative to VID.** The IC will regulate to the voltage on this pin if it is below the highest VID voltage (1.75V). Such a requirement may occur during CPU initialization or during some power saving modes. This pin has a 10µA current source, so that its voltage can be programmed with a resistor to GND. See Alternative Voltage Programming on page 8 for details.
7	FREQ	**Frequency Set.** Logic Low sets the operating frequency to 300Khz. High sets the frequency to 600Khz.
8–12	VID0–4	**Voltage Identification Code**. Input to VID DAC. Sets the output voltage according to the codes set as defined in Table 1.
13	VIN	**Input Voltage from battery.** This voltage is used by the oscillator for feed-forward compensation of input voltage variation.
14	SS	**Soft Start.** A capacitor from this pin to GND programs the slew rate of the converter during initialization as well as in operation. This pin is used as the reference against which the output is compared. During initialization, this pin is charged with a 25µA current source. Once this pin reaches 0.5V, its function changes, and it assumes the value of the voltage as set by the VID programming. The current driving this pin is then limited to $\pm$500µA, that together with C_{SS} sets a controlled slew rate for VID code changes.
15	ILIM	**Current Limit.** A resistor from this pin to GND sets the current limit.
16	V_{CORE}+	**VCORE Output Sense.** This pin is the feedback from the VCORE output. Used for regulation as well as PGOOD, under-voltage and over-voltage protection and monitoring.
17	NC	**No internal connection.** While no connection is necessary, tying this pin to GND is recommended to reduce coupled noise into pin 16 from pin 18.
18	BOOT	**BOOT.** The positive supply for the upper MOSFET driver. Connect as shown in Figure 1.
19	HDRV	**High-Side Drive.** The high-side (upper) MOSFET driver output.
20	SW	**Switching node.** The return for the high-side MOSFET driver.
21	ISNS	**Current Sense Input.** Monitors the voltage drop across the lower MOSFET or external sense resistor for current feedback.
22	PGND	**Power Ground.** The return for the low-side MOSFET driver.
23	LDRV	**Low-Side Drive.** The low-side (lower) MOSFET driver output.
24	PVCC	**Power VCC.** The positive supply for the lower MOSFET driver.

Absolute Maximum Ratings

Absolute maximum ratings are the values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied

Parameter	Min.	Typ.	Max.	Units
VCC Supply Voltage			6.5	V
VIN			27	V
BOOT, SW, HDRV Pins			33	V
BOOT to SW			6.5	V
All Other Pins	-0.3		VCC + 0.3	V
Junction Temperature (T_J)	-10		150	°C
Storage Temperature	-65	150		°C
Lead Soldering Temperature, 10 seconds			300	°C

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage VCC		4.75	5	5.25	V
Supply Voltage VIN		5		24	V
Ambient Temperature (T_A)		–10		85	°C

Electrical Specifications

(VCC = 5V, VIN = 5V–24V, and T_A = recommended operating ambient temperature range using circuit of Figure 1, unless otherwise noted)

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Supplies					
VCC Current	Operating, C_L = 10pF		2.7	3.2	mA
	Shut-down (EN = 0)		6	30	µA
VIN Current	Operating		12	20	µA
	Shut-down (EN = 0)			1	µA
UVLO Threshold	Rising VCC	4.3	4.65	4.75	V
	Falling	4.1	4.35	4.45	V
Regulator / Control Functions					
Output Voltage	per Table 1. Output Voltage VID	0.6		1.75	V
Initial Accuracy		-1		1	% VID
Static Load Regulation		-2		2	% VID
Error Amplifier Gain			86		dB
Error Amplifier GBW			2.7		MHz
Error Amplifier Slew Rate			1		V/µS
ILIM Voltage	R_{ILIM} = 30KΩ	0.89		0.91	V
Over-voltage Threshold		1.9	1.95	2.0	V
Over-voltage Protection Delay		1.6		3.2	µS
Under-voltage Shutdown	Disabled during VID code change	72	75	78	% VID
Under-voltage Delay		1.2		1.6	µS
EN, input threshold	Logic LOW			1.2	V
	Logic HIGH	2			V
Output Drivers					
HDRV Output Resistance	Sourcing		3.8	5	Ω
	Sinking		1.6	3	Ω
LDRV Output Resistance	Sourcing		3.8	5	Ω
	Sinking		0.8	1.5	Ω
Oscillator					
Frequency	FREQ = HIGH	255	300	345	KHz
	FREQ = LOW	510	600	690	KHz
Ramp Amplitude, pk-pk	VIN = 16V		2		V
Ramp Offset			0.5		V
Ramp Gain	$\frac{\text{Ramp amplitude}}{\text{VIN}}$			125	mV/V
Reference, DAC and Soft-Start					
VID input threshold	Logic LOW			1.21	V
	Logic HIGH	1.62			V
VID pull-up current	to internal 2.5V reference		12		µA
DAC output accuracy		-1		1	%

Electrical Specifications (continued)

(VCC = 5V, VIN = 5V–24V, and T_A = recommended operating ambient temperature range using circuit of Figure 1, unless otherwise noted)

Parameter	Conditions	Min.	Typ.	Max.	Units
Soft Start current (I_{SS})	at start-up, V_{SS} < 0.5	20	26	32	µA
	at start-up, 1.75 > V_{SS} > 0.5	350	500	650	µA
ALTV Current Source		9.5	10	10.5	µA
ALTV to VID mode threshold		1.71	1.75	1.78	V
PGOOD					
VCORE Upper Threshold		123		127	% VID
VCORE Lower Threshold	Falling Edge	77		81	% VID
	Rising Edge	87		94	% VID
PGOOD Output Low	IPGOOD = 4mA		0.5		V
Leakage Current	V_{PULLUP} = 5V			1	µA

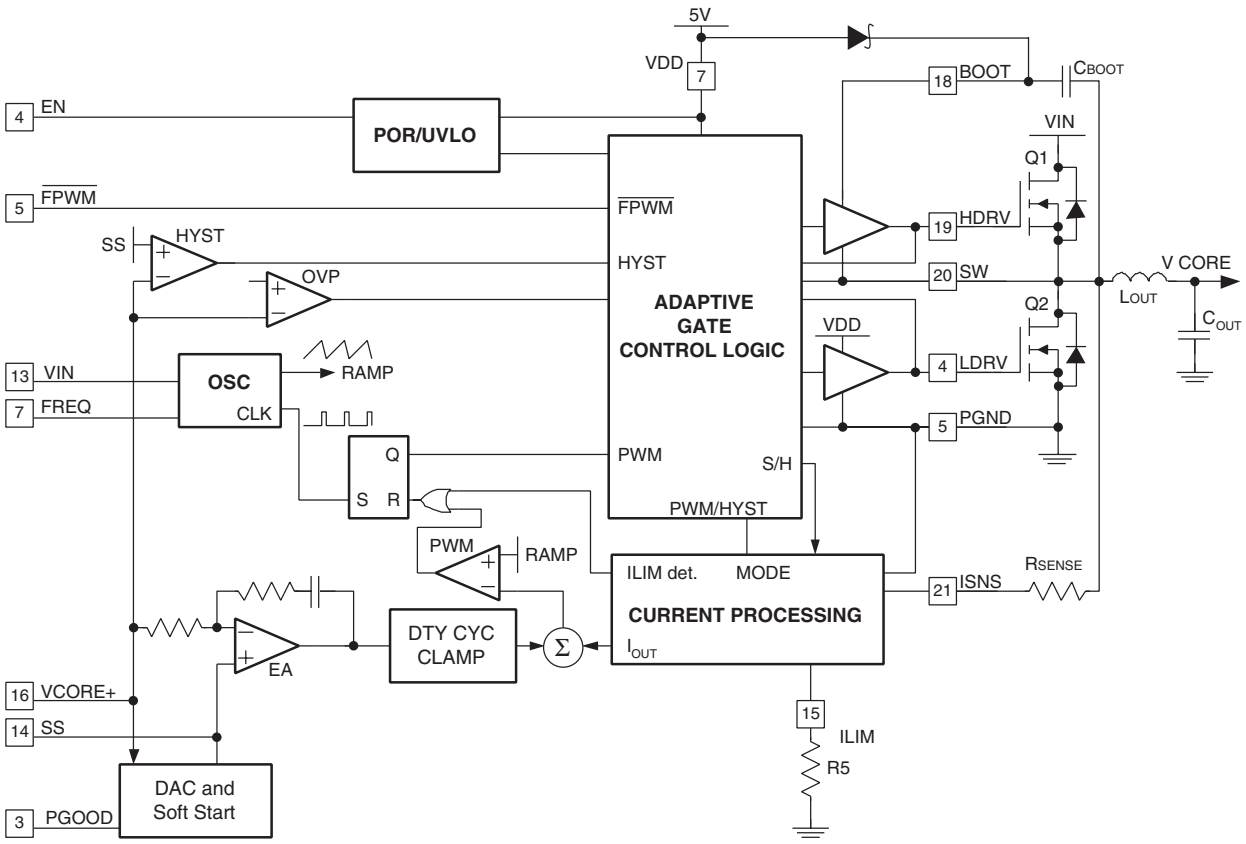


Figure 2. IC Block Diagram

Circuit Description

Overview

The FAN5250 is a single output power management IC supplies the low-voltage, high-current power to modern processors for notebook and sub-notebook PCs. Using very few external components, the IC controls a precision programmable synchronous buck converter driving external N-Channel power MOSFETs. The output voltage is adjustable from 0.6V to 1.75V by changing the DAC code settings (see Table 1). Alternatively, the output voltage can be set by an analog input. This feature is important in systems where VID code may not be established during start-up or CPU core power saving modes. The output voltage of the core converter can be changed on-the-fly with programmable slew rate, which meets a key requirement of the processor.

The converter can operate in two modes: fixed frequency PWM, and variable frequency hysteretic depending on the load. At loads lower than the point where filter inductor current becomes discontinuous, hysteretic mode of operation is activated. Switchover from PWM to hysteretic operation at light loads improves the converter's efficiency and prolongs battery run time. As the filter inductor resumes continuous current, the PWM mode of operation is restored. The chip can be prevented from entering hysteretic mode by driving the FPWM pin low.

The core converter incorporates a proprietary output voltage droop method for optimum handling of fast load transients found in modern processors.

Initialization and Soft Start

Assuming EN is high, FAN5250 is initialized when power is applied on VCC. Should VCC drop below the UVLO threshold, an internal Power-On Reset function disables the chip.

The IC attempts to regulate the VCORE output according to the voltage that appears on the SS pin (V_{SS}). During start-up of the converter, this voltage is initially 0, and rises linearly to 0.5V via the current supplied to C_{SS} through the 25µA internal current source. The time it takes to reach 0.5V is:

$$T_{0.5} = \frac{0.5 \times C_{SS}}{25} \quad (1)$$

where $T_{0.5}$ is in seconds if C_{SS} is in µF.

At that point, the current source changes to 500µA, which then sets the slew rate of voltage changes at the output in response to changes in VID.

This dual slope approach helps to provide safe rise of voltages and currents in the converters during initial start-up and at the same time sets a controlled speed of the core voltage change when the processor commands to do so.

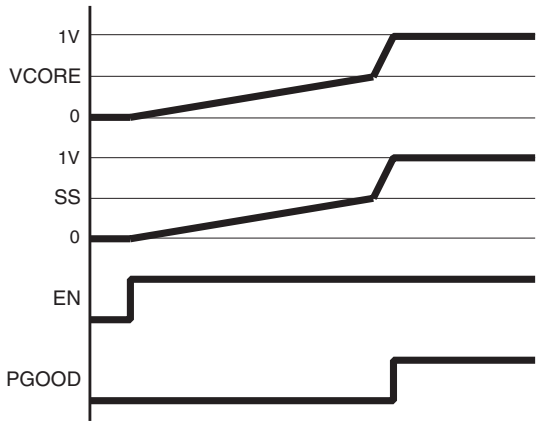


Figure 3. Soft-Start Function

C_{SS} typically is chosen based on the slew rate desired in response to a VID change. For example, if the spec requires a 50mV step to occur in 32µS:

$$C_{SS} = \frac{\Delta I_{SS}}{\Delta V_{DAC}} \Delta t = \left(\frac{500\mu A}{50mV}\right) 32\mu S \cong 0.33\mu F \quad (2)$$

With this value of C_{SS}, the time for the output voltage to rise to 0.5V if found using equation 1:

$T_{0.5} = 6.6mS$

We defined a slew rate of 50mV/32µS to choose the capacitor, therefore it takes an additional 450µS to rise from 0.5V to 1.2V.

$$T_{1.2} = T_{0.5} + T_{(0.5to1.2)} = 6.6 + 0.45 = 7mS \quad (3)$$

Converter Operation

At nominal current the converter operates in fixed frequency PWM mode. The output voltage is compared with a reference voltage set by the DAC, which appears on the SS pin. The derived error signal is amplified by an internally compensated error amplifier and applied to the inverting input of the PWM comparator. To provide output voltage droop for enhanced dynamic load regulation, a signal proportional to the output current is added to the voltage feedback signal. This feedback scheme in conjunction with a PWM ramp proportional to the input voltage allows for fast and stable loop response over a wide range of input voltage and output current variations. For the sake of efficiency and maximum simplicity, the current sense signal is derived from the voltage drop across the lower MOSFET during its conduction time.

Output Voltage Programming

The output voltage of the converter is programmed by an internal DAC in discrete steps between 0.6V and 1.75V:

Table 1. Output Voltage VID

VID4	VID3	VID2	VID1	VID0	V_{OUT} to CPU
1	1	1	1	1	0.600
1	1	1	1	0	0.625
1	1	1	0	1	0.650
1	1	1	0	0	0.675
1	1	0	1	1	0.700
1	1	0	1	0	0.725
1	1	0	0	1	0.750
1	1	0	0	0	0.775
1	0	1	1	1	0.800
1	0	1	1	0	0.825
1	0	1	0	1	0.850
1	0	1	0	0	0.875
1	0	0	1	1	0.900
1	0	0	1	0	0.925
1	0	0	0	1	0.950
1	0	0	0	0	0.975
0	1	1	1	1	1.000
0	1	1	1	0	1.050
0	1	1	0	1	1.100
0	1	1	0	0	1.150
0	1	0	1	1	1.200
0	1	0	1	0	1.250
0	1	0	0	1	1.300
0	1	0	0	0	1.350
0	0	1	1	1	1.400
0	0	1	1	0	1.450
0	0	1	0	1	1.500
0	0	1	0	0	1.550
0	0	0	1	1	1.600
0	0	0	1	0	1.650
0	0	0	0	1	1.700
0	0	0	0	0	1.750

1 = Logic High or open, 0 = Logic Low

VID0–4 pins will assume a logic 1 level if left open as each has a 12µA internal current source pull-up to 2.5V. The output of the DAC voltage also establishes the thresholds for PGOOD, UVP and OVP thresholds.

Alternative Voltage Programming Input

The output voltage can alternatively be set by the ALTV pin. This override of the VID DAC becomes necessary during power-up and some power saving modes of operation, when the voltage on the processor is insufficient to provide correct VID codes to the controller. Therefore, the required core voltage should be set by some means external to the processor. A common approach to this problem is to provide hard-wired VID codes via a multiplexer controlled by the CPU. That approach lacks simplicity and takes many external components and valuable motherboard area.

The FAN5250 uses a simpler way to set the core voltages when the CPU is incapable of providing valid VID codes. A resistor-MOSFET network (shown in Figure 4) works with the calibrated 10µA current from the ALTV pin to set the ALTV voltage when the MOSFET's gate is driven high. The controller regulates the output voltage to the level established on the ALTV pin when this voltage is lower than the highest VID programmed voltage (1.75V). When both MOSFET gates are low, the ALTV pin goes to 2.5V and the output is controlled by the VID code. If a more accurate Deep-Sleep (DSX) and Start voltages are required than the internal current source can provide, it may be overridden with the external resistor shown (grey-shading).

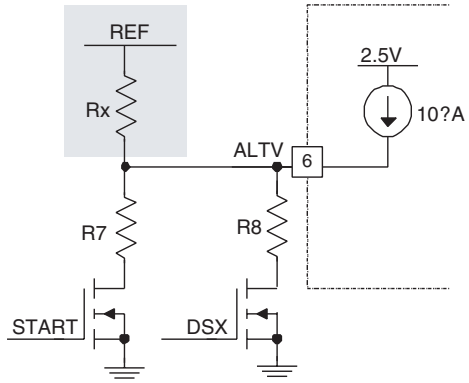


Figure 4. ALTV Programming

When relying on the internal current source to set ALTV:

$$R7 = \left(\frac{V_{START}}{10\mu A}\right) \text{ and } R8 = \left(\frac{V_{DSX}}{10\mu A}\right) \quad (4)$$

When using Rx for greater accuracy, on the internal current source to set ALTV, Choose a value for Rx where

$$\left(\frac{V_{REF} - V_{START}}{R_X}\right) \gg 10\mu A, \text{ then}$$

$$R7 = \left(\frac{V \times V_{START}}{V_{REF} - V_{START} + (R_X \times 10\mu A)}\right) \quad (5)$$

$$R8 = \left(\frac{R \times V_{START}}{V_{REF} - V_{DSX} + (R_X \times 10\mu A)}\right)$$

Operation Mode Control

The mode-control circuit changes the converter's mode of operation based on the voltage polarity of the SW node when the lower MOSFET is conducting and just before the upper MOSFET turns on. For continuous inductor current, the SW node is negative when the lower MOSFET is conducting and the converters operate in fixed-frequency PWM mode as shown in Figure 5. This mode of operation achieves high efficiency at nominal load. When the load current decreases to the point where the inductor current flows through the lower MOSFET in the 'reverse' direction, the SW node becomes positive, and the mode is changed to hysteretic, which achieves higher efficiency at low currents by decreasing the effective switching frequency.

A comparator handles the timing of the SW node voltage sensing. A low level on the SW comparator output indicates a negative SW voltage during the conduction time of the lower MOSFET. A high level on the comparator output indicates a positive SW voltage. To prevent accidental mode change and "mode chatter", the circuit must detect eight consecutive matching sign signals in a row before it changes mode. If during the monitoring process the mismatch of voltage signs occurs, no decision to mode change will occur. This same decision algorithm is used both for changing from PWM to Hysteretic mode as well as from Hysteretic to PWM mode.

PWM mode is sustained during all upward and downward transitions commanded by either VID code change, or during transitions from ALTV programmed voltage to VID code set voltage, or vice versa, as well as in Soft-Start.

The boundary value of inductor current, where current becomes discontinuous, can be estimated by the following expression.

$$I_{LOAD(DIS)} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{2\ F_{SW}\ L_{OUT}\ V_{VIN}} \qquad (6)$$

Hysteretic Mode

The mode change from hysteretic to PWM can be caused by one of two events. One event is the same mechanism that causes a PWM to hysteretic transition. But instead of looking for eight consecutive positive occurrences on the SW node it is looking for eight consecutive negative occurrences on the SW node. The operation mode will be changed from hysteretic to PWM when these eight consecutive pulses occur. This transition technique prevents jitter of the operation mode at load levels close to boundary.

The other mechanism for changing from hysteretic to PWM is due to a sudden increase in the output current. This step load causes an instantaneous decrease in the output voltage due to the voltage drop on the output capacitor ESR. If the decrease causes the output voltage to drop below the hysteretic regulation level (20mV below V_{SS}), the mode is changed to PWM on the next clock cycle. This insures the full power required by the increase in output current.

In hysteretic mode, the PWM comparator and the error amplifier that provided control in PWM mode are inhibited and the hysteretic comparator is activated. In this mode the synchronous rectifier MOSFET is controlled in diode emulation mode, where the voltage across it is monitored, and it is switched off when its voltage goes positive (current flowing back from the load) allowing the schottky diode to block reverse conduction.

The hysteretic comparator initiates a PFM signal to turn on UDRV when the output voltage falls below the lower threshold (10mV below V_{SS}) and terminates the PFM signal when the output voltage rises over the higher threshold (5mV above V_{SS}).

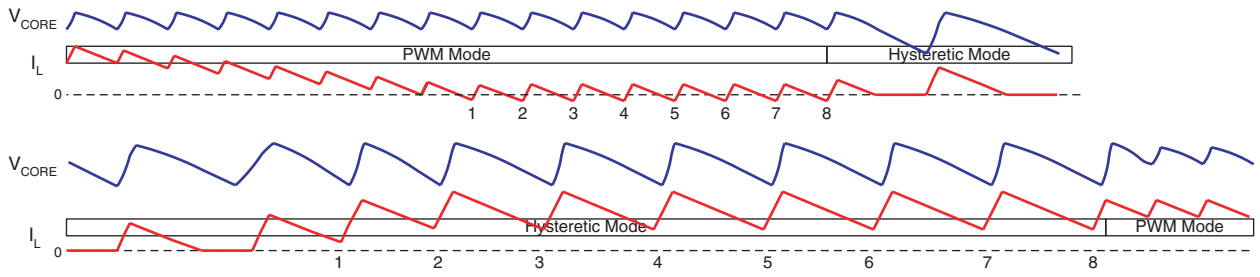


Figure 5. Transitioning Between PWM and Hysteresis

The switching frequency is primarily a function of:

1. Spread between the two hysteretic thresholds
2. I_{LOAD}
3. Output Inductor and Capacitor ESR

A transition back to PWM (Continuous Conduction Mode or CCM) mode occurs when the inductor current has risen sufficient as to be positive for 8 consecutive cycles. This occurs when:

$$I_{LOAD(CCM)} = \frac{\Delta V_{HYSTERESIS}}{2\ ESR} \quad (7)$$

where $\Delta V_{HYSTERESIS}$ = 15mV and ESR is the equivalent series resistance of C_{OUT}.

Because of the different control mechanisms, the value of the load current where transition into CCM operation takes place is typically higher compared to the load level at which transition into hysteretic mode had occurred. Hysteretic mode can be disabled by setting the $\overline{FPWM}$ pin low. The presence of this pin enhances applicability of the controller. Figure 6 shows an application circuit where hysteretic mode is only allowed in a Deep Sleep Extension (DSX) mode. In this mode the CPU has stopped and its current is significantly lower compared to other modes of operation. Using the $\overline{FPWM}$ pin simplifies control over converter modes of operation and increases efficiency.

Current Processing Section

The following discussion refers to Figure 7.

Active Droop

"Active Droop" or voltage positioning is now widely used in the computer power applications. The technique is based on raising the converter voltage at light load in anticipation of a step increase in load current, and conversely, lowering V_{CORE} in anticipation of a step decrease in load current.

With Active Droop, the output voltage varies with the load as if a resistor were connected in series with the converter's output, in other words, it's effect is to raise the output resistance of the converter. To get the most from the Active Droop, its magnitude should be scaled to match the output capacitor's ESR voltage drop.

$$V_{DROOP} = I_{MAX} \times ESR \quad (8)$$

Active Droop allows the size and cost of the output capacitors required to handle CPU current transients to be reduced. The reduction may be almost a factor of 2 when compared to a system without Active Droop.

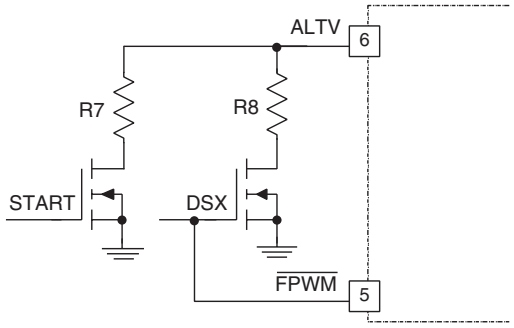


Figure 6. Allowing Hysteretic Mode in Deep Sleep

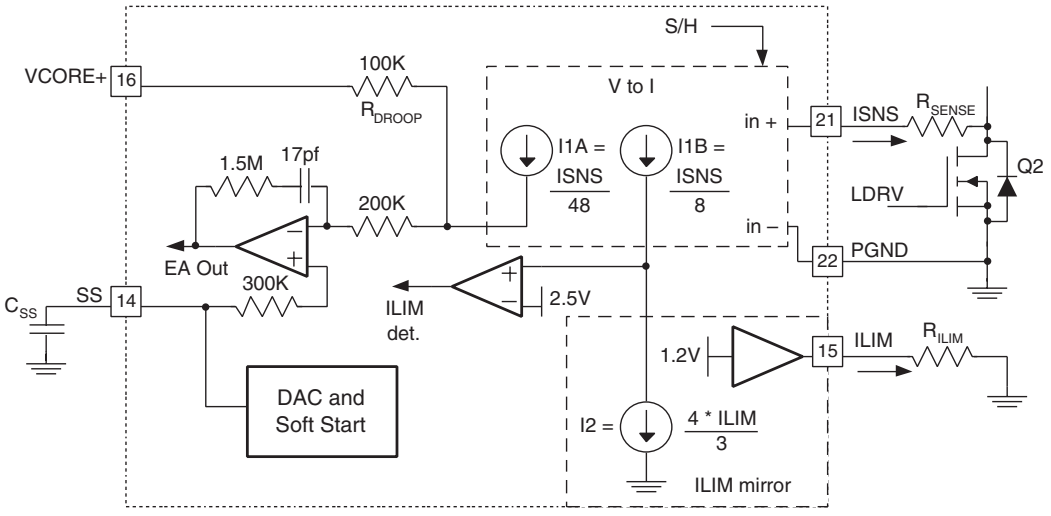


Figure 7. Current Limit and Active Droop Circuits

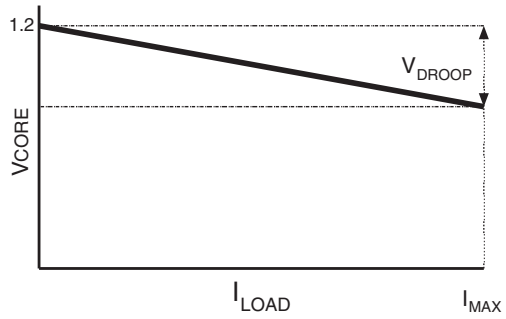


Figure 8. Active Droop

Additionally, the CPU power dissipation is also slightly reduced as it is proportional to the applied voltage squared and even slight voltage decrease translates to a measurable reduction in power dissipated.

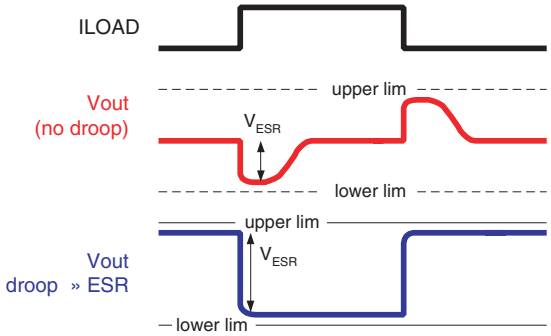


Figure 9. Effect of Active Droop on ESR

The Crusoe™ processor regulation window including transients is specified as +5%…–2%. To accommodate the droop, the output voltage of the converter is raised by about 3.25% at no load as shown below (R24 = 1K and R25 = 30.1K):

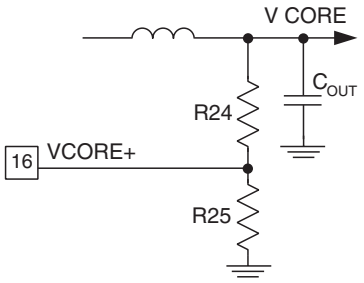


Figure 10. Setting the No-Load Output Voltage Rise

The converter response to the load step is shown in Figure 11. At zero load current, the output voltage is raised ~50mV above nominal value of 1.35V. When the load current increases, the output voltage droops down approximately 55mV. Due to use of Active Droop, the converter's output voltage adaptively changes with the load current allowing better utilization of the regulation window.

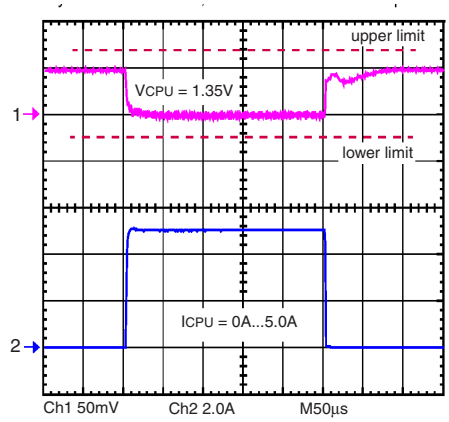


Figure 11. Converter Response to 5A Load Step

The current through R_{SENSE} resistor (ISNS) is sampled shortly after Q2 is turned on. That current is held, and then injected (with a 1/48 gain) into the inverting path of the error amp to produce an offset to the sensed output voltage at V_{CORE} + proportional to the load current.

$$V_{DROOP} = 100K \times \frac{I_{LOAD} \times R_{DS(ON)}}{48 \times R_{SENSE}} \quad (9a)$$

$$V_{DROOP} = 2083 \times \frac{I_{LOAD} \times R_{DS(ON)}}{R_{SENSE}} \quad (9b)$$

Setting the Current Limit

A ratio of ISNS is also compared to the current established when a 1.2 V internal reference drives the ILIM pin. The threshold is determined at the point when the

$$\frac{ISNS}{8} > \frac{ILIM \times 4}{3}$$

Since

$$ISNS = \frac{I_{LOAD} \times R_{DS(ON)}}{R_{SENSE}}$$

therefore,

$$I_{LIMIT} = \frac{1.2V}{R_{LIM}} \times \frac{4}{3} \times \frac{8 \times (100 + R_{SENSE})}{R_{DS(ON)}} \quad (10)$$

Since the tolerance on the current limit is largely dependent on the ratio of the external resistors it is fairly accurate if the voltage drop on the Switching Node side of R_{SENSE} is an accurate representation of the load current. When using the MOSFET as the sensing element, the variation of $R_{DS(ON)}$ causes proportional variation in the ISNS. This value not only varies from device to device, but also has a typical junction temperature coefficient of about 0.4%/°C (consult the MOSFET datasheet for actual values), so the actual current limit set point will decrease proportional to increasing MOSFET die temperature. The same discussion applies to the V_{DROOP} calculation, which has an additional initial error of ±20% due to its value being determined by a ratio between R_{SENSE} and the internal 100K resistor.

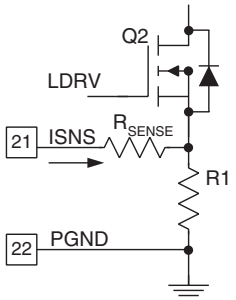


Figure 12. Improving Current Sensing Accuracy

More accurate sensing can be achieved by using a resistor (R1) instead of the RDSon of the FET as shown in Figure 12. This approach causes higher losses, but yields greater accuracy in both V_{DROOP} and I_{LIMIT}. R1 is a low value (e.g. 10mΩ) resistor.

Current limit (I_{LIMIT}) should be set sufficiently high as to allow the output slew rate required by the design, since the output capacitors will have to be charged during this slew.

$$I_{LIMIT} > I_{LOAD} + C_{OUT}\frac{dV}{dt} \quad (11a)$$

The dv/dt term we used earlier in the discussion (set up by the C_{SS}) was 50mV/32µS or 1.56V/mS. In addition, since I_{LIMIT} is a peak current cut-off value, we will need to multiply the result by the inductor ripple current (we'll use 30%). Assuming C_{OUT} of 1000µF, and a maximum load current of 6A the target for I_{LIMIT} would be:

$$I_{LIMIT} > 1.3(6A + (1mF \times 1.56V/mS)) \approx 13A \quad (11b)$$

Gate Driver Section

The gate control logic translates the internal PWM control signal into the MOSFET gate drive signals providing necessary amplification, level shifting and shoot-through protection. Also, it has functions that help optimize the IC performance over a wide range of operating conditions. Since MOSFET switching time can vary dramatically from type to type and with the input voltage, the gate control logic provides adaptive dead time by monitoring the gate-to-source voltages of both upper and lower MOSFETs. The lower MOSFET drive is not turned on until the gate-to-source voltage of the upper MOSFET has decreased to less than approximately 1 Volt. Similarly, the upper MOSFET is not turned on until the gate-to-source voltage of the lower MOSFET has decreased to less than approximately 1 volt. This allows a wide variety of upper and lower MOSFETs to be used without a concern for simultaneous conduction, or shoot-through.

There must be a low – resistance, low – inductance path between the driver pin and the MOSFET gate for the adaptive dead-time circuit to work properly. Any delay along that path will subtract from the delay generated by the adaptive dead-time circuit and a shoot-through condition may occur.

Frequency Loop Compensation

Due to the implemented current mode control, the modulator has a single pole response with -1 slope at frequency determined by load

$$F_{P0} = \frac{1}{2\pi R_O C_O} \quad (12)$$

where R_O is load resistance, C_O is load capacitance. For this type of modulator Type 2 compensation circuit is usually sufficient. To reduce the number of external components and simplify the design task, the PWM controller has an internally compensated error amplifier. Figure 13 shows a Type 2 amplifier and its response along with the responses of a current mode modulator and of the converter. The Type 2 amplifier, in addition to the pole at the origin, has a zero-pole pair that causes a flat gain region at frequencies between the zero and the pole.

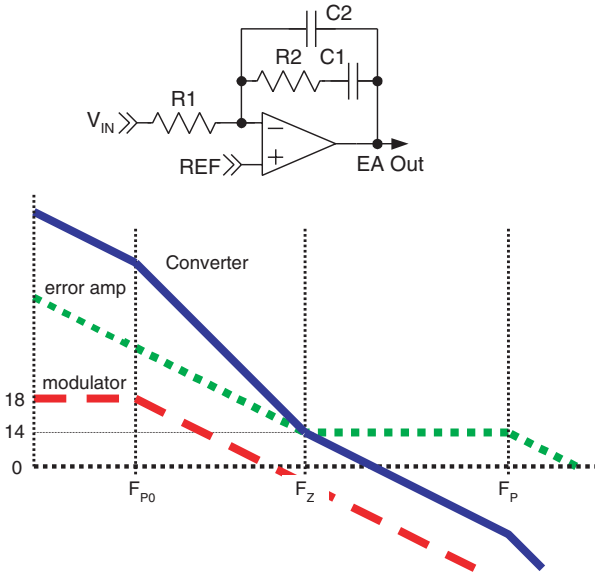


Figure 13. Compensation

$$F_Z = \frac{1}{2\pi R_2 C_1} = 6\ kHz \quad (13a)$$

$$F_p = \frac{1}{2\pi R_2 C_1} = 600\ kHz \quad (13b)$$

This region is also associated with phase 'bump' or reduced phase shift. The amount of phase shift reduction depends on how wide the region of flat gain is and has a maximum value of 90°. To further simplify the converter compensation, the modulator gain is kept independent of the input voltage variation by providing feed-forward of VIN to the oscillator ramp.

The zero frequency, the amplifier high frequency gain and the modulator gain are chosen to satisfy most typical applications. The crossover frequency will appear at the point where the modulator attenuation equals the amplifier high

frequency gain. The only task that the system designer has to complete is to specify the output filter capacitors to position the load main pole somewhere within one decade lower than the amplifier zero frequency. With this type of compensation plenty of phase margin is easily achieved due to zero-pole pair phase ‘boost’.

Conditional stability may occur only when the main load pole is positioned too much to the left side on the frequency axis due to excessive output filter capacitance. In this case, the ESR zero placed within the 10kHz...50kHz range gives some additional phase ‘boost’. Fortunately, there is an opposite trend in mobile applications to keep the output capacitor as small as possible.

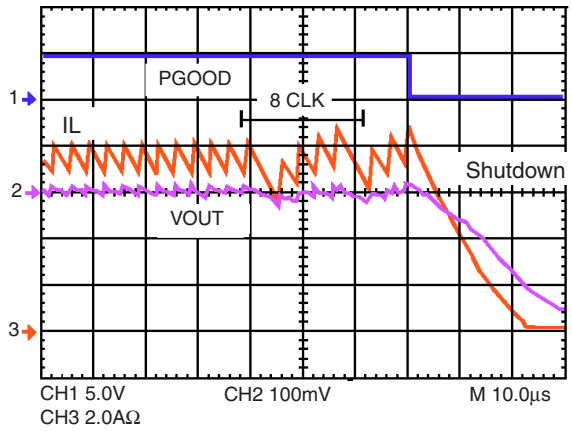
Protection

The converter output is monitored and protected against extreme overload, short circuit, over-voltage and under-voltage conditions.

A sustained overload on the output sets the PGOOD pin low and latches-off the whole chip. Operation can be restored by cycling the VCC voltage or enabling (EN) pin.

Over-Current Sensing

When the circuit's current limit signal (“ILIM det” as shown in Figure 7) goes high, a pulse-skipping circuit is activated. HDRV will be inhibited as long as the sensed current is higher than the ILIM value. This limits the current supplied by the DC input. This condition continues for 8 clock cycles after the over-current comparator was tripped for the first time. If after these first 8 clock cycles the current exceeds the over-current threshold again at any time within the subsequent 8 clock cycles, the overcurrent protection circuit is latched and the chip is disabled. If "ILIM det" goes away during the first 8 clock cycles, normal operation is restored and the over-current circuit resets itself 16 clock cycles after the over-current threshold was exceeded for the first time.



If the load step is strong enough to pull the V_{CORE} + lower than the under-voltage threshold, the chip shuts down

immediately.

Over-Voltage Protection

Should the output voltage exceed 1.9V due to an upper MOSFET failure, or for other reasons, the overvoltage protection comparator will force the LDRV high. This action actively pulls down the output voltage and, in the event of the upper MOSFET failure, will eventually blow the battery fuse. As soon as the output voltage drops below the threshold, the OVP comparator is disengaged.

This OVP scheme provides a ‘soft’ crowbar function which helps to tackle severe load transients and does not invert the output voltage when activated — a common problem for OVP schemes with a latch.

Over-Temperature Protection

The chip incorporates an over temperature protection circuit that shuts the chip down when a die temperature of 150°C is reached. Normal operation is restored at die temperature below 125°C with internal Power On Reset asserted, resulting in a full soft-start cycle.

Design and Component Selection Guidelines

As an initial step, define operating voltage range and minimum and maximum load currents for the controller.

Output Inductor Selection

The minimum practical output inductor value is the one that keeps inductor current just on the boundary of continuous conduction at some minimum load. The industry standard practice is to choose the minimum current somewhere from 15% to 35% of the nominal current. At light load, the controller can automatically switch to hysteretic mode of operation to sustain high efficiency. The following equations help to choose the proper value of the output filter inductor.

$$\Delta I = 2 \times I_{MIN} = \frac{\Delta V_{OUT}}{ESR}$$

where ΔI is the inductor ripple current and ΔV_{OUT} is the maximum ripple allowed.

$$L = \frac{V_{IN} - V_{OUT}}{F_{SW} \times \Delta I} \times \frac{V_{OUT}}{V_{IN}}$$

for this example we'll use:

$$V_{IN} = 20V, V_{OUT} = 1V$$

$$\Delta I = 30\% \times 5A = 1.25A$$

$$F_{SW} = 300KHz$$

Therefore,

$$L \approx 1.8\mu H$$

Output Capacitor Selection

The output capacitor serves two major functions in a switching power supply. Along with the inductor it filters the sequence of pulses produced by the switcher, and it supplies the load transient currents. The filtering requirements are a function of the switching frequency and the ripple current allowed, and are usually easy to satisfy in high frequency converters.

The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. Modern microprocessors produce transient load rates in excess of 10A/µs. High frequency ceramic capacitors placed beneath the processor socket initially supply the transient and reduce the slew rate seen by the bulk capacitors. The bulk capacitor values are generally determined by the total allowable ESR rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the processor power pins as physically possible. Consult with the processor manufacturer for specific decoupling requirements. Use only specialized low-ESR electrolytic capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a transient. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Power MOSFET Selection

For the example in the following discussion, we will be selecting components for:

V_{IN} from 5V to 20V
V_{OUT} = 1.2V @ $I_{LOAD(MAX)}$ = 7A

The FAN5250 converter's output voltage is very low with respect to the input voltage, therefore the Lower MOSFET (Q2) is conducting the full load current for most of the cycle. Therefore, Q2 should be selected to be a MOSFET with low $R_{DS(ON)}$ to minimize conduction losses.

In contrast, Q1 is on for a maximum of 20% (when V_{IN} = 5V) of the cycle, and its conduction loss will have less of an impact. Q1, however, sees most of the switching losses, so Q1's primary selection criteria should be gate charge ($Q_{G(SW)}$).

High-Side Losses:

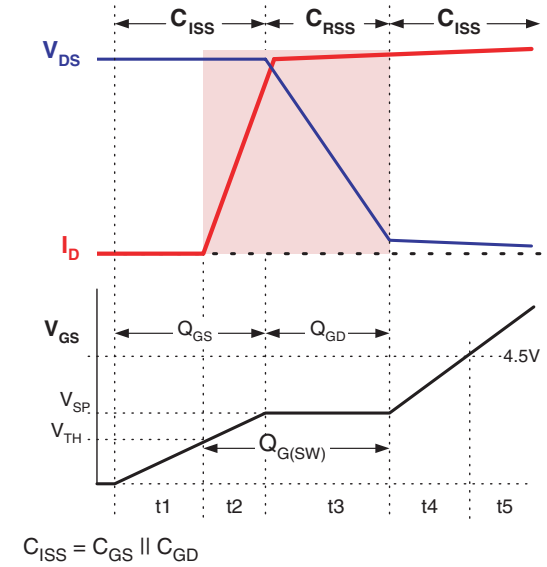


Figure 14. Switching Losses and Q_G

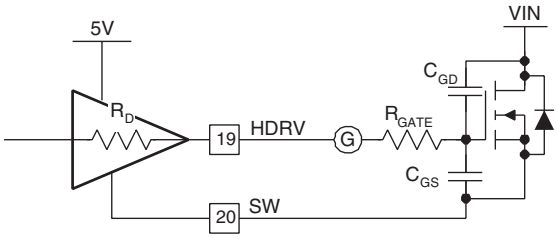


Figure 15. Drive Equivalent Circuit

Assuming switching losses are about the same for both the rising edge and falling edge, Q1's switching losses, as can be seen by Figure 14, are given by:

$$P_{UPPER} = P_{SW} + P_{COND} \quad (14a)$$

$$P_{SW} = \left(\frac{V_{DS} \times I_L}{2} \times 2 \times t_S\right) F_{SW} \quad (14b)$$

$$P_{COND} = \frac{V_{OUT}}{V_{IN}} \times I_{OUT}^2 \times R_{DS(ON)} \quad (14c)$$

Where $R_{DS(ON)}$ is @$T_{J(MAX)}$ and t_S is the switching period (rise or fall time) and is predominantly the sum of t2, t3 (Figure 14), a function of the impedance of the driver and the $Q_{G(SW)}$ of the MOSFET. Since most of t_S occurs when V_{GS} = V_{SP} we can use a constant current assumption for the driver to simplify the calculation of t_S:

$$t_S = \frac{Q_{G(SW)}}{I_{DRIVER}} \approx \frac{Q_{G(SW)}}{\left(\frac{VDD - V_{SP}}{R_{DRIVER} + R_{GATE}}\right)} \quad (15)$$

For the high-side MOSFET, V_{DS} = VIN, which can be as high as 20V in a typical portable application. Q2, however, switches on or off with its parallel shottky diode conducting, therefore $V_{DS} \approx 0.5V$. Since P_{SW} is proportional to V_{DS}, Q2's switching losses are negligible and we can select Q2 based on $R_{DS(ON)}$ only.

Care should also be taken to include the delivery of the MOSFET's gate power (P_{GATE}) in calculating the power dissipation required for the FAN5250:

$$P_{GATE} = Q_G \times VDD \times F_{SW} \quad (16)$$

Low-Side Losses

Conduction losses for Q2 are given by:

$$P_{COND} = (1 - D) \times I_{OUT}^2 \times R_{DS(ON)} \quad (17)$$

where $R_{DS(ON)}$ is the $R_{DS(ON)}$ of the MOSFET at the highest operating junction temperature and $D = \frac{V_{OUT}}{V_{IN}}$ is the minimum duty cycle for the converter. Since D_{MIN} is 5% for portable computers, (1-D) ≈ 1, further simplifying the calculation.

The maximum power dissipation ($P_{D(MAX)}$) is a function of the maximum allowable die temperature of the low-side MOSFET, the θ_{J-A}, and the maximum allowable ambient temperature rise:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\Theta_{J-A}}$$

θ_{J-A}, depends primarily on the amount of PCB area that can be devoted to heat sinking (see FSC app note AN-1029 for SO-8 MOSFET thermal information).

Table 2. Suggested Component Values

	Design 1	Design 2	Design 3
$I_{CPU(MAX)}$	6 A	12 A	18 A
Inductor	1.8µH Sumida CEP1231R8MH	1.0µH Panasonic ETQP6F1R0BFA	0.8µH Panasonic ETQP6F0R8BFA
Output Caps	4 x 220µF Sanyo POSCAP 2R5TPC220M or 3 x 270µF Panasonic EEFUE271R	6 x 220µF Sanyo POSCAP 2R5TPC220M or 5 x 270µF Panasonic EEFUE271R	6 x 270µF Panasonic EEFUE271R
High-Side MOSFETs	FDS6612A	FDS6694	FDS6694
Low-Side MOSFETs	FDS6690S	2 X FDS6672A	2 X FDS7764A
R_{SNS} for 3% droop	3.57K	2.8K	3K

Layout Considerations

Switching converters, even during normal operation, produce short pulses of current which could cause substantial ringing and be a source of EMI if layout constrains are not observed.

There are two sets of critical components in a DC-DC converter. The switching power components process large amounts of energy at high rate and are noise generators. The low power components responsible for bias and feedback functions are sensitive to noise.

A multi-layer printed circuit board is recommended. Dedicate one solid layer for a ground plane. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels.

Notice all the nodes that are subjected to high dV/dt voltage swing such as SW, HDRV and LDRV, for example. All surrounding circuitry will tend to couple the signals from these nodes through stray capacitance. Do not oversize copper traces connected to these nodes. Do not place traces connected to the feedback components adjacent to these traces.

It is not recommended to use High Density Interconnect Systems, or micro-vias on these signals. The use of blind or buried vias should be limited to the low current signals only. The use of normal thermal vias is left to the discretion of the designer.

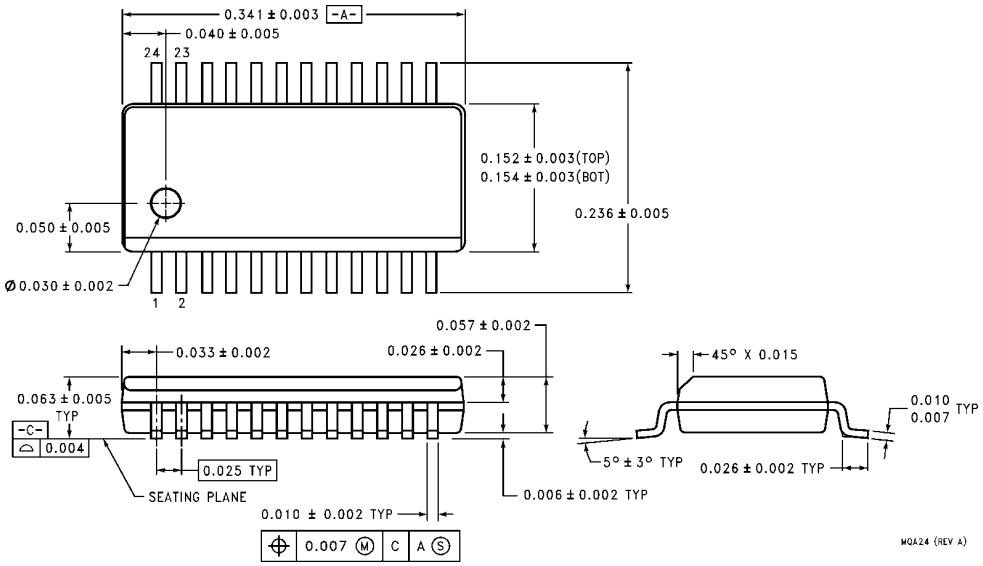
Keep the wiring traces from the IC to the MOSFET gate and source as short as possible and capable of handling peak currents of 2A. Minimize the area within the gate-source path to reduce stray inductance and eliminate parasitic ringing at the gate.

Locate small critical components like the soft-start capacitor and current sense resistors as close as possible to the respective pins of the IC.

The FAN5250 utilizes advanced packaging technology that will have lead pitch of 0.6mm. High performance analog semiconductors utilizing narrow lead spacing may require special considerations in PWB design and manufacturing. It is critical to maintain proper cleanliness of the area surrounding these devices. It is not recommended to use any type of rosin or acid core solder, or the use of flux in either the manufacturing or touch up process as these may contribute to corrosion or enable electromigration and/or eddy currents near the sensitive low current signals. When chemicals such as these are used on or near the PWB, it is suggested that the entire PWB be cleaned and dried completely before applying power.

Mechanical Dimensions

MQA24



24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
Package Number MQA24

Ordering Information

Part Number	Temperature Range	Package
FAN5250QSC	-10°C to 85°C	QSOP-24

3/12/03 0.0m 003
Stock#DS30005250