FAIRCHILD SEMICONDUCTOR™

August 1986
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DM74S161 • DM74S163
Synchronous 4-Bit Binary Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. They are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a LOW level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable input.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be HIGH to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a HIGH-level output pulse with a duration approximately equal to the HIGH-level portion of the Q_A output. This HIGH-level overflow ripple carry pulse can be used to enable successive cascaded stages.

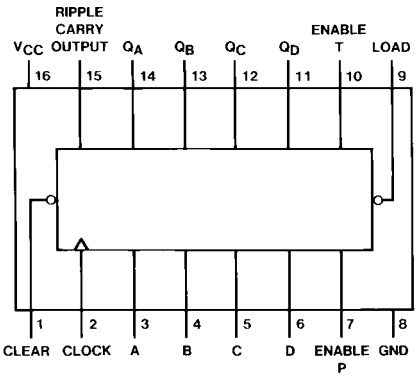
Features

- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs

Ordering Code:

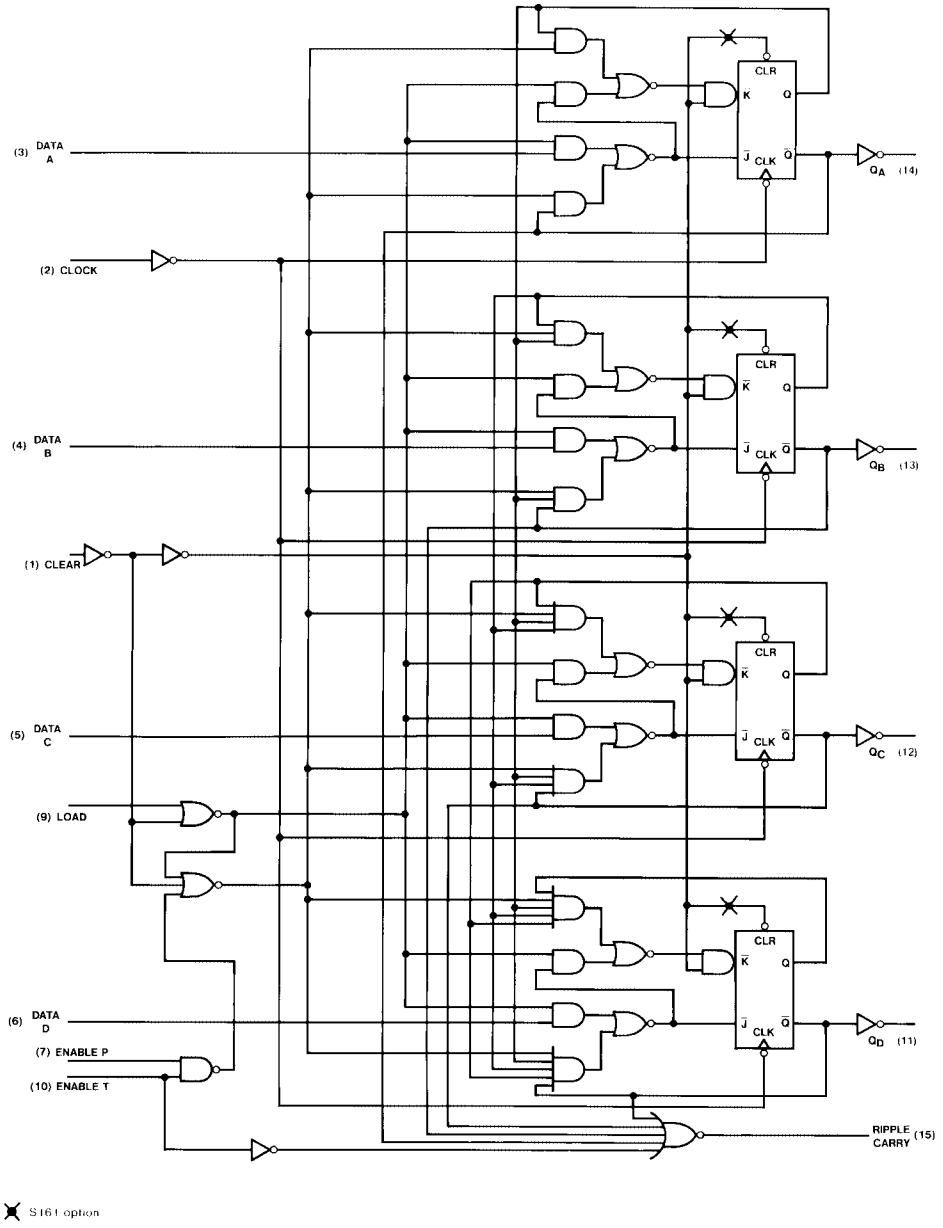
Order Number	Package Number	Package Description
DM74S161N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
DM74S163N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Connection Diagram

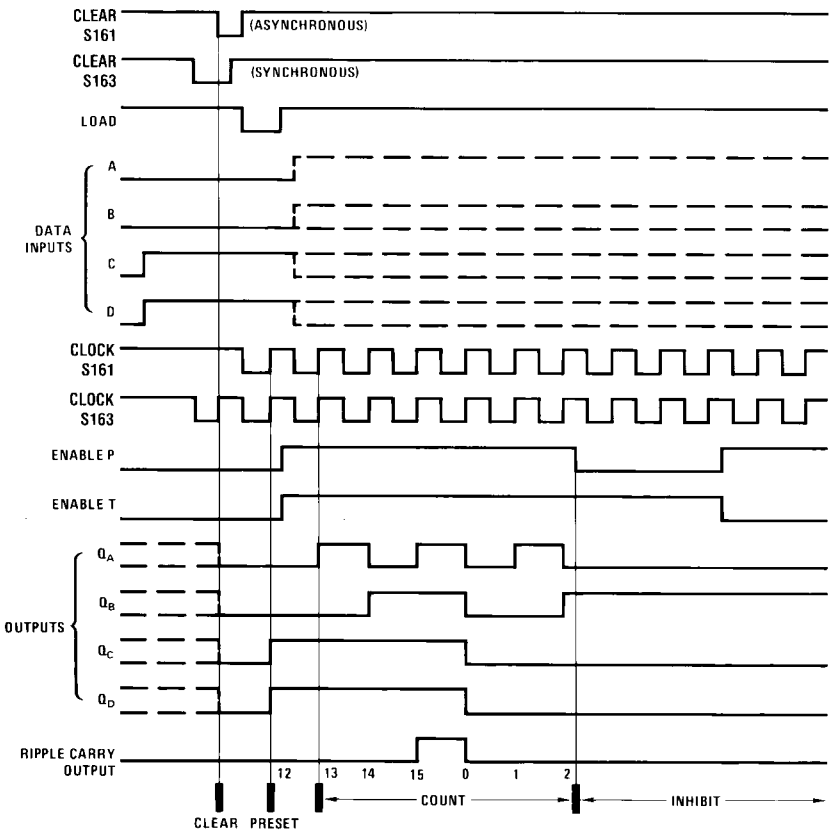


Logic Diagram

DM74S161 • DM74S163



Timing Diagram

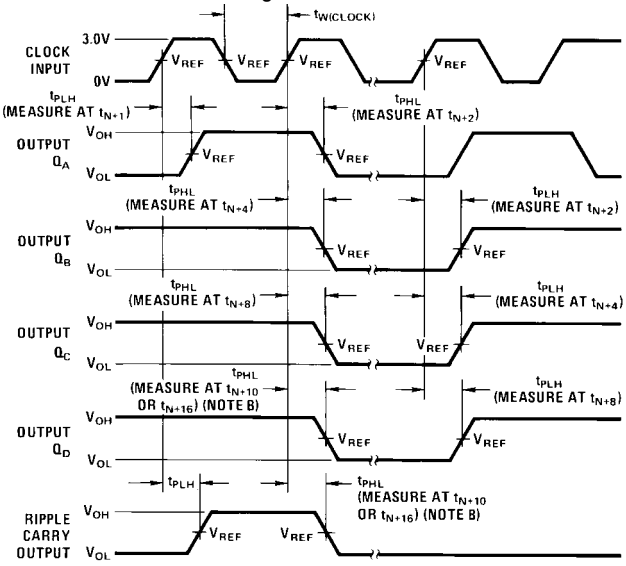


Sequence:

1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one and two
4. Inhibit

Parameter Measurement Information

Switching Time Waveforms

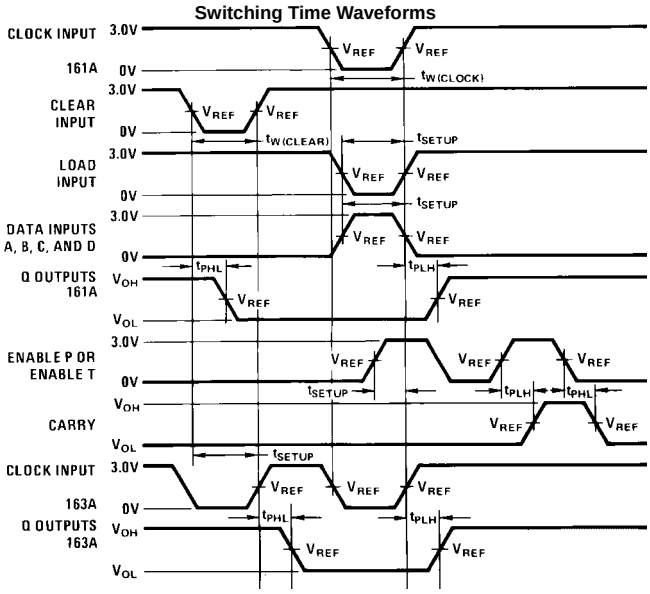


Note A: The input pulses are supplied by generators having the following characteristics:
PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$. For DM74S161/163, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns. Vary PRR to measure f_{MAX}.

Note B: Outputs Q_D and carry are tested at $t_n + 16$ for DM74S161, SM74S163 where t_n is the bit time when all outputs are LOW

Note C: $V_{REF} = 1.5V$.

Switching Time Waveforms



Note A: The input pulses are supplied by generators having the following characteristics:
PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$. $t_r \le 2.5$ ns, $t_f \le 2.5$ ns. Vary PRR to measure f_{MAX}.

Note B: Enable P and enable T setup times are measured at $t_n + 0$.

Note C: $V_{REF} = 1.5V$.

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				−1	mA
I_{OL}	LOW Level Output Current				20	mA
f_{CLK}	Clock Frequency (Note 2)		0		40	MHz
	Clock Frequency (Note 3)		0		35	
t_W	Pulse Width (Note 2)	Clock	10			ns
		Clear (Note 5)	10			
	Pulse Width (Note 3)	Clock	12			
		Clear (Note 5)	12			
t_{SU}	Setup Time (Note 2)	Data	4			ns
		Enable P or T	12			
		Load	14			
		Clear (Note 4)	14			
	Setup Time (Note 3)	Data	5			
		Enable P or T	14			
		Load	16			
		Clear (Note 4)	16			
t_H	Hold Time (Note 2)	Data	3			ns
		Others	0			
	Hold Time (Note 3)	Data	5			
		Others	2			
t_{REL}	Load or Clear Release Time (Note 2)		12			ns
	Load or Clear Release Time (Note 3)		14			
T_A	Free Air Operating Temperature		0		70	°C

Note 2: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 4: Applies only to the DM74S163 which has synchronous clear inputs.

Note 5: Applies only to the DM74S161 which has asynchronous clear inputs.

Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 6)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	LOW Level Input Current	V_{CC} = Max	CLK, Data			50	µA
		V_I = 2.7V	Others	−10		−200	
I_{IL}	LOW Level Input Current	V_{CC} = Max	Enable T			−4	mA
		V_I = 0.5V	Others			−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 7)		−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max			95	160	mA

Note 6: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 7: Not more than one output should be shorted at a time, and the duration should not exceed one second.

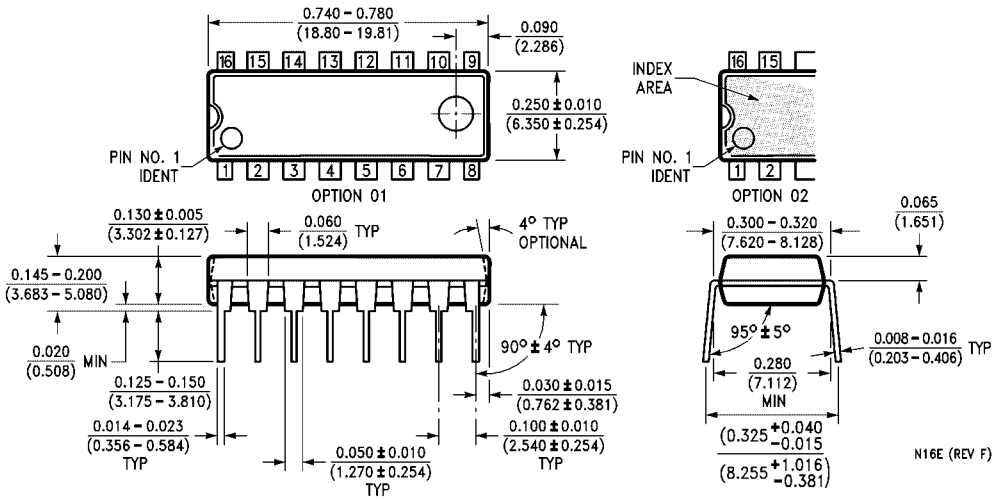
Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		40		35		MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Ripple Carry		25		25	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Ripple Carry		25		28	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Any Q		15		15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Any Q		15		18	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable T to Ripple Carry		15		18	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable T to Ripple Carry		15		18	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output (Note 8)	Clear to Any Q		20		24	ns

Note 8: Propagation delay for clearing is measured from clear input for the DM74S161 and from the clock input transition for the DM74S163.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E